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ORIGINAL RESEARCH

# MDGN: Circuit design of memristor-based denoising autoencoder and gated recurrent unit network for lithium-ion battery state of charge estimation

Jiayang Wang[1] | Xinghao Zhang[1] | Yifeng Han[2] | Chun Sing Lai[3] | Zhekang Dong[1] | Guojin Ma[1] | Mingyu Gao[1]

[1]The School of Electronics and Information, Hangzhou Dianzi University, Hangzhou, China

[2]The College of Electrical Engineering, Zhejiang University, Hangzhou, China

[3]The Department of Electronic and Electrical Engineering, Brunel University London, London, UK

**Correspondence**
Zhekang Dong, The School of Electronics and Information, Hangzhou Dianzi University, Hangzhou, China.
Emai: englishp@126.com

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**Abstract**

Due to the highly complex and non-linear physical dynamics of lithium-ion batteries, it is unfeasible to measure the state of charge (SOC) directly. Designing systems capable of accurate SOC estimation has become a key technology for battery management systems (BMS). Existing mainstream SOC estimation approaches still suffer from the limitations of low efficiency and high-power consumption, owing to the great number of samples required for training. To address these gaps, this paper proposes a memristor-based denoising autoencoder and gated recurrent unit network (MDGN) for fast and accurate SOC estimation of lithium-ion batteries. Specifically, the DAE circuit module is designed to extract useful feature representation with strong generalization and noise immunity. Then, the gated recurrent unit (GRU) circuit module is designed to learn the long-term dependencies between high-dimensional input and output data. The overall performance is evaluated by root mean square error (RMSE) and mean absolute error (MAE) at 0, 25, and 45°C, respectively. Compared with the current state-of-the-art methods, the entire scheme shows its superior performance in accuracy, robustness, and operation cost (referring to time cost).

## 1 | INTRODUCTION

Considering the root of the climate change may be the high-mass carbon emissions, it is necessary to develop clean and efficient energy devices and systems. Lithium-ion battery with eco-friendly nature, fast charging efficiency, long service life, low self-discharge rate, and low maintenance cost has been regarded as a potential remedy to relieve climate change [1]. So far, lithium-ion batteries have been widely used in electric vehicles (EV) and energy storage power stations [2]. The state of charge (SOC) representing the ratio between the available capacity and rated capacity is an important parameter to evaluate the performance of batteries used as energy storage devices [3]. Since the lithium-ion battery is a highly time-invariant, non-linear, and complex electrochemical system, direct measurement of SOC is difficult and challenging. How to design a vehicle-mounted computing system that enables fast and accurate SOC estimation is gradually becoming a key technology in low carbon energy systems [4].

Currently, SOC estimation algorithms can be roughly divided into three sorts, that is, traditional estimation methods, control theory-based (CTB) methods, and the data driven-based (DDB) methods [4].

1. For traditional methods, they are easy to implement, but are susceptible to the interference of temperature and noise, leading to a large error in the final estimation [5–7].
2. For CTB methods, considering that the non-linear properties of the battery are difficult to characterize, the model-building process is relatively complex and time-consuming.

Meanwhile, the CTB method is always designed for a specific battery model, which means this kind of estimation method is lack of universality, especially for different lithium-ion batteries [8–10].

3. For DDB methods, the lithium-ion battery is considered a black box, and it is possible to achieve the estimation by analyzing the non-linear relationship between the battery measurement data (e.g. temperature, voltage, current) and SOC without considering both the internal mechanism and battery type [11–20]. Theoretically, SOC estimation is a time series prediction problem with previous and current measurement data, recurrent neural networks (RNNs) and their variants, for example, the long short-term memory (LSTM) and gated recurrent unit (GRU) neural networks have been widely used to deal with this estimation task [11–13]. For example, Xi et al. [11] proposed a time-delayed RNN for SOC estimation. Yang et al. [12] investigated a LSTM network with multiple hidden layers to estimate SOC of lithium-ion batteries and verified its superior performance. Jiao et al. [13] employed a GRU network to estimate SOC and optimized the weights of the network with a momentum gradient method. However, these single network-based methods are susceptible to noise interference and fail to achieve stronger robustness [14]. To address this issue, a lot of hybrid intelligent estimation methods have been developed [14–20]. While almost all these methods are pure software-based methods, high estimation accuracy also brings new challenges, that is, the high computational burden and high latency [20]. Hence, exploring the hardware implementation for accurate and time-saving EV SOC estimation is an effective way.

Nanoscale memristor is a potential candidate for addressing the research gaps in computational complexity and energy consumption, due to their excellent characteristics such as low power consumption, non-volatility, fast resistance switching, compatibility with Complementary Metal Oxide Semiconductor (CMOS), and the ability of performing computational operations in parallel with extremely high efficiency in the crossbar array [21–23]. In this paper, we present a memristor-based hybrid neural network to perform the EV SOC estimation task, aiming to deal with the noise interference issue (emerging in traditional methods) and high computational cost (emerging in DDB methods). The main contributions of this paper are summarized below:

1. The circuit design scheme of denoising autoencoder (DAE) and GRU network are both proposed using the nanoscale memristors. The former is used to deal with the noise interference issue, the latter is responsible for sequence estimation. Notably, it is the first attempt to use the hardware-based GRU network for sequence estimation.
2. Different with the pure software-based methods, a hybrid hardware circuit framework (MDGN), containing the DAE circuit model, GRU circuit module, and other necessary peripheral circuit module, is proposed to perform the accurate and fast EV SOC estimation task under different temperature and working conditions.
3. This work integrates nanoscience, materials science, and life science, which provides a good reference for future interdisciplinary research, especially in lower carbon energy systems.

The rest of the paper is organized as follows. Section 2 briefly introduces the memristor background and details the mathematical and PSPICE models of Ag/$TiO_x$ nanobelt/Ti memristor. Section 3 provides the hybrid network topology composed by DAE and GRU network. The corresponding hybrid hardware circuit framework is proposed in Section 4. In Section 5, a series of contrast experiments with comprehensive analysis are executed to demonstrate the superiority of the proposed MDGN in SOC estimation. The limitations of the proposed method and directions for future improvements are discussed in Section 6. Finally, Section 7 summarizes the whole work.

## 2 | MEMRISTOR BACKGROUND

Memristor was first introduced by Professor Chua in 1971 and physically implemented by Hewlett-Packard Laboratory in 2008. This nanoscale device is a passive two-terminal circuit component, representing the relationship between the charge $q$ and the magnetic flux $\varphi$, with the following equation [24].

$$M = \frac{d\varphi}{dq} \tag{1}$$

where $M$ denotes the resistance value of the memristor.

The successful fabrication of the memristor has aroused widespread interest from research scholars worldwide due to its superior non-volatility properties, ultra-low power consumption, and ability to be compatible with CMOS. So far, numerous different types of memristor models have been developed [25–27], such as HP memristor, spintronic memristor, voltage threshold adaptive memristor etc.

In this paper, we use the Ag/$TiO_x$ nanobelt/Ti memristor [27]. This device exhibits non-standard faradic capacitance (NFC), battery-like capacitance (BLC), and resistive switching (RS) characteristics at ambient humidity of 0%, 35%–45%, and 95%–100%, respectively. Notably, the relative humidity of the Ag/$TiO_x$ nanobelt/Ti memristor discussed in this paper is maintained at 95% to 100%. According to [27], the $V$–$I$ relationship of the Ag/$TiO_x$ nanobelt/Ti memristor can be mathematically expressed by

$$i = \begin{cases} a_1 \cdot x \cdot \exp(b_1 \cdot x^3 + 1) \cdot \sinh(c_1 \cdot (v - v_{th1})^3 + d_1), v < 0 \\ a_2 \cdot x \cdot \exp(b_2 \cdot x^3 + 1) \cdot \sinh(c_2 \cdot (v - v_{th2})^3 + d_2), v > 0 \end{cases} \tag{2}$$

where $i$ is the current passing through the memristor, $v$ is the applied voltage, $x$ is the state variable representing the electrical conductivity of the memristor, $a_1$, $a_2$, $b_1$, $b_2$, $c_1$, $c_2$, $d_1$, and $d_2$ are all the fitting parameters, and $\sinh(\cdot)$ is a non-linear function.

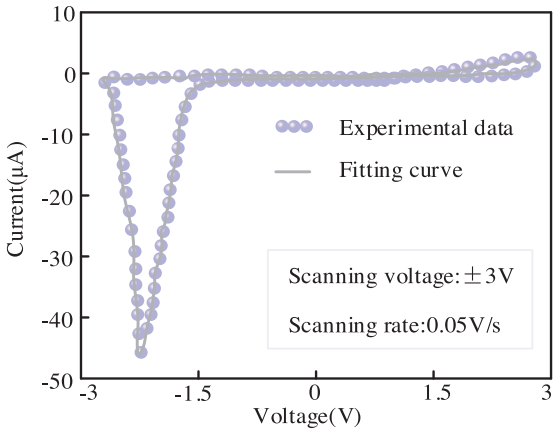


**FIGURE 1** *V–I* characteristics of the Ag/$TiO_x$ nanobelt/Ti memristor.

Further, the dynamic equation for state variable $x(t)$ is expressed as follows:

$$\frac{dx}{dt} = h(v) \cdot f(x) \tag{3}$$

$$h(v) = \begin{cases} k_L \cdot (v - v_{th1})^{\alpha_L}, & v < v_{th1} < 0 \\ 0, & v_{th1} \le v \le v_{th2} \\ k_H \cdot (v - v_{th2})^{\alpha_H}, & 0 < v_{th2} < v \end{cases} \tag{4}$$

$$f(x) = \begin{cases} f_L(x) = \exp\left(-\exp\left(\frac{a_L - x}{w_c}\right)\right) \\ f_H(x) = \exp\left(-\exp\left(\frac{x - a_H}{w_c}\right)\right) \end{cases} \tag{5}$$

where $f(x)$ denotes the window function, it is used to keep the state variable $x$ in the range of $[x_{min}, x_{max}]$. When $x = x_{min}$, the resistance of the memristor is $R_H$; Conversely, when $x = x_{max}$, the resistance of the memristor is $R_L$. $v_{th1}$ and $v_{th2}$ are the negative and positive threshold voltages, respectively. $k_L$, $k_H$, $\alpha_L$, $\alpha_H$, $a_L$, $a_H$, and $w_c$ are the fitting parameters of the memristor model.

Figure 1 demonstrates the *V–I* curve of the Ag/$TiO_x$ nanobelt/Ti memristor. The specific device parameters can be found in the Appendix Table 1 (i.e. the PSPICE circuit model). Notably, the grey solid line is the fitting result generated by Equations (2) to (5), and the purple dot line is the measured *V-I* values of the real Ag/$TiO_x$ nanobelt/Ti memristor. It can be seen that the memristor behaves RS characteristics and the current has asymmetry at positive and negative voltages.

## 3 | NETWORK TOPOLOGIES

Figure 2 depicts the overview of the proposed hybrid neural network framework.

From Figure 2, the entire network framework is composed by DAE and GRU connected in a cascaded configuration. Specifically, after training the DAE network, the output layer, which implements the decoding operation, is removed. Then the hidden vector values are transferred to the input layer of the GRU network for subsequent training and testing.

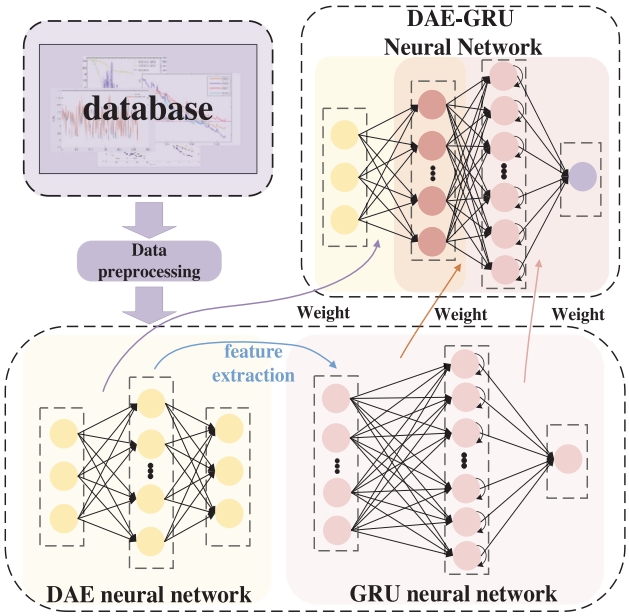


**FIGURE 2** DAE-GRU neural network framework. DAE, denoising autoencoder; GRU, gated recurrent unit.

To facilitate the comprehension of the network topology design, we describe it using two modules, that is, DAE module and GRU module, which implements the denoising and estimation functions, respectively.

### 3.1 | DAE neural network

By adding a noise to the input layer of the autoencoder (AE) neural network, DAE is designed to prevent overfitting problem in AEs and deal with the complete conditions [28]. Meanwhile, DAE prevents replication of inputs to outputs robotically and forces it learn efficient representations of data.

The DAE neural network consisting of three layers (i.e. the input layer, hidden layer, and output layer) mainly performs two operations, that is, the encoding and decoding operation. The structure of the DAE neural network is shown in Figure 3.

From Figure 3, the vector $\boldsymbol{x}_{noise}$ is considered the input layer data after adding some noise to the original data $\boldsymbol{x}_{in}$. Subsequently, an encoding operation is performed on the input layer to obtain $\boldsymbol{h}$. The final output $\boldsymbol{z}$ is derived by performing a decoding to the hidden layer. The specific operation mechanism of DAE can be described by

$$\mathbf{x}_{noise} = \mathbf{A} \cdot \mathbf{x}_{in} \tag{6}$$

$$\mathbf{h} = f(\mathbf{W}_{encoder} \cdot \mathbf{x}_{noise} + b_{encoder}) \tag{7}$$

$$\mathbf{z} = g(\mathbf{W}_{decoder} \cdot \mathbf{h} + b_{decoder}) \tag{8}$$

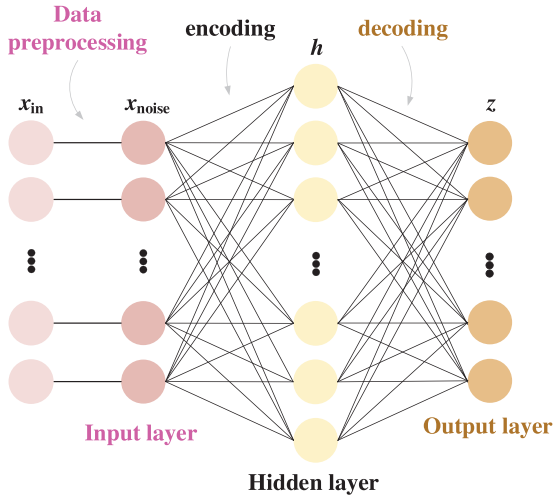


**FIGURE 3** DAE neural network structure. DAE, denoising autoencoder.

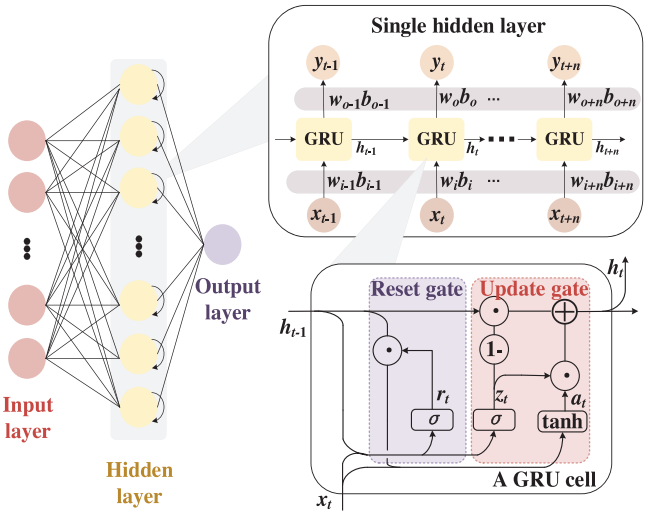


**FIGURE 4** GRU neural network structure. GRU, gated recurrent unit.

where $\boldsymbol{A}$ represents a random matrix with only elements 0 and 1. $\boldsymbol{W}_{\text{encoder}}$, $\boldsymbol{W}_{\text{decoder}}$, $b_{\text{encoder}}$, and $b_{\text{decoder}}$ are all network parameters for the implementation of encoder and decoder. Both $f(\cdot)$ and $g(\cdot)$ act as non-linear activation functions.

The target of DAE is to recover the corrupted data to the original data, that is, the final output result $\boldsymbol{z}$ should be as close as possible to the original data $\boldsymbol{x}_{\text{in}}$. Therefore, the loss function can be obtained by

$$l = \frac{1}{n}\sum_{i=1}^{n}\left\|\mathbf{z}^{(i)} - \mathbf{x}_{\text{in}}^{(i)}\right\|^2 \tag{9}$$

where $l$ is the error in the training process of the DAE network, and $n$ denotes the length of the training samples.

## 3.2 | GRU neural network

Traditional RNNs suffer from the gradient explosion or disappearance problem, which makes them fail to learn long-term dependencies [29]. Aiming to solve such gradient problems, the GRU network with a simple structure, few parameters, and fast execution is selected in this work.

As shown on the left of Figure 4, the GRU neural network is usually handled by a hidden layer used to preserve historical information for time series problems. The refined structure of hidden layer units is shown in the upper right of Figure 4. GRU has two gates, that is, the update gate and the reset gate, to store and filter information. With the update gate the amount of information available to pass from the previous state to the next state is controlled. A larger value of the update gate means that there is more input information to be obtained. The reset gate determines how much of the previous information needs to be ignored. A smaller value of the reset gate indicates that more information from the previous state remains forgotten. The schematic diagram of a GRU cell is shown in the bottom right of Figure 4; its internal operating mechanism is mathematically expressed by

$$\begin{bmatrix} r_t \\ z_t \end{bmatrix} = \sigma\left(\begin{bmatrix} W_r & U_r & b_r \\ W_z & U_z & b_z \end{bmatrix}\begin{bmatrix} x_t \\ h_{t-1} \\ 1 \end{bmatrix}\right) \tag{10}$$

$$\mathbf{a}_t = \tanh\left(\mathbf{W}_h\mathbf{x}_t + \mathbf{U}_h\left[\mathbf{h}_{t-1} \odot \mathbf{r}_t\right] + b_h\right) \tag{11}$$

$$\mathbf{h}_t = \left[1 - \mathbf{z}_t\right] \odot \mathbf{h}_{t-1} + \mathbf{z}_t \odot \mathbf{a}_t \tag{12}$$

where $\boldsymbol{x}_t$ denotes the input vector, $\boldsymbol{r}_t$ and $\boldsymbol{z}_t$ are the values of the update gate and reset gate respectively. $\boldsymbol{h}_t$ and $\boldsymbol{h}_{t\text{-}1}$ are the output of the hidden layer at time steps $t$ and $t-1$. $\boldsymbol{a}_t$ denotes the candidate state. $\boldsymbol{W}$ ($\boldsymbol{W}_r$, $\boldsymbol{W}_z$, $\boldsymbol{W}_h$), $\boldsymbol{U}$ ($\boldsymbol{U}_r$, $\boldsymbol{U}_z$, $\boldsymbol{U}_h$), and $b$ ($b_r$, $b_z$, and $b_h$) are all the network parameters, which represent the weight values and biases values. tanh(·) and σ(·) represent the hyperbolic tangent function and sigmoid function, respectively, and ⊙ is the elemental multiplication, known as Hadamard Product.

# 4 | CIRCUIT DESIGN OF DAE-GRU HYBRID NETWORK

In this section, the specific hardware circuit design of the hybrid DAE-GRU network (i.e. MDGN) is proposed. To illustrate the entire framework, two main components, that is, DAE and GRU circuit module, are described below.

## 4.1 | Circuit design of DAE module

Figure 5 describes the circuit design of the memristor-based DAE module. The entire DAE neural network circuit consists of two main subcircuits for performing matrix vector multiplication and activation function, respectively. Since the inputs and outputs of the designed circuit are all voltages, mathematical

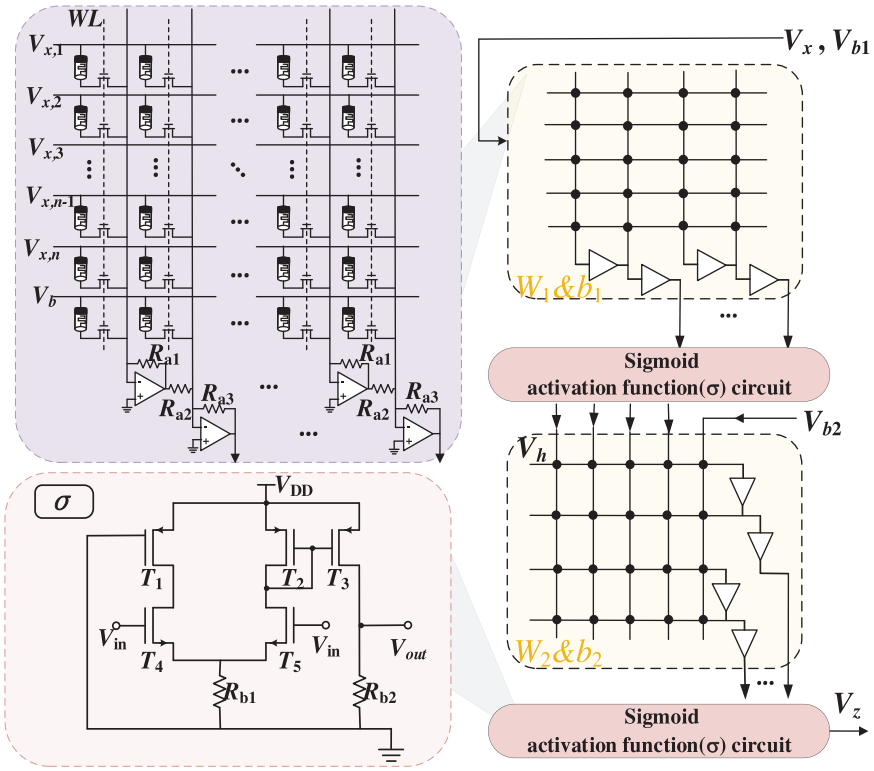


**FIGURE 5** Circuit design of memristor-based DAE neural network. DAE, denoising autoencoder.

Equations (7) and (8) representing the DAE module are rewritten in the following form:

$$\mathbf{V}_h = \sigma(\mathbf{W}_1 \cdot \mathbf{V}_x + V_{b1}) \tag{13}$$

$$\mathbf{V}_{\tilde{z}} = \sigma(\mathbf{W}_2 \cdot \mathbf{V}_h + V_{b2}) \tag{14}$$

where $\boldsymbol{V}_x$, $\boldsymbol{V}_h$ and $\boldsymbol{V}_{\tilde{z}}$ are the voltage vectors corresponding to the vectors $\boldsymbol{x}_{\text{noise}}$, $\boldsymbol{h}$ and $\tilde{\boldsymbol{z}}$, respectively. The matrices $\boldsymbol{W}_1$ and $\boldsymbol{W}_2$ match $\boldsymbol{W}_{\text{encoder}}$ and $\boldsymbol{W}_{\text{decoder}}$, respectively. $V_{b1}$ and $V_{b2}$ are the voltage forms of biases $b_{\text{encoder}}$ and $b_{\text{decoder}}$.

Specifically, the elements $V_{h,j}$ that make up the voltage vector $\boldsymbol{V}_h$ in Equation (13) are given by

$$V_{h,j} = \sigma\left(\sum_{i=1}^{n}\sum_{j=1}^{m}\left(G_{i,2j} - G_{i,2j-1}\right)\cdot V_{x,i} + V_{b1}\right) \tag{15}$$

where $G_{i,2j}$ and $G_{i,2j\text{-}1}$ are the conductance of the adjacent column memristors. $V_{x,i}$ denote the elements composing the vector $\boldsymbol{V}_x$. Similarly, Equation (14) can also be expressed in this form.

$\boldsymbol{W}_1$ & $b_1$ and $\boldsymbol{W}_2$ & $b_2$ are represented by the one transistor one memristor (1T1M) crossbar structure. Positive, zero, and negative weights (e.g. $\boldsymbol{W}_1$ and $\boldsymbol{W}_2$) are achieved using the conductance difference between two adjacent columns of memristors in the crossbar array. In particular, the 1T1M crossbar array can solve the current leakage problem of the crossbar array constructed by only memristors, thus improving the accuracy of matrix vector multiplication. The regular resistors $R_{a1}$ and $R_{a2}$ with equal resistance values are set to achieve $\boldsymbol{W}_1 \cdot \boldsymbol{V}_x + V_{b1}$ and $\boldsymbol{W}_2 \cdot \boldsymbol{V}_h + V_{b2}$.

In this paper, the sigmoid activation functions are chosen for the $f(\cdot)$ and $g(\cdot)$ functions in the DAE neural network. As shown in the bottom left corner of Figure 5, the sigmoid function circuit consists of five Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistors (two N-Metal-Oxide-Semiconductor (NMOS) transistors, three P-Metal-Oxide-Semiconductor (PMOS) transistors) and two regular resistors. The lengths of the transistors are all 0.18 $\mu$m, and the widths of $T_1$, $T_2$, $T_3$, $T_4$, and $T_5$ are 1.8 , 1.8, 10, 0.9, and 0.9 $\mu$m. The regular resistors $R_{b1}$ and $R_{b2}$ have resistances of 5 and 25 k$\Omega$, respectively.

## 4.2 | Circuit design of GRU module

Based on Equations (10) to (12), the circuit design of the GRU module is supposed to contain matrix vector multiplication circuit, sigmoid activation function circuit, hyperbolic tangent activation function circuit, and several basic arithmetic circuit modules that can implement addition, subtraction, and multiplication. The memristor-based circuit for a GRU cell is shown in Figure 6.

The circuit for implementing the matrix vector multiplication operation in Equations (10) and (11) is along the same lines as the above-mentioned matrix vector multiplication circuit. Notably, the GRU module circuit contains six memristor crossbar arrays that are divided into representative network parameters $\boldsymbol{W}_r$, $\boldsymbol{W}_{\tilde{z}}$, $\boldsymbol{W}_h$, $\boldsymbol{U}_r$ & $b_r$, $\boldsymbol{U}_{\tilde{z}}$ & $b_{\tilde{z}}$, and $\boldsymbol{U}_h$ & $b_h$.

In this work, the sigmoid activation function circuit can be derived from the activation function circuit in the DAE module. Meanwhile, the hyperbolic tangent activation function circuit

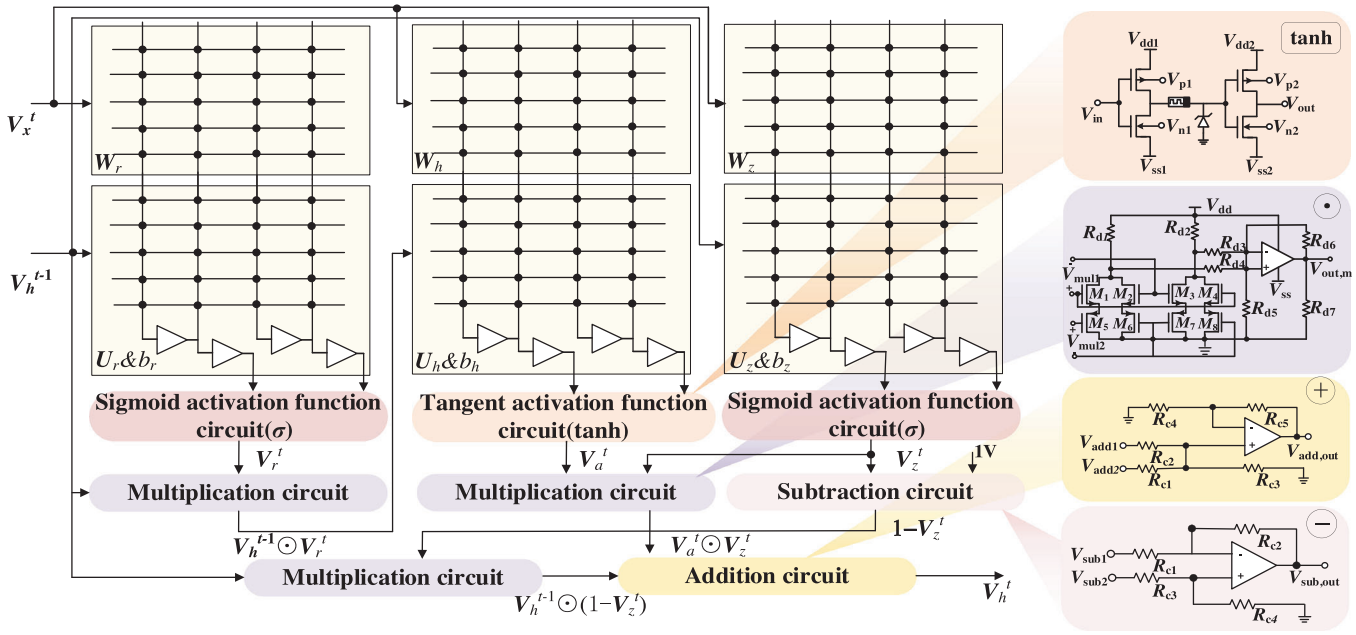


**FIGURE 6** Circuit design of memristor-based GRU cell. GRU, gated recurrent unit.

is designed with the specific configuration of four transistors, one voltage regulator diode, and one memristor. Also, the corresponding circuit parameters $V_{dd1}$, $V_{dd2}$, $V_{p1}$, $V_{p2}$, $V_{n1}$, $V_{n2}$, $V_{ss1}$, $V_{ss2}$ are set as 1.3, 1.3, 0.4, 0.5, −1.2, −0.4, −0.5, −1.1 V, respectively.

In the basic circuit arithmetic modules, the addition and subtraction circuits are mainly realized by the joint action of operational amplifiers and regular resistors, ensuring that $R_{c1} = R_{c2} = R_{c3} = R_{c4} = 0.5R_{c5}$. The implementation of element-wise multiplication operations usually requires the additional CMOS transistors. Since the output values of both the tanh function and the sigmoid function will be served as the input to the multiplier, the input values are either positive or negative. A four-quadrant multiplier is preferred for the inter-element multiplication operation. Set the width and length of transistors $M_1$, $M_2$, $M_3$, $M_4$ to 1.6/0.18 $\mu$m, $M_5$, $M_6$, $M_7$, $M_8$ to 2.0/0.2 $\mu$m, the resistance value of resistors $R_{d1}$∼$R_{d6}$ to 20 kΩ, and $R_{d7}$ to 10 kΩ.

Therefore, according to the designed circuit, the output voltage of the reset gate, update gate, and the whole GRU cell can be expressed as the following mathematical equation:

$$\mathbf{V}_r^t = \sigma\left(\mathbf{W}_r \cdot \mathbf{V}_x^t + \mathbf{U}_r \cdot \mathbf{V}_h^{t-1} + V_{b,r}\right) \tag{16}$$

$$\mathbf{V}_z^t = \sigma\left(\mathbf{W}_z \cdot \mathbf{V}_x^t + \mathbf{U}_z \cdot \mathbf{V}_h^{t-1} + V_{b,z}\right) \tag{17}$$

$$\mathbf{V}_a^t = \tanh\left(\mathbf{W}_h \cdot \mathbf{V}_x^t + \mathbf{U}_h \cdot \left(\mathbf{V}_h^{t-1} \odot \mathbf{V}_r^t\right) + V_{b,h}\right) \tag{18}$$

$$\mathbf{V}_h^t = \left(1 - \mathbf{V}_z^t\right) \odot \mathbf{V}_h^{t-1} + \mathbf{V}_z^t \odot \mathbf{V}_a^t \tag{19}$$

where $\boldsymbol{V}_x^t$, $\boldsymbol{V}_r^t$, $\boldsymbol{V}_z^t$, $\boldsymbol{V}_a^t$, $\boldsymbol{V}_h^t$, and $\boldsymbol{V}_h^{t-1}$ represent the voltage vectors corresponding to the vectors $\boldsymbol{x}_t$, $\boldsymbol{r}_t$, $\boldsymbol{z}_t$, $\boldsymbol{a}_t$, $\boldsymbol{h}_t$, and $\boldsymbol{h}_{t-1}$ in Equations (10) to (12), respectively. $V_{b,r}$, $V_{b,z}$, and $V_{b,b}$ are the voltage forms of biases $b_r$, $b_z$, and $b_h$, respectively.

**TABLE 1** Parameters of Samsung 18650-20R battery.

| Nominal capacity | Nominal voltage | Weight | Maximum charge voltage | Minimum discharge voltage |
|---|---|---|---|---|
| 2000 mAh | 3.6 V | 45.0 g | 4.2 V | 2.5 V |

## 5 | APPLICATION IN SOC ESTIMATION

To evaluate the effectiveness and practicality of the proposed method MDGN, we utilize it to estimate the remaining charge of the lithium-ion battery and conduct a series of comparison tests with the current state-of-the-art methods.

### 5.1 | Experiment environment

The proposed memristor-based DAE-GRU neural network is used for forward computation and the error back-propagation operation is performed on a desktop workstation with the Intel Core i7 10700K processor with 32.0GB RAM running PyCharm 2022.

### 5.2 | Dataset and parameter setting

The public lithium-ion battery dataset, namely Center for Advanced Life Cycle Engineering (CALCE), collected from the Samsung 18650-20R batteries is used in this part [30]. The specific battery parameters are shown in Table 1.

**TABLE 2** Train data and test data allocation during the tests.

| Tests | Training data | Test data |
|---|---|---|
| Test 1 | US06 | FUDS |
| | BJDST | |
| | DST | |
| Test 2 | BJDST | US06 |
| | DST | |
| | FUDS | |
| Test 3 | DST | BJDST |
| | FUDS | |
| | US06 | |
| Test 4 | FUDS | DST |
| | US06 | |
| | BJDST | |

The dataset involves the voltage and current data at ambient temperatures of 0, 25, and 45°C in BJDST, FUDS, US06, and DST driving cycles. We have taken three conditions in four driving cycles as training data and one as test data for a total of four ($C_4^3$) tests, and the specific data allocation during the experiment is described in Table 2. Notably, during the battery discharge process, there is a significant downward trend in SOC if it falls below 80%. For effective alleviation of mileage anxiety, the discharge data with the initial SOC of 80% are chosen in the tests.

Before applying the designed DAE-GRU neural network circuit via memristor circuits to SOC estimation, the numbers of nodes in the input, hidden, and output layers of the DAE and GRU neural networks are set to 3, 30, 3, 30, 150, and 1, respectively. Then the forward computation-related circuit parameters are required to be set. To be more specific, the scan voltage, scan rate, read voltage, word line voltage, and bit line voltage are set to ± 3 V, 0.05 V/s, 0.5 V, 3 V, and 1.7 V, respectively. The error back-propagation process depends on the Adam optimizer with an initial learning rate of 0.0001. And training epochs of DAE network and GRU are set to 200 and 500, respectively.

## 5.3 | Experimental results

For the purpose of evaluating the accuracy of the proposed method MDGN for SOC estimation, we conducted some comparative experiments with seven SOC estimation methods (i.e. GRU, LSTM, Standard RNN, AE-GRU, DAE-GRU, LSTM-attention, and LSTM-attention-Kalman) [11–13, 16–18].

Figure 7 shows the SOC estimation results with different methods at different ambient temperatures (0, 25, and 45°C) and different tests (Test 1, Test 2, Test 3, and Test 4), with embedded plots showing the SOC estimation errors. The validity of the proposed MDGN is confirmed by comparing the estimated SOC values (purple solid line) and the actual SOC values (grey solid line). From Figure 7, the proposed MDGN and the seven compared methods are all affected by the external ambient temperature in SOC estimation, and the impact trends are the same. At low temperature (0°C), the SOC estimation curves slightly shift the real SOC curve, whereas at high temperature (45°C), the estimated curves overlap more with the real curve.

In addition, it is difficult to distinguish the performance of these different methods from the human visual system due to the almost overlapping prediction curves. Thus, we introduced the root mean square error (RMSE) and mean absolute error (MAE) [31, 32] as SOC estimation metrics to judge the robustness and accuracy, respectively. The mathematical expressions of RMSE and MAE are described as follows:

$$\mathrm{RMSE} = \frac{1}{T}\sqrt{\sum_{t=1}^{T}(\mathrm{soc}_t - \mathrm{soc}_t')} \tag{20}$$

$$\mathrm{MAE} = \frac{1}{T}\sum_{t=1}^{T}\left|\mathrm{soc}_t - \mathrm{soc}_t'\right| \tag{21}$$

where $T$ is the total number of SOC samples contained in the test data. A lower RMSE signifies more robustness as the proposed estimation method is less affected by abnormal values. Besides the smaller value of MAE indicates the more accurate estimation performance.

Table 3 lists RMSE, MAE, training time, and test time of various SOC estimation methods in the above comparison experiments. It can be seen from Table 3 that the accuracy of SOC estimation has a strong correlation with the ambient temperature, which is especially remarkable at low ambient temperatures, as manifested by the relatively high RMSE and MAE values at 0°C. In addition, the LSTM-attention-Kalman method showed the best estimation accuracy and robust performance in all the comparison experiments for different driving conditions at an ambient temperature of 45°C. The proposed MDGN shows the best performance in terms of SOC estimation accuracy and robustness under different driving conditions at a low temperature environment of 0°C. Among these SOC estimation methods at ambient temperature (25°C) the LSTM-attention-Kalman method and the proposed method perform better, but the proposed method has a great advantage over the LSTM-attention-Kalman method in terms of training time, which is reduced by 2911.73 s. There are also LSTM-attention method and DAE-GRU method that perform well in terms of accuracy and robustness. The table also shows that all estimation methods performed best in Test 1, also known as more accurate battery SOC estimation for FUDS driving conditions. Besides, the proposed method based on the memristor hardware implementation of the neural network greatly reduces the time cost of SOC estimation, compared to other methods.

Table 4 lists the power consumption and the number of each submodule, where the Metal Oxide Semiconductor Field Effect Transistor (DAC) module is implemented to convert the data in CALCE to the specific circuit voltages. In addition, the total power consumption of the proposed MDGN circuit is listed in the last row of Table 4. Typically in integrated circuits, resistors, capacitors, transistors, and memristors are in the micron size range. The power consumption for the 1-bit calculation is 25.07 mW when the read voltage is 0.5 V and 50 ns.

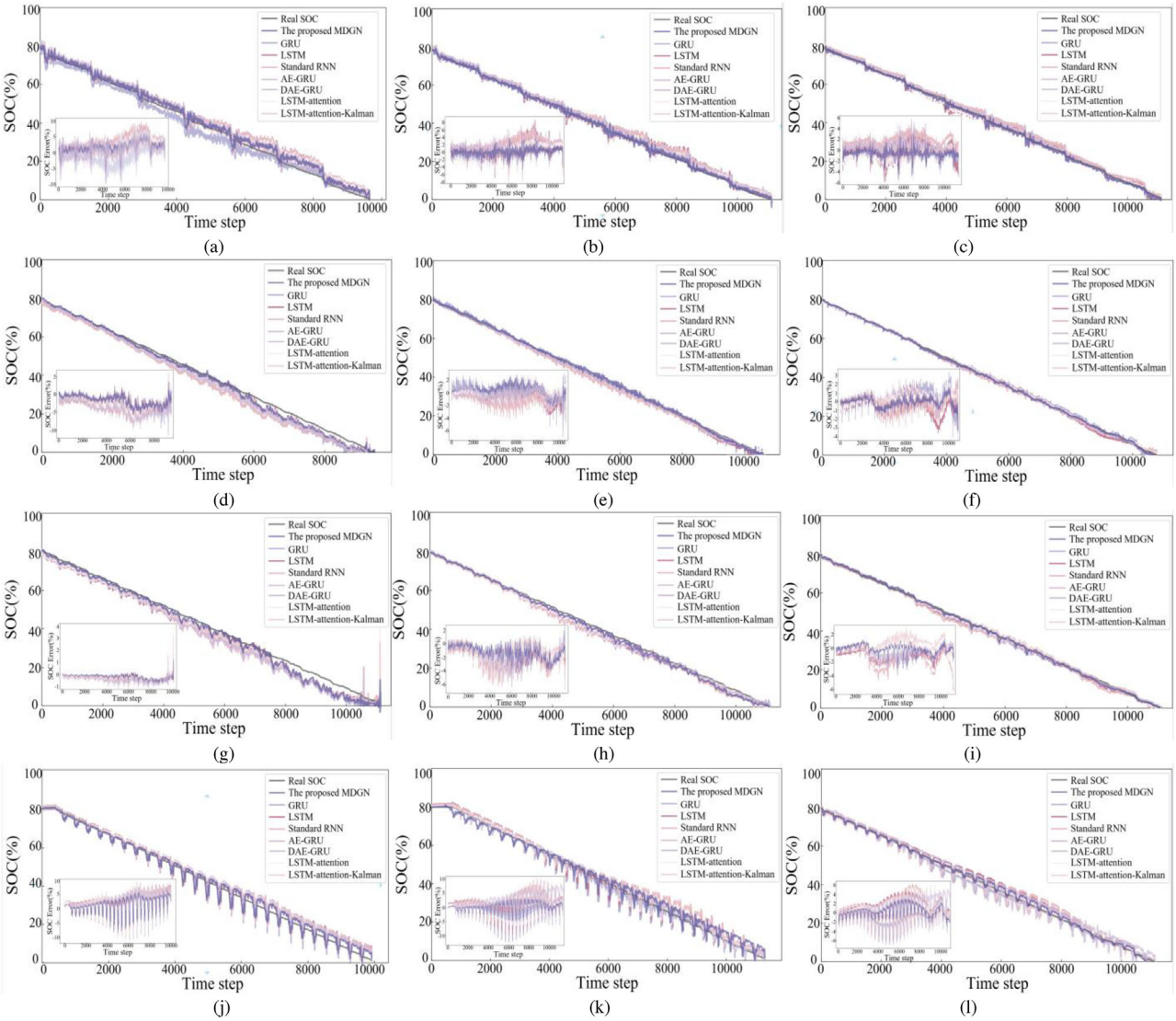


**FIGURE 7** SOC estimation results and error results under different tests at different ambient temperatures (a) to (c) results of Test 1 at 0, 25, and 45°C, (d) and (e) results of Test 2 at 0, 25, and 45°C, (g) to (i) results of Test 3 at 0, 25, and 45°C, (j) to (l) results of Test 4 at 0, 25, and 45°C. SOC, state of charge.

## 5.4 | Experimental analysis

To minimize the effects of ambient temperature and datasets (e.g. training data and test data) on the SOC estimation error, Test 2 is chosen for the following tests and conducted at 25°C.

1. SOC estimation at different training epochs

During the training process, the choice of different epochs can have an impact on the accuracy of SOC estimation. The epoch indicates the number of times the dataset is trained. Multiple training of the network can optimize the model and thus improve the prediction effectiveness, while too many training epochs increase the training time.

Table 5 collects the comparison results of RMSE, MAE, training time, and test time of our proposed method under different epochs. When the epochs of DAE and GRU are small (less than 200), the RMSE and MAE of the estimated SOC results are high and the network is not sufficiently fitted. When the number of training DAE is certain, the accuracy and robustness of the network improve with the increase of GRU epoch. While too many epochs of GRU may lead to overfitting issue, and finally degrade the estimation performance. When the epoch of GRU is certain, RMSE and MAE show a significant decrease first and then fluctuate continuously with the increase of DAE epoch. In addition, the increase of training epochs also means the increase of the training time. In these experiments, the estimation performance is optimal when the epochs of DAE and GRU are set to 200 and 500, respectively.

1. Anti-noise analysis

Considering that noise can have an effect on the accuracy of SOC estimation methods, we discuss the noise immunity of the open-circuit voltage method [6], the ampere-hour integration

**TABLE 3** Performance evaluation of different methods under different tests.

| Methods | Temp. (°C) | RMSE (%) | | | | | MAE (%) | | | | | Training time/s | Test time/s |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Test 1 | Test 2 | Test 3 | Test 4 | Avg. | Test 1 | Test 2 | Test 3 | Test 4 | Avg. | | |
| **The proposed MDGN** | 0 | 2.37 | 2.75 | 2.78 | 2.86 | 2.69 | 1.98 | 2.11 | 2.15 | 2.41 | 2.16 | 662.63 | 1.22 |
| | 25 | 0.96 | 0.94 | 1.56 | 1.38 | 1.21 | 0.73 | 0.81 | 1.29 | 1.07 | 0.98 | | |
| | 45 | 0.92 | 0.54 | 0.59 | 1.08 | 0.78 | 0.71 | 0.41 | 0.45 | 0.77 | 0.59 | | |
| GRU | 0 | 2.98 | 3.58 | 3.59 | 3.66 | 3.45 | 2.42 | 2.96 | 2.99 | 3.07 | 2.86 | 2274.49 | 1.16 |
| | 25 | 1.68 | 2.21 | 2.26 | 2.23 | 2.10 | 1.32 | 1.83 | 1.85 | 1.43 | 1.61 | | |
| | 45 | 1.30 | 0.83 | 1.12 | 1.94 | 1.30 | 1.02 | 0.66 | 0.89 | 1.46 | 1.26 | | |
| LSTM | 0 | 3.52 | 3.63 | 3.69 | 3.75 | 3.65 | 2.88 | 3.26 | 3.26 | 3.19 | 2.55 | 2732.56 | 1.28 |
| | 25 | 2.36 | 2.53 | 2.54 | 3.37 | 2.70 | 1.82 | 2.25 | 2.25 | 1.85 | 2.04 | | |
| | 45 | 1.54 | 0.95 | 1.28 | 2.17 | 1.49 | 1.21 | 0.68 | 1.11 | 1.77 | 1.19 | | |
| Standard RNN | 0 | 4.29 | 4.40 | 4.45 | 4.02 | 4.29 | 3.81 | 3.93 | 3.96 | 3.52 | 3.81 | 3003.19 | 1.53 |
| | 25 | 2.81 | 2.72 | 2.80 | 1.73 | 2.52 | 2.56 | 2.25 | 2.31 | 0.67 | 1.95 | | |
| | 45 | 2.02 | 0.97 | 1.93 | 2.56 | 1.87 | 1.85 | 0.76 | 1.46 | 1.97 | 1.51 | | |
| AE-GRU | 0 | 3.27 | 4.33 | 4.36 | 3.49 | 3.86 | 2.92 | 2.86 | 2.86 | 2.88 | 2.88 | 2535.37 | 1.66 |
| | 25 | 2.31 | 2.01 | 2.06 | 1.56 | 1.97 | 1.98 | 1.66 | 1.66 | 1.36 | 1.67 | | |
| | 45 | 1.05 | 0.74 | 0.91 | 1.18 | 0.97 | 0.81 | 0.60 | 0.70 | 0.70 | 0.71 | | |
| DAE-GRU | 0 | 2.85 | 3.86 | 4.84 | 3.36 | 3.73 | 2.48 | 3.57 | 2.35 | 2.83 | 2.68 | 2462.62 | 1.70 |
| | 25 | 1.07 | 1.54 | 1.92 | 1.32 | 1.46 | 1.31 | 0.90 | 1.65 | 1.08 | 1.24 | | |
| | 45 | 0.91 | 0.65 | 1.02 | 0.91 | 0.87 | 0.71 | 0.45 | 0.80 | 0.92 | 0.72 | | |
| LSTM-attention | 0 | 3.07 | 3.64 | 3.67 | 3.23 | 3.40 | 2.45 | 3.56 | 3.37 | 2.78 | 3.04 | 3359.13 | 1.59 |
| | 25 | 1.41 | 1.68 | 1.71 | 1.47 | 1.57 | 1.12 | 1.43 | 1.43 | 1.27 | 1.31 | | |
| | 45 | 1.33 | 0.57 | 0.99 | 1.18 | 1.02 | 1.16 | 0.44 | 0.79 | 0.85 | 0.81 | | |
| LSTM-attention-Kalman | 0 | 2.07 | 3.37 | 3.12 | 3.03 | 2.90 | 1.68 | 3.33 | 2.74 | 2.53 | 2.57 | 3574.36 | 1.73 |
| | 25 | 1.01 | 1.05 | 1.05 | 1.47 | 1.15 | 0.72 | 0.87 | 0.87 | 1.53 | 1.00 | | |
| | 45 | 0.73 | 0.44 | 0.73 | 0.97 | 0.72 | 0.53 | 0.35 | 0.57 | 0.69 | 0.54 | | |

*Note*: The time (training time and test time) is an average result of different tests at different temperatures.
AE-GRU, autoencoder-gated recurrent unit; DAE, denoising autoencoder; GRU, gated recurrent unit; LSTM, long short-term memory; MDGN, memristor-based denoising autoencoder and gated recurrent unit network; RNN, recurrent neural networks.

method [7], and the proposed method MDGN by adding noise to the input signal. Figure 8 shows the MAE results of different noise variances for these three estimation methods. It can be seen that the estimation accuracy of MDGN remains at a high level although the input is contaminated by noise. However, the estimation performance of the open-circuit voltage method and the ampere-hour integration method is severely impaired, which also confirms the good noise immunity of the proposed method in this paper.

## 6 | DISCUSSION

As the experimental results show, it is valid to build a deep neural network on hardware by memristors, and the key information in the battery measurement data (voltage, current, temperature) can be extracted and encoded as the conductance value of memristors by the DAE in the front-end of the proposed network, and subsequently the non-linear mapping relationship between the measurement data and SOC is constructed by the GRU network, which in turn enables the SOC estimation of lithium-ion batteries. Compared with the traditional data-driven approaches, this method exhibits obvious advantages in terms of energy efficiency and computational speed. Due to the nanometre size and rapid resistance switching time of the non-volatile memory device, the memristor crossbar array not only enables the in-store calculation but also has a high degree of parallelism, which greatly reduces the time cost.

Nevertheless, the proposed scheme uses software to realize the error back-propagation calculation, which requires analog-to-digital and digital-to-analog conversion modules. These modules have a large impact on the performance of the overall neural network circuit in terms of reduced accuracy and increased power consumption. In the future, we need to explore circuits for error backpropagation to achieve better performance of fully analog neural network circuits based on memristors. Furthermore, the accuracy of SOC estimation for low-temperature environment is lower compared to that for high-temperature conditions, and the proposed method is not effective in alleviating the mileage anxiety problem highlighted with the

**TABLE 4** Power consumption of the proposed MDGN.

| Module | Number | Power consumption /mW |
|---|---|---|
| DAC | 3 | 19.58 |
| Layer normalization circuit | 1 | 0.03 |
| 1T1M array | 8 | 4.85 |
| Sigmoid activation function ($\sigma$) circuit | 4 | 0.04 |
| Tangent activation function (tanh) circuit | 1 | 0.01 |
| Multiplication circuit | 3 | 0.49 |
| Subtraction circuit | 1 | 0.01 |
| Addition circuit | 6 | 0.06 |
| Total | | 25.07 |

MDGN, memristor-based denoising autoencoder and gated recurrent unit network.

**TABLE 5** SOC estimation at different training epochs.

| DAE epoch | GRU epoch | RMSE (%) | MAE (%) | Training time/s | Test time/s |
|---|---|---|---|---|---|
| 100 | 200 | 2.17 | 1.85 | 283.98 | 1.02 |
| | 500 | 1.07 | 0.90 | 567.97 | 1.19 |
| | 1000 | 1.37 | 1.17 | 1041.28 | 1.23 |
| 200 | 200 | 1.87 | 1.57 | 378.65 | 1.10 |
| | 500 | 0.94 | 0.81 | 662.63 | 1.25 |
| | 1000 | 1.22 | 1.02 | 1135.94 | 1.70 |
| 500 | 200 | 1.92 | 1.59 | 671.49 | 1.27 |
| | 500 | 1.00 | 0.84 | 946.61 | 1.66 |
| | 1000 | 1.24 | 1.03 | 1419.92 | 1.82 |

DAE, denoising autoencoder; GRU, gated recurrent unit; MAE, mean absolute error; RMSE, root mean square error; SOC, state of charge.

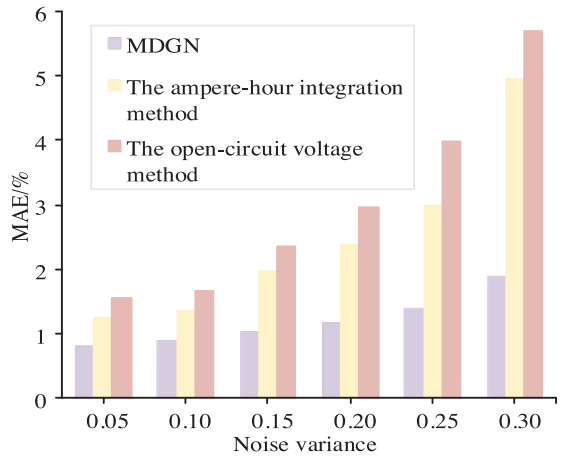


**FIGURE 8** Anti-noise analysis of the proposed method MDGN, the ampere-hour integration method, and the open-circuit voltage method. MDGN, memristor-based denoising autoencoder and gated recurrent unit network.

development of the EV field, especially for harsh environments, which is also the main obstacle to be tackled in the future.

## 7 | CONCLUSION

This paper proposes an efficient memristor-based DAE-GRU hybrid neural network circuit framework for SOC estimation. First, the mathematical and PSPICE model of the Ag/$TiO_x$ nanobelt/Ti memristor are introduced briefly. Then the circuit designs of the DAE and the GRU module are proposed based on the nanoscale memristors. Both of them are the fundamental circuit modules of the entire hybrid circuit framework (MDGN). Specifically, the circuit mainly contains the matrix vector multiplication circuit implemented by 1T1M crossbar arrays, the sigmoid and hyperbolic tangent activation function circuits, and basic operation circuits such as addition, subtraction, and multiplication. To validate the effectiveness of the circuit, we tested the proposed MDGN at different temperatures of 0, 25, and 45°C under FUDS, US06, BJDST, and DST conditions. Its SOC estimation performance was further verified by comparing it with seven advanced SOC estimation methods, and the experimental results showed that the proposed MDGN is superior in terms of both the estimation performance and computational efficiency.

## AUTHOR CONTRIBUTION

Jiayang Wang: Software, Writing-original draft. Xinghao Zhang: Software, Validation. Yifeng Han: Formal analysis, Investigation, Writing-original draft. Chun Sing Lai: Conceptualization, Writing-review and editing. Zhekang Dong: Project administration, writing-review and editing. Guojin MA: Writing-review and editing. Mingyu Gao: Formal analysis.

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## CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

## DATA AVILIBALITY STATEMENT

No

## ORCID

*Chun Sing Lai* https://orcid.org/0000-0002-4169-4438
*Zhekang Dong* https://orcid.org/0000-0003-4639-3834

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# APPENDIX

**TABLE A1** PSPICE sub-circuit description of Ag/$TiO_x$ nanobelt/Ti memristor model.

```
*Ag/TiOx nanobelt/Ti memristor model
 SUBCKT Memristor mode TE BE XSV:
 params a1=0.008 a2=−500 b1=−0.308 b2=8.15 c1=0.0066
c2=2E−8 d1=9.96E−5 d2=1.0 +Vth1=0 Vth2=0 kL=−5.66
AlphaL=1.0 aL=0.096 kH=2.9E−5 AlphaH=4.0 aH=0.041
wc=−0.047
*****Multiplication functions to ensure zero state*****
**********Function dx/dt=F(x(t), v(t))**********
 func
F(x, v, kL, kH, AlphaL, AlphaH, aL, aH, wc)=
{If(v<Vth1, f1(x, v, kL, Vth1, AlphaL, aL, wc), +If(v>Vth2, f2(x, v, kH, Vth2, AlphaH, aH, wc), 0))}
 func
f1(x, v, kL, Vth1, AlphaL, aL, wc)= kL*(v−Vth1)^AlphaL*exp(−exp((aL−x)/wc))
 func
f2(x, v, kH, Vth2, AlphaH, aH, wc)= kH*(v−Vth2)^AlphaH*exp(−exp((x−aH)/wc))
**IV Response Hyperbolic sine due to MIN structure**
 func IVRel(V)= {If(v<0,a1*x*exp(b1*x^3+1)*sinh(c1*(V−Vth1)+d1)), If(v>0, a2*x*exp(b2*x^3+1)*sinh(c2*(V−Vth2)+d2))}
********Circuit to determine state variable********
Cx XSV 0 {1}
 ic V(XSV)=x0
Gx 0 XSV
*****Current source for memristor IV response*****
Gm TE BE value = {IVRel (V (TE, BE), V (XSV, 0))}
 ENDS Ag/TiOx nanobelt/Ti memristor model
```