
# A New Configuration for Shunt Active Power Filters

A thesis submitted for the degree of Doctor of Philosophy

by

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*To my Parents*

*with love and respect*

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# A New Configuration for Shunt Active Power Filters

## Abstract

This thesis presents a new power circuit configuration to be used in shunt active power filters. A new control algorithm based on the linear voltage control suitable for the proposed circuit is introduced. The system is analysed both in time and frequency domains. The practical implementation of the system proves its suitability for the proposed task. The switching frequency of the proposed circuit is much lower than that in other active filters. The switching losses are then considerably reduced, in addition to the fact that the switching devices can withstand larger values of currents being switched on and off at lower frequencies which is an advantage to this circuit. The component sizes (capacitors and inductors) in the proposed circuit are also much smaller than those in other filter configurations.

In addition, the thesis presents a new method for categorising the active filter systems proposed in the surveyed literature. The survey includes a comparison of these techniques showing their respective merits and drawbacks. The thesis also includes an implementation of a reference current generator that is suitable for single-phase applications without the need for excessive computations. The technique involves a modified Fourier analysis, which is suitable for active filtering applications.

# List of Abbreviations

| | |
|---|---|
| AF | Active Filter |
| BIOS | Basic Input Output System |
| CSI | Current source inverter |
| DFT | Discrete Fourier transform |
| DSP | Digital Signal Processor |
| FACTS | Flexible AC transmission systems |
| FFT | Fast Fourier transform |
| HPF | High-pass filter |
| IRQ0 | PC interrupt request of level 0 |
| ISA | Industry Standard Applications |
| LPF | Low-pass filter |
| PCC | Point of Common Coupling |
| PPI | Programmable Peripheral Interface |
| PWM | Pulse width modulation |
| THD | Total Harmonic Distortion |
| VSI | Voltage source inverter |

# List of Symbols

| | |
|---|---|
| $A_i$, $B_i$ | Fourier coefficients of the analysed signal |
| $C_{dc}$ | dc-link capacitance (F) |
| $C_{dc1}$, $C_{dc2}$ | Proposed filter dc-link capacitances (F) |
| $C_f$ | Filter capacitance (F) |
| $e_c$ | Control effort |
| $E_c^{max}$ | Maximum value of control effort |
| $f_n$ | Frequency under investigation (Hz) |
| $f_p$ | Resonant frequency of the transfer function poles (Hz) |
| $f_{rl}$ | Resonance frequency of the active filter components (Hz) |
| $f_s$ | Supply frequency (Hz) |
| $f_{sw}$ | Modulation frequency of the power switches (Hz) |
| $f_z$ | Resonant frequency of the transfer function zeros (Hz) |
| $G(f_n)$ | Open loop transfer function of the system |
| $G_{AF}$ | Closed loop transfer function of the system |
| $G_{ij}$ | Transfer matrix elements of the power system analysed in the frequency domain |
| $h$ | hysterisis error band |
| $i_1$ | Fundamental component of current (Amp) |
| $I_1^{cos}$ | Fundamental cosine component of analysed current (Amp) |
| $I_1^{sin}$ | Fundamental sine component of analysed current (Amp) |
| $I_1^{total}$ | Total fundamental component of analysed current (Amp) |
| $I_{AF}^{h}$ | Active filter current at the frequency $f_h$ (Amp) |
| $i_{ch}$ | Current in the charging inductance (Amp) |
| $I_{ch}^{max}$ | Peak value of charging current (Amp) |
| $i_D$ | Overall current of the direction switches (Amp) |
| $i_{DA}$ | Current in the direction switch $S_{A1}$ (Amp) |
| $i_{DB}$ | Current in the direction switch $S_{B1}$ (Amp) |
| $i_f$ | Filter current (Amp) |
| $i_f^*$ | Filter reference current (Amp) |

| | |
|---|---|
| $I_f^{max}$ | Peak value of filter current (Amp) |
| $i_h$ | Harmonic components of current (without the fundamental) (Amp) |
| $i_{ld}$ | Nonlinear load current (Amp) |
| $I_{ld}^{h}$ | Load current at the frequency $f_h$ (Amp) |
| $i_s$ | Supply current (Amp) |
| $i_{sA}$ | Current in the main switch $S_A$ (Amp) |
| $i_{sB}$ | Current in the main switch $S_B$ (Amp) |
| $I_s^{h}$ | Supply current at the frequency $f_h$ (Amp) |
| $K$ | Open loop gain of the system |
| $K_c$ | Cascade controller gain |
| $K_f$ | feedback gain |
| $L$ | Inductance (H) |
| $L_{AF}$ | Active filter inductance (H) |
| $L_{ch}$ | Filter charging inductance (H) |
| $L_f$ | Filter inductance (H) |
| $L_s$ | Supply inductance (H) |
| $N_{current}$ | index of the current sample considered for Fourier analysis |
| $N_{max}$ | number of discrete frequencies considered in the Fourier analysis |
| $N_{points}$ | number of samples of the signal considered for Fourier analysis |
| $R_{AF}$ | Internal resistance of the active filter inductor (ohm) |
| $R_{ch}$ | Internal resistance of charging inductor (ohm) |
| $R_f$ | Internal resistance of filter inductor (ohm) |
| $R_s$ | Internal resistance of the supply (ohm) |
| $R_{SA}$, $R_{SB}$ | Resistance of $S_A$ and $S_B$ (ohm) |
| $R_{SA1}$, $R_{SB1}$ | Resistance of $S_{A1}$ and $S_{B1}$ (ohm) |
| $S_A$, $S_B$ | Main modulation switches in the proposed circuit |
| $S_{A1}$, $S_{B1}$ | Auxiliary direction switches in the proposed circuit |
| $T_{ON}$ | On-time of the switches (sec) |
| $T_{ON}^{max}$ | Maximum value of switch on-time (sec) |
| $T_p$ | modulation time period of the switches (sec) |
| $T_p$ | Period of the signal under Fourier analysis (sec) |
| $T_{r1}$ | Resonance periodic time of the active filter components (sec) |

| | |
|---|---|
| $T_s$ | Periodic time of the supply voltage (sec) |
| $V_{AF}^{\ h}$ | Active filter output voltage at the frequency $f_h$ (Volt) |
| $v_C$ | Voltage across the filter capacitor (Volt) |
| $v_{ch}$ | Voltage across the charging inductor (Volt) |
| $V_{dc}$ | dc-link voltage (Volt) |
| $V_{dc1}$, $V_{dc2}$ | Proposed filter dc-link voltages (Volt) |
| $v_f$ | Filter voltage on the other side of the filter inductor (Volt) |
| $v_L$ | Voltage across the filter inductor (Volt) |
| $V_{ld}^{\ h}$ | Point of common coupling voltage at the frequency $f_h$ (Volt) |
| $V_{peak}^{\ Computed}$ | Peak voltage from the oscilloscope for current waveforms (Volt) |
| $v_s$ | Supply voltage (Volt) |
| $V_C^{\max}$ | Peak value of the filter capacitor voltage (Volt) |
| $V_s^{\max}$ | Peak value of the supply voltage (Volt) |
| $V_s^{\ h}$ | Supply voltage at a frequency $f_h$ (Volt) |
| $x(t)$ | Continuous time-domain waveform considered for Fourier Analysis |
| $x(k\tau)$ | Discrete time-domain waveform considered for Fourier Analysis |
| $Z_{AF}^{\ h}$ | Active filter impedance at the frequency $f_h$ (ohm) |
| $Z_s^{\ h}$ | Supply impedance at the frequency $f_h$ (ohm) |

# List of Greek Symbols

| | |
|---|---|
| $\Delta V_C^{drop}$ | Voltage drop due to discharging of $V_C$ in the filter circuit (Volts) |
| $\Delta V_C^{tot}$ | Voltage rise due to charging of $V_C$ from the charging inductor (Volts) |
| $\omega_h$ | Angular frequency for the harmonic under consideration (rad/sec) |
| $\omega_{r1}$ | Resonance angular frequency of the active filter components (rad/sec) |
| $\omega_p$ | Resonant angular frequency of the transfer function poles (rad/sec) |
| $\omega_z$ | Resonant angular frequency of the transfer function zeros (rad/sec) |
| $\xi_p$ | Damping ratio of the transfer function poles |
| $\xi_z$ | Damping ratio of the transfer function zeros |
| $\tau$ | Incremental time step of sampled signals used in Fourier analysis (sec) |

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# Chapter 1

# Introduction

# Chapter 1

# Introduction

## 1.1 Problem Overview

In recent years, there has been a considerable increase in the occurrence of non-linear loads in power systems. This is due to the tremendous growth in power electronic technology and the associated use of power semiconductor switching devices such as thyristors, GTOs as well as transistors of various types (BJT, MOSFET, IGBT, etc). Small distributed loads, such as computer loads and TV sets with switched-mode power supplies at their inputs, add up to a large increase in the amount of harmonic current injection in power distribution systems. On a larger scale, the large power rectifying loads, such as motor drives, arc welding and arc furnaces are considered to be large sources of harmonics in the medium voltage network. These, when added up to the reflected low voltage harmonics, cause problems to the continuity of power flow due to their harmful effects of increasing power losses in the system, resulting in oversized power devices and feeder derating. Harmonics also contribute, as one of the main reasons, in transformer saturation, mains-voltage flickering, audible noise in power system components, electromagnetic interference, shorter life of organic insulation, incorrect operation of voltage sensitive devices and above all the malfunction of protective relaying systems. All these problems have led to the ever increasing concern about how to eliminate or at least reduce the undesirable effects of harmonic pollution in power systems [1-4]. Hence, emerges the idea of harmonic filtration techniques which first started with passive filters.

The basic principle behind methods of controlling harmonics, at first, was to provide a low impedance path to ground for the higher harmonics [1]. Two main configurations are available, namely shunt and series passive circuits. In these configurations, tuned LC sub-circuits are used to divert the harmonic currents to ground in the shunt configuration; while providing a very high impedance path for these currents in series configurations, hence decreasing their magnitudes. Such filters are relatively easy to design, cheap and reliable. Other filter sub-circuits could be tuned to eliminate different other harmonic currents. However, this implies increasing the number of components used at a given site, which is considered as a major drawback as most of the filter size and cost lies in the capacitor banks. Also, the system impedance, which is normally difficult to measure, affects the component magnitudes. The installation of such devices has led to a very important consequence. They act as though they were reactive power compensators for improving the power factor of the system. On the other hand, their effectiveness depends upon the network characteristic impedance and is greatly affected by the nature of harmonic pollution of the network, ageing of filter capacitors and the changes in distorting-load operating conditions. In addition, voltage and current amplification phenomena due to parallel or series resonance may also occur for certain harmonics [1,3]. These drawbacks forced researchers to look for other solutions.

Many specialists approach the problem from the point of view of preventing the generation of harmonics, simply by making use of high input power factor and low current ripple switching power regulators and converters [5-8]. These include ac/dc converters with high pulse numbers. Others face the problem by the installation of dc-side filters for harmonic reduction on both sides of large power converters [9,10].

Such systems have to be included into the design of nonlinear loads and can not be used as a 'retrofit' to cancel harmonics generated by existing nonlinear loads.

Other approaches are required to alleviate the cumulative effects of small distributed-loads. This is simply the case for "**Active Power Filters**" which is the subject of this thesis.

## 1.2 Layout of this thesis

This thesis is divided into five chapters. This chapter is a mere introduction to the problem of harmonics in the power system. In addition, it provides the first basic attempts proposed in the literature regarding the elimination of their corresponding problems using passive compensation techniques.

The second chapter further elaborates earlier techniques used for harmonic compensation and power system conditioning using active filtering techniques. It also introduces a new method for classifying power system conditioners. The main purpose of this chapter is to introduce the reader to the main advantages and drawbacks accompanying each of the presented techniques. It also helps to clarify the main directions of the current research trends in this field.

Chapter 3 follows with the discussion of the problems accompanying the current trends in active filtering techniques. These problems are developed in order to identify the main requirements of the proposed active filter circuits needed to accomplish the job as well as avoiding the problems of the available techniques. The basic theoretical analysis and ideas of the proposed system are presented, leading to

the new power circuit proposed in this research. The modelling equations of the circuit are presented in the different modes of operation, which identify the main performance requirements of the system. This is followed by an approximate circuit component value determination that acts as a set of main guidelines in tailoring the circuit for a specific application.

The frequency response analysis of the system is also presented in chapter 3 with the reference made to the switching power amplifier circuit. The resulting control model can then be used for characterising the circuit closed loop controller necessary for the system operation. The frequency response analysis of the active filter in the power system is then presented in order to prove the viability of the closed loop voltage tracking control law suggested earlier in the same chapter. The simulation results of the proposed active filter system in the time domain are finally presented.

The overall system implementation under closed loop conditions is discussed in chapter 4. The implementation of each of the active filter blocks is presented. This includes the implementation of the mathematical and the software techniques necessary to generate an accurate and fast estimated harmonic current signal for the purpose of reference generation. The global system controller and the PWM techniques implemented are also discussed. Finally the practical results from the active filter implementation are presented and analysed.

The thesis concludes with the fifth chapter, which discusses the outcome of the theoretical and practical results of the proposed system. Chapter 5 also includes the proposed future work.

# Chapter 2

# A Survey of Active Power Line Conditioning Methodologies

# Chapter 2

# A Survey of Active Power Line Conditioning Methodologies

## 2.1 Introduction

The survey of published papers on active filtering techniques shows a great deal of interest in the past few years. Many references in the surveyed literature have discussed the evolution of active filtering techniques over many years [3,4,11,12]. The interest in the subject focuses on power circuit configurations with their possible interconnections. Some of these references review the control technique associated with some of the available methods. This chapter classifies the available filtering techniques according to their suitability for harmonic elimination, reactive power compensation as well as balancing of mains voltages and currents. It also presents a brief discussion of the merits and drawbacks of each method; leading to the provision of the main guidelines for choosing the appropriate filtering technique for a given application. The chapter highlights the problems associated with each technique, which will be used in the following chapter.

## 2.2 Classification of Active Power Filters

A large number of active power filter circuit configurations and compensation methods have been proposed in the literature to enable the compensation of harmonics in power systems. To classify these techniques for the purpose of clarifying the strengths and weaknesses of each technique, it is desirable first to distinguish the overall active filtering process into its main building blocks.

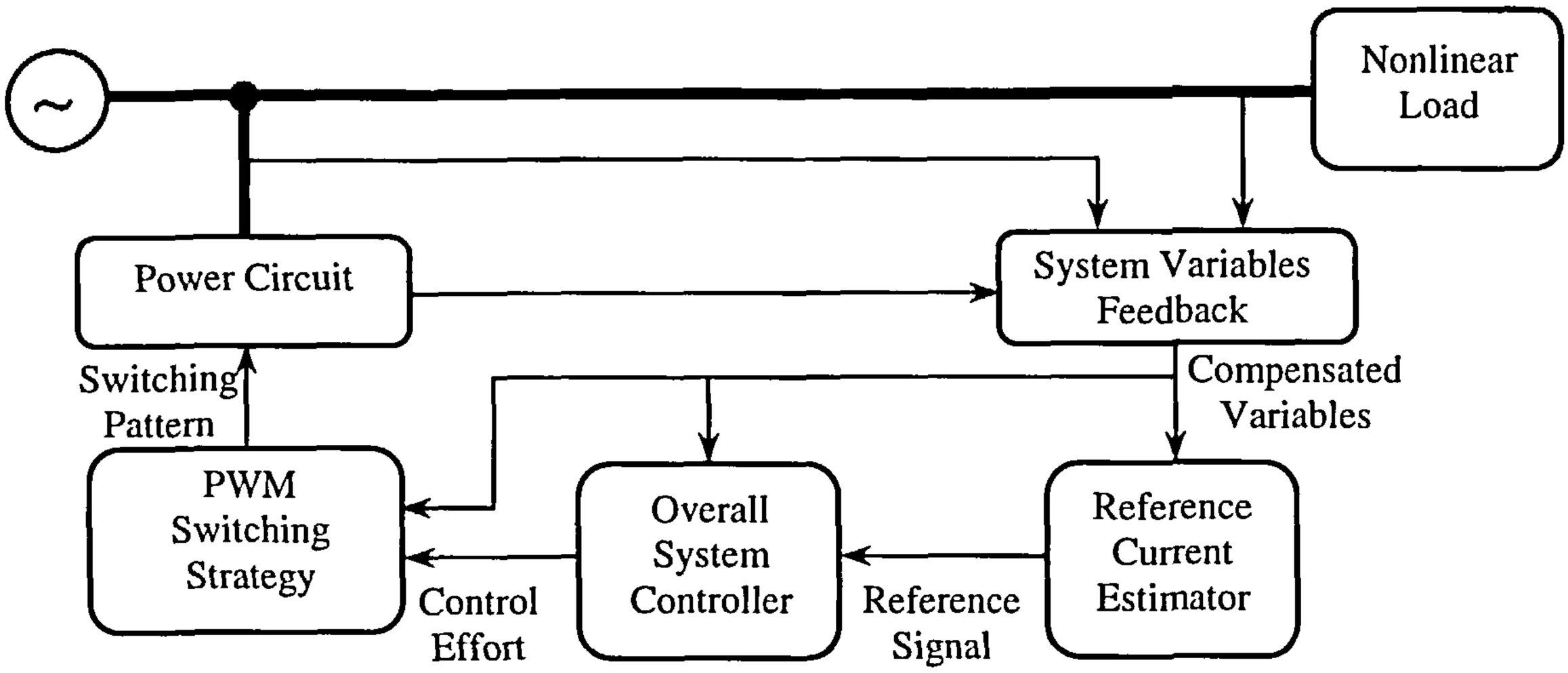



Fig.2.1 : Generalised Block Diagram for Shunt Active Filters

A typical active filter configuration can be represented by the generalised block diagram shown in Fig.2.1. The block diagram shows five main sections constituting the power active filter structure. The harmonic current generated by the nonlinear load is detected and fed back to the reference current estimator, in conjunction with the other system variables. The resulting reference signal drives the overall system controller, which, in turn, generates the control effort necessary for the PWM switching strategy to generate the switching pattern for the filter switches. The resulting filter current is also detected and fed back to the controller.

Based on this diagram, it is convenient to classify the published literature according to the following criteria depending on the technique used to perform each task. The subdivision follows according to:

1. The rating of the compensated system and its dynamic response.
2. The power circuit configurations.
3. The compensated variables (power factor, harmonics, three-phase unbalance, ...).
4. The control technique.

5. The reference current estimation technique.

The following sections will demonstrate the subdivisions according to each of the above criteria. This will provide a better understanding in dealing with these systems, as it shows the merits and drawbacks of each type.

## 2.3 Classification according to the power rating of the compensated system and its dynamic response

The rating of the compensated system and its dynamic response play a major role in deciding the control philosophy to implement the required filter. These two factors follow a reciprocal relationship [13-15]. The cost of such compensating systems is normally proportional to their dynamic response and the maximum rating of the compensator [13]. The block diagram shown in Fig.2.2 identifies the main subdivisions of power system conditioners according to the power rating of the compensated system.

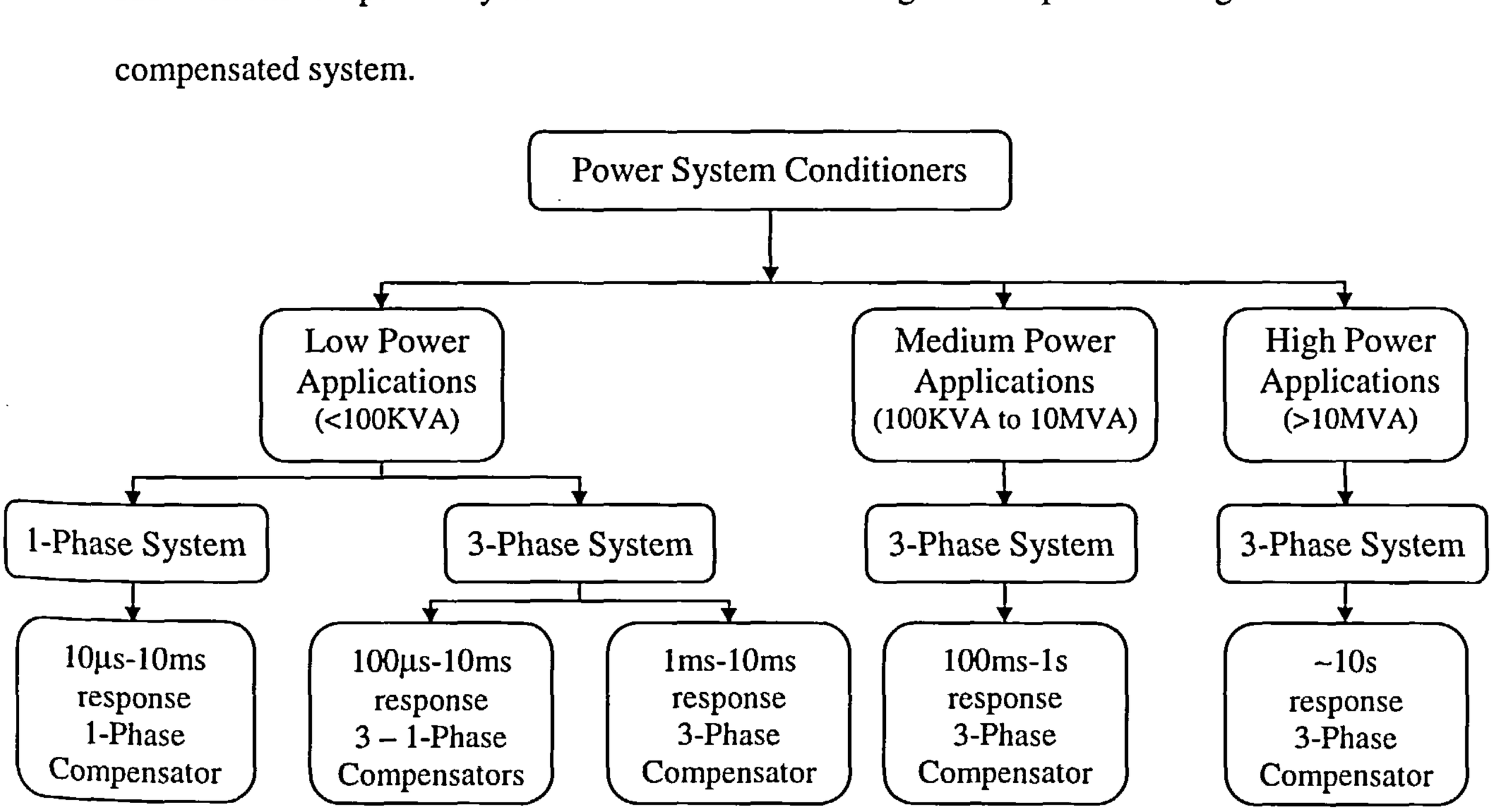



Fig.2.2 : Subdivision of power system conditioners according to power rating and dynamic response

### 2.3.1 Low power applications

This type of application is mainly concerned with power ratings below 100 KVA, which is the case for most residential areas and for a wide range of small to medium factory loads and motor drive systems. This range of applications employs sophisticated techniques of dynamic active filters especially those with high pulse-number PWM controlled voltage or current source inverters. Their response time is relatively much faster compared to the other techniques. It ranges from tens of microseconds to milliseconds. This results in the considerable reduction in their power compensation range as stated. This type comprises the following two categories:

**Single-phase systems**

The type of active filters used in single-phase systems [16-31] is not suitable for residential areas except for those cases where the quality of the input waveform is of great importance. This is due to the fact that the maximum rating of single-phase systems is normally limited to a few kilowatts, which implies that the harmonic currents generated are very small and are "unfortunately" ignored. The problem would only arise at the three-phase distribution panels, where the harmonic currents add up to large values. This case will be treated in the following subsection.

Single-phase filters have to deal with low powers and hence their switching frequencies can be easily increased leading to a better performance. Several of these retrofit filters can be installed on the site under consideration at various locations and hence they reduce the necessity for large, high power bulk filters.

**Three phase systems**

At this relatively low power level (100KVA), the three-phase system can accommodate the presence of either three single-phase compensators or one three-phase compensator. The former type is necessary for use in distribution systems where the currents and voltages in the three phases are not balanced and sometimes unsymmetrical. It can therefore incorporate three independent current feedback signals that would balance the supply currents or voltages. These are recommended by many designers for filter configurations [32], especially those who do not rely upon a standard inverter configurations such as the lattice structures and the switched capacitor techniques [23-31].

The three-phase compensator type is mainly concerned with three-phase systems, where balancing the mains currents or voltages is not critical and the concern is only towards the symmetrical harmonics in all three phases. These systems rely on the standard inverter configuration to achieve the required switching function, which results in eliminating harmonics in systems under consideration [3,4,11-15,33-51]. These systems will be further discussed in the following sections.

### 2.3.2 Medium power applications

The type of applications addressed in this category lies mainly within three-phase systems ranging from 100 KVA to 10 MVA [3,52]. Such applications can best be represented by the case of medium and high voltage distribution systems where the effect of phase unbalance is quite negligible [1], as well as the case of high power, high voltage drive systems [3], where the only concern is the harmonic current elimination. The question of reactive power compensation can no longer be

addressed solely by dynamic power filters discussed in the low power applications section. The implementation would then have pronounced negative effects on the resulting expensive and oversized system [14]. Other techniques are considered more appropriate in this case, including capacitive and inductive static power compensators as well as the quasi-dynamic compensators, such as the category of relay controlled reactive components (switched L-C circuits), tuneable harmonic filters, line commutated thyristor controlled reactive sources [53] and synchronous condensers [1]. The necessary system response time for such cases is in the range spanning from tens of milliseconds to seconds.

### 2.3.3 High power applications

The implementation of very high power dynamic filters is extremely cost ineffective; as the lack of high switching frequency power devices, that can control the current flow at such power ratings, is a major limitation for such systems [3,14]. However, the harmonic pollution in high-power ranges, which include systems of ratings above 10 MVA, is not a major problem, as in the case for lower-power systems. These high power systems include power transmission grids and ultra-high power dc-drives as well as dc transmission systems. The effect of harmonics generated at the low-power side would be minimised, either naturally or by the installation of several medium and low power active filters downstream to contribute to the compensation of such cases. The static VAR compensation is then the major concern and is usually compensated for using traditional static power conditioners as well as several sets of synchronous condensers connected in parallel. The required response time for such cases is in the range of tens of seconds which is quite reasonable for contactors and circuit breakers to operate after taking the optimal switching decision [1,14].

One of the few applications of active filters in high power systems is the Japanese bullet train (Sinkansen) [3,54], which uses a parallel combinations of several active filters. The control and coordination of these filters are however complicated [3].

## 2.4 Classification according to the power circuit configuration

The power circuit configuration plays a great role in the selection of the compensated variable as some circuits are only valid for certain cases of controlled variables and power ranges as discussed in this section and demonstrated in the block diagram shown in Fig.2.3.

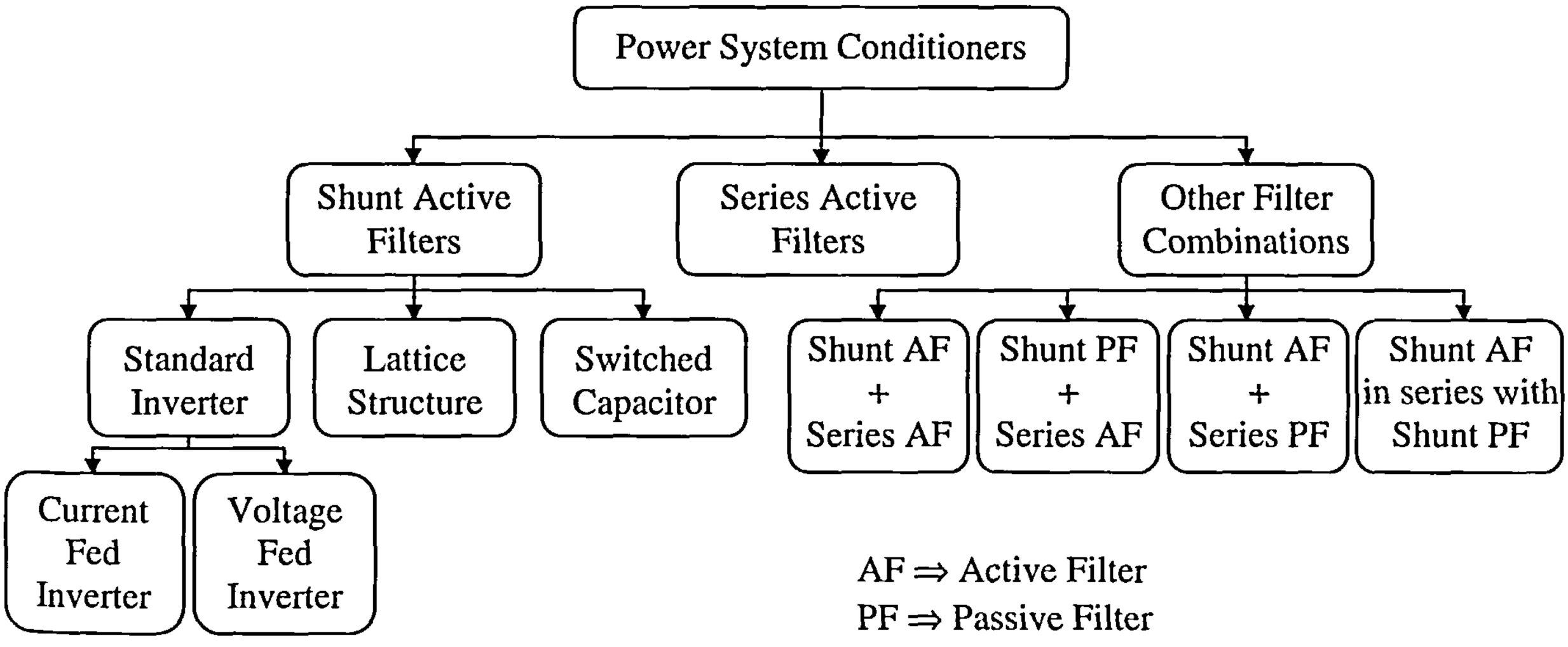



Fig.2.3 : Subdivision of power system conditioners according to power circuit configurations

### 2.4.1 Shunt active filters

This type of filter configuration constitutes the most important and most widely used type of filters that can easily be applied in industrial processes [3]. It is connected to

the main power circuit as shown in the single-line diagram of Fig.2.4. It is mainly aimed towards cancelling the load current harmonic as it has the ability of controlling the amount of current flowing in the circuit. It can also contribute to reactive power compensation and balancing of three-phase currents as mentioned earlier. This configuration has the advantage of only carrying the compensation current while a small amount of active fundamental current circulates in order to compensate for system losses. It is also possible to connect several filters in parallel to share higher values of compensation currents, which makes this type of hardware circuit suitable for a wide range of power ratings. This configuration comprises three distinct categories of circuits, namely inverter configurations, switched capacitor techniques and lattice structured filters. These are discussed below in further details.

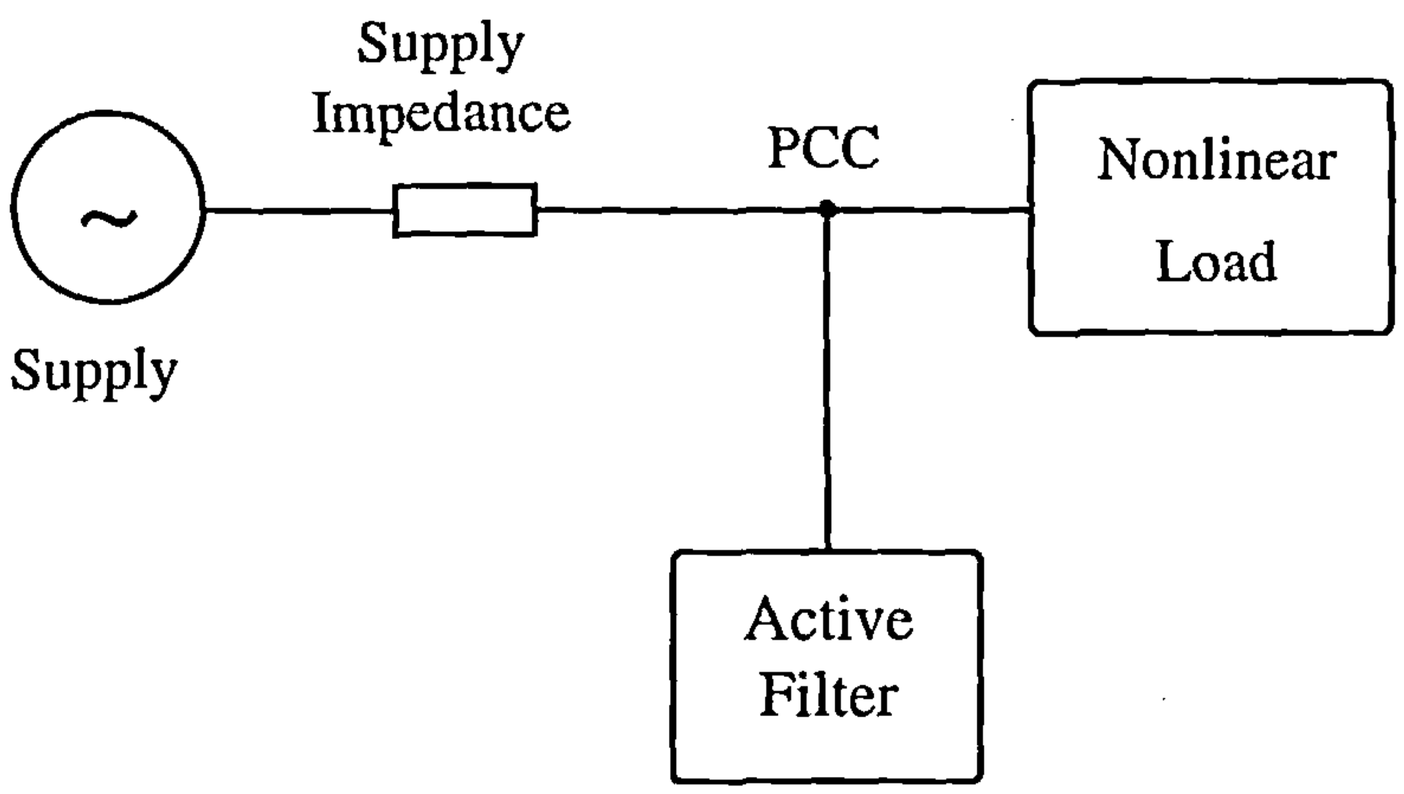



Fig.2.4 : Shunt active filter configuration

### 2.4.1.1 Standard inverter configuration for active filters

The use of an inverter in the power circuit has emerged from the fact that it is an already existing product serving in others fields. The technology of inversion techniques is well established for drive system applications; henceforth filtering

systems can make use of it. Two main circuit configurations emerge, namely, current and voltage fed inverters.

## Active filters based on current fed inverters with inductor on the dc-side

This type of filters [4,14,21,33-36,46,49,50] injects predefined current harmonics at the point of common coupling (PCC), which eliminate the current harmonics generated by the nonlinear load as shown in Fig.2.5. This configuration is not common in low power applications due to the complexity of the control strategy needed and the sensitivity of the inverter circuit to current variations in the dc-link inductor [4]. This configuration, especially when using several ones in parallel, is mainly adequate for the case of medium power applications that matches the main requirement of lower switching frequencies and high power ratings of GTOs [3,4].

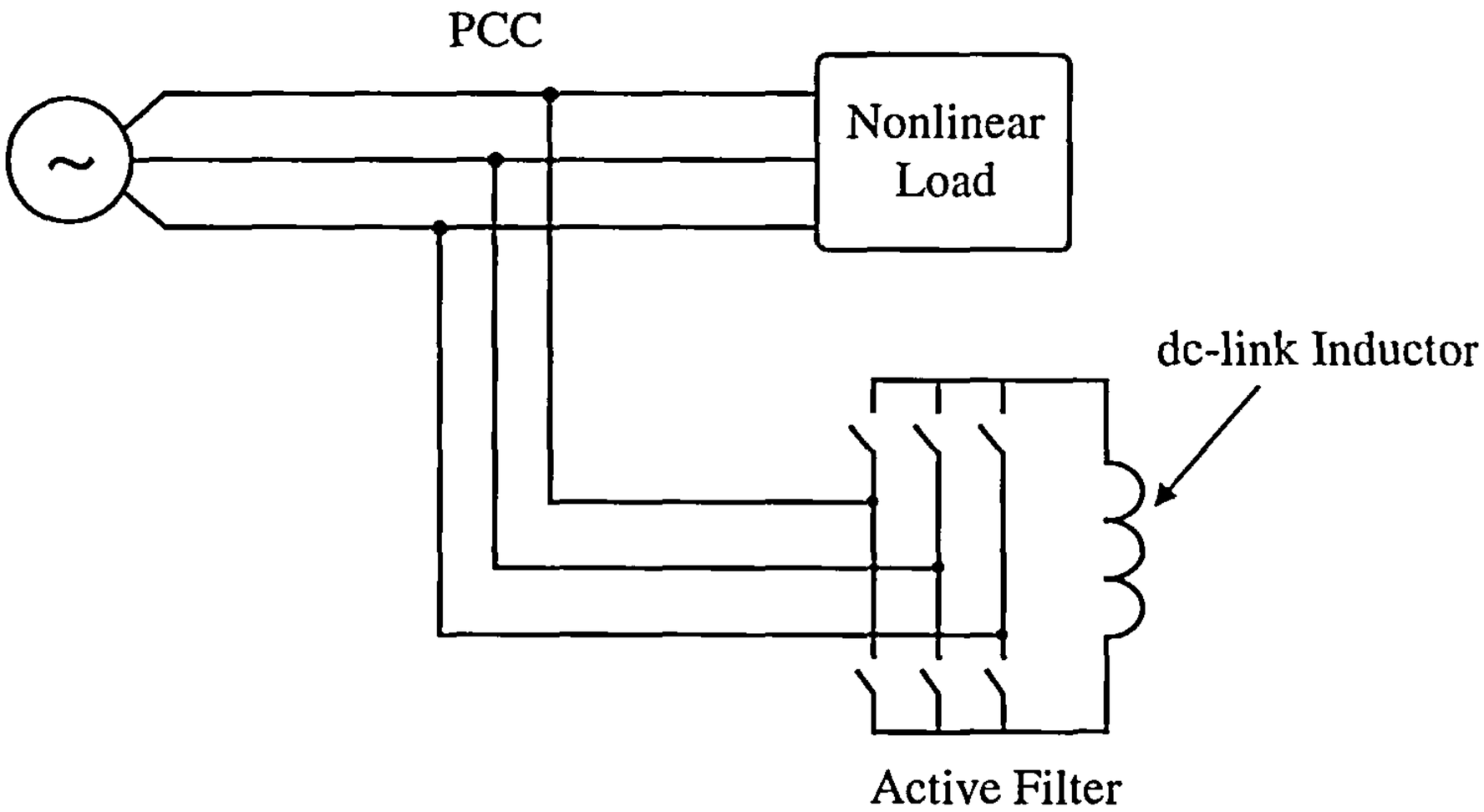



Fig.2.5 : Active filter based on current-fed inverter

## Active filters based on voltage fed inverters with capacitor on the dc-side

The compensated variable in this configuration still remains to be the current, which normally requires a current fed inverter as outlined above. However, by the

alternative use of fast switching power devices, a voltage fed inverter with a superimposed current control loop can fulfil the task [48,55-58], as shown in Fig.2.6. This circuit is common in most shunt active filters using the current controlled voltage fed inverter techniques either for three-phase [12,37,44,45,47,51,52] or single-phase [15-19] configurations. Other configurations such as the neutral point clamped inverters [59] are in use in order to produce multi-level output waveforms.

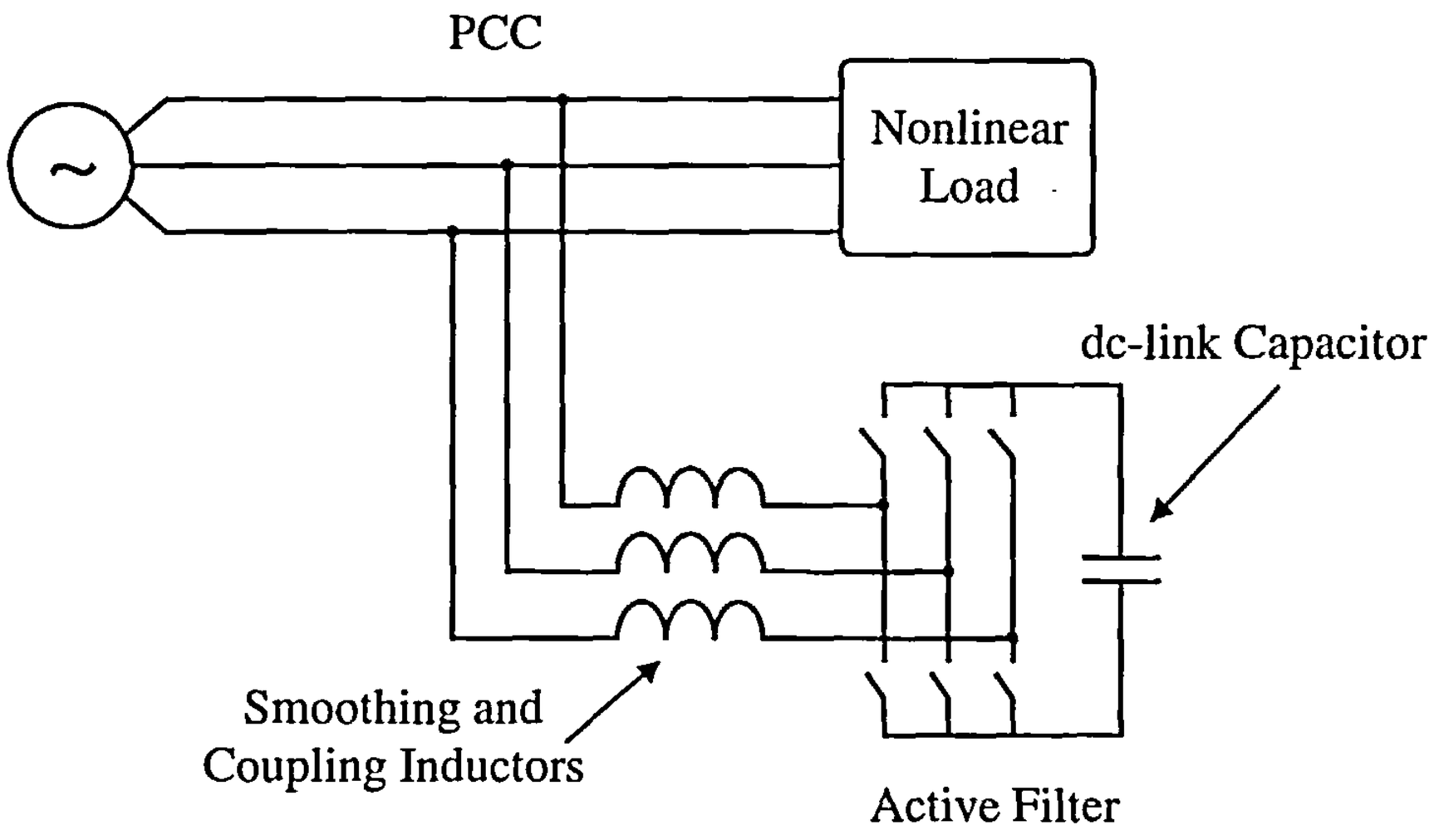



Fig.2.6 : Active filter based on voltage fed inverter

The main advantages of the current-controlled voltage-fed inverter type are the relatively simple control strategy needed for PWM waveshaping and the standard availability of the inverter for power ratings that can cover the low and medium power application regions of active filters. However, the switching frequency of such systems is considered to be relatively high and sometimes irregular due to the use of hysterisis control techniques [3,11,48].

### 2.4.1.2 Switched-capacitor filter configurations

These configurations, which were developed by the power electronics group at Brunel University [23-26,29-31], constitute a revolution in switching techniques and power circuits for active power filter applications. The different configurations, shown in Fig.2.7, were developed and tested as presented in the literature [23,24,29]. It basically consists of one or two capacitors of relatively small values as compared to the dc-link capacitor of inverter configurations, in addition to several bi-directional semiconductor switches and a very low value of current smoothing and limiting inductance. The main characteristic of this filter is its simplicity in the power circuit. However, the control algorithm is more complicated compared to inverter based filter configurations [29]. The other important point to note regarding this type of filters is that it is only applicable to single-phase systems or three-phase configurations with three single-phase compensators.

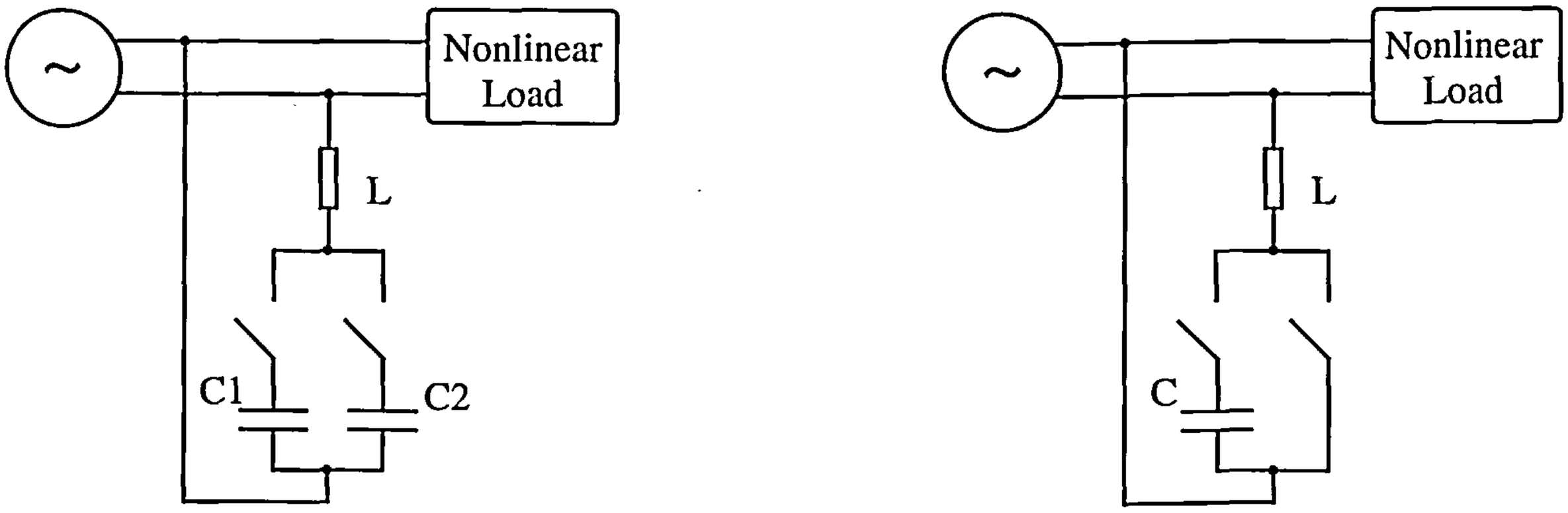



Fig.2.7 : Switched capacitor filter

### 2.4.1.3 Lattice-structure filters

Recently the power electronics group at Brunel University has also developed this new type of active filters based on the lattice structure of the filter configurations as

shown in Fig.2.8 [27-29]. It has several properties among which the simplicity of power circuit implementation. The control of these circuits is again rather difficult, as will be explained later on in this chapter. It depends on optimisation processes, which are normally time-consuming. The possible power circuit structures are thoroughly discussed in [29]. These filters, as for the previous one, are only used for single-phase systems or three single-phase compensators used in three-phase systems. The other point to consider is that these circuits depend in their operation on the resonance phenomena between the inductors and the capacitors, which is not desirable in power system applications.

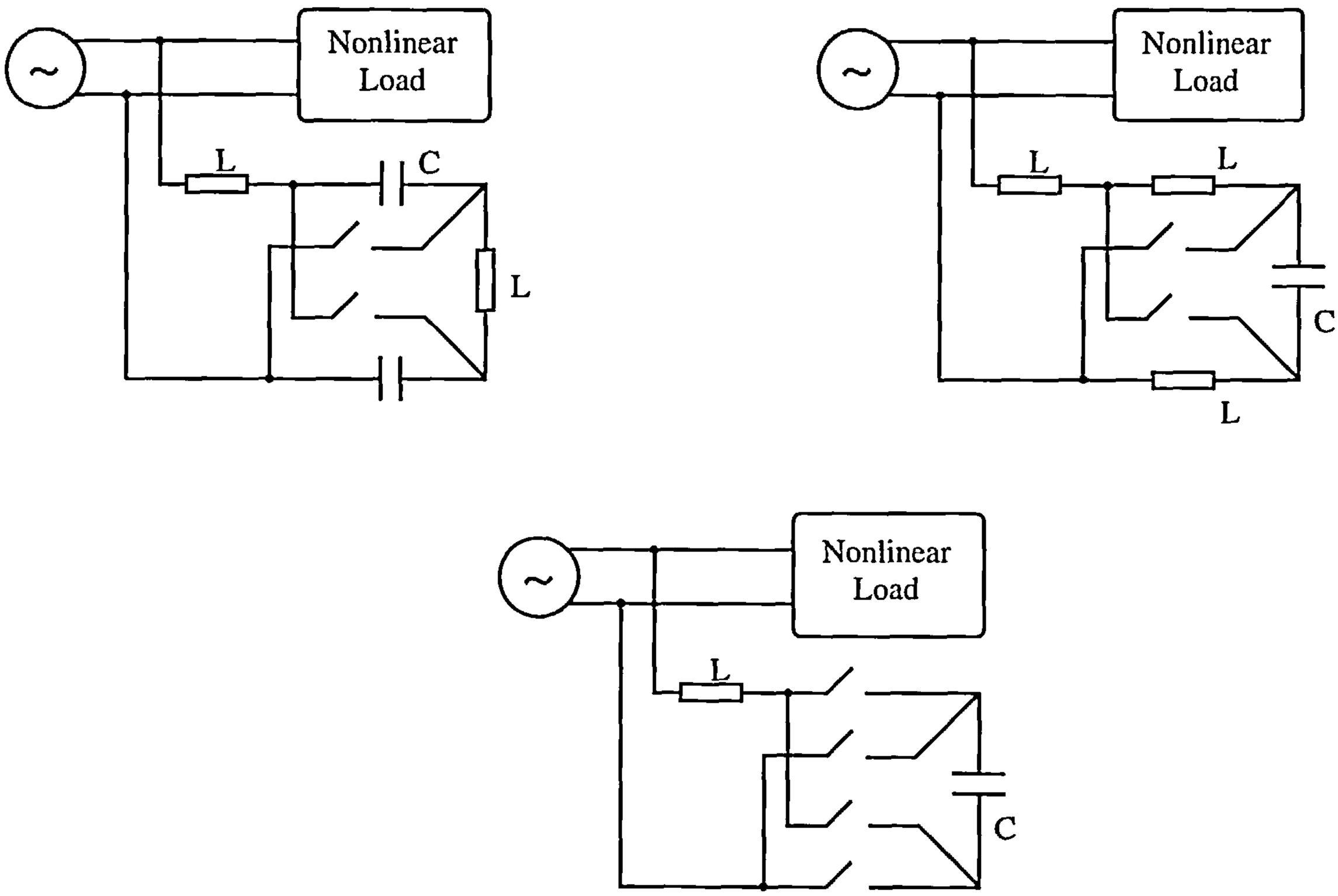



Fig.2.8 : Lattice structure configuration

### 2.4.2 Series active filters

The filter in this configuration produces a PWM voltage waveform, which is to be added/subtracted, on an instantaneous basis, to/from the supply voltage in order to apply a pure sinusoidal voltage waveform to the load [3,32]. The main power circuit configuration is shown by the single-line diagram of Fig.2.9. The inverter configuration accompanying such a system is of the voltage fed inverter type without any current control loops. These series active filters are less common industrially than their rivals, the shunt active filters. This is because of the main drawback of series filters. Due to their position in the circuit, they have to withstand high values of

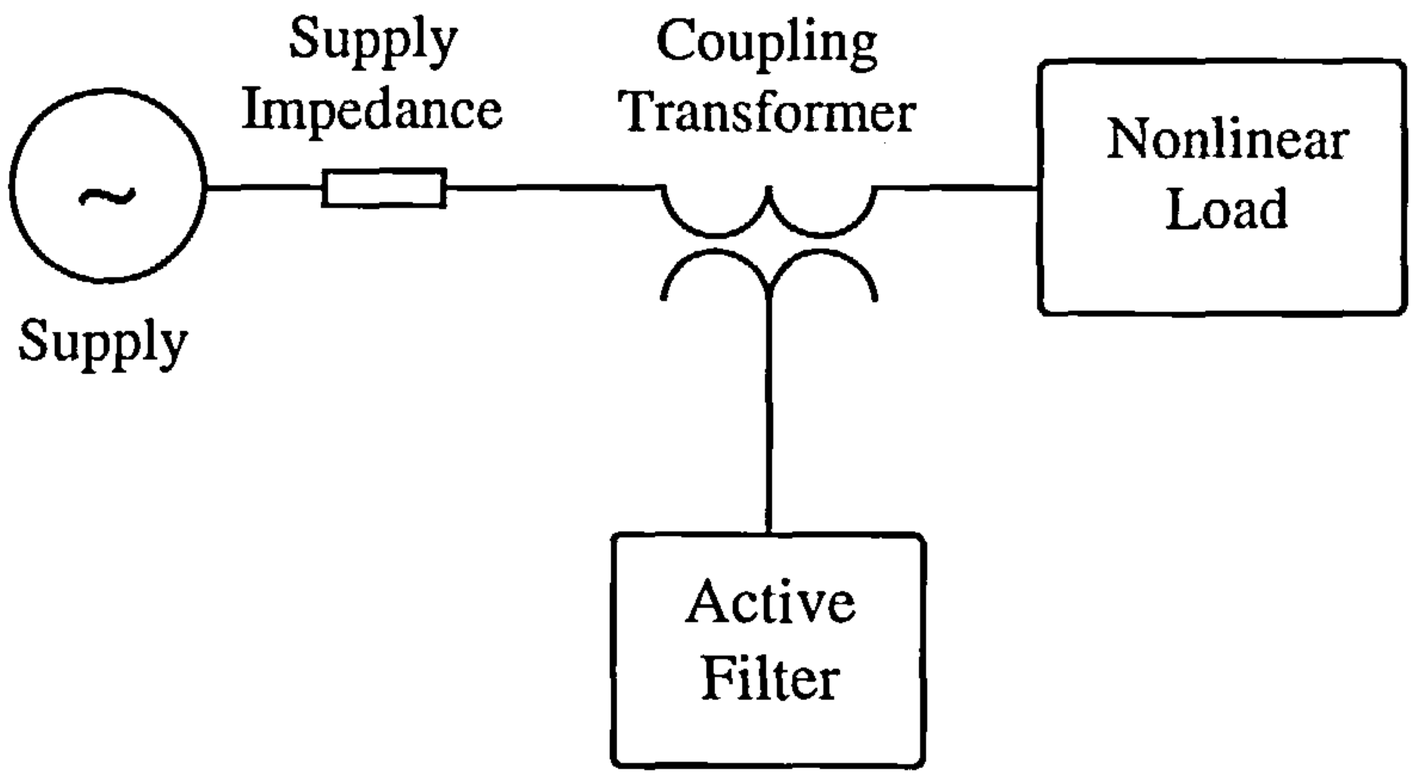



Fig.2.9 : Series active filter configuration

rated load current, which increases their current rating considerably; especially the secondary side of the coupling transformer (increasing the copper losses and the physical size of the filter). Series filters have a main advantage over shunt ones in that they can be used much easier to eliminate voltage waveform harmonics, and to balance three phase voltages [20,22,38-40]. This in fact means that this category of filters is mainly dedicated to the benefit of loads. It provides the load with a pure sinusoidal waveform that is very important from the point of view of voltage sensitive devices. It is worthwhile to note that most of the circuit configurations of the shunt

active filters can be reused in this case; however only the inverter configuration was reported in the literature.

### 2.4.3 Filter Combinations

Some combinations of several types of filters can achieve more benefits to the filtering operation. These are namely:-

**Combination of both shunt and series active filters**

In order to gain the advantages of both series and parallel inverter type configurations, a combination of both types of filters, shown in Fig.2.10, can be controlled in order to reach the ultimate target of performing all sorts of power system conditioning. Of course the load needing such complexities are rare and consequently these types of filters were given much less attention than all the other configurations [3,60,61]. The configuration is however used extensively for other purposes in power system FACTS [62]. The only difference is the control algorithm applied to the controller of the PWM switching strategy.

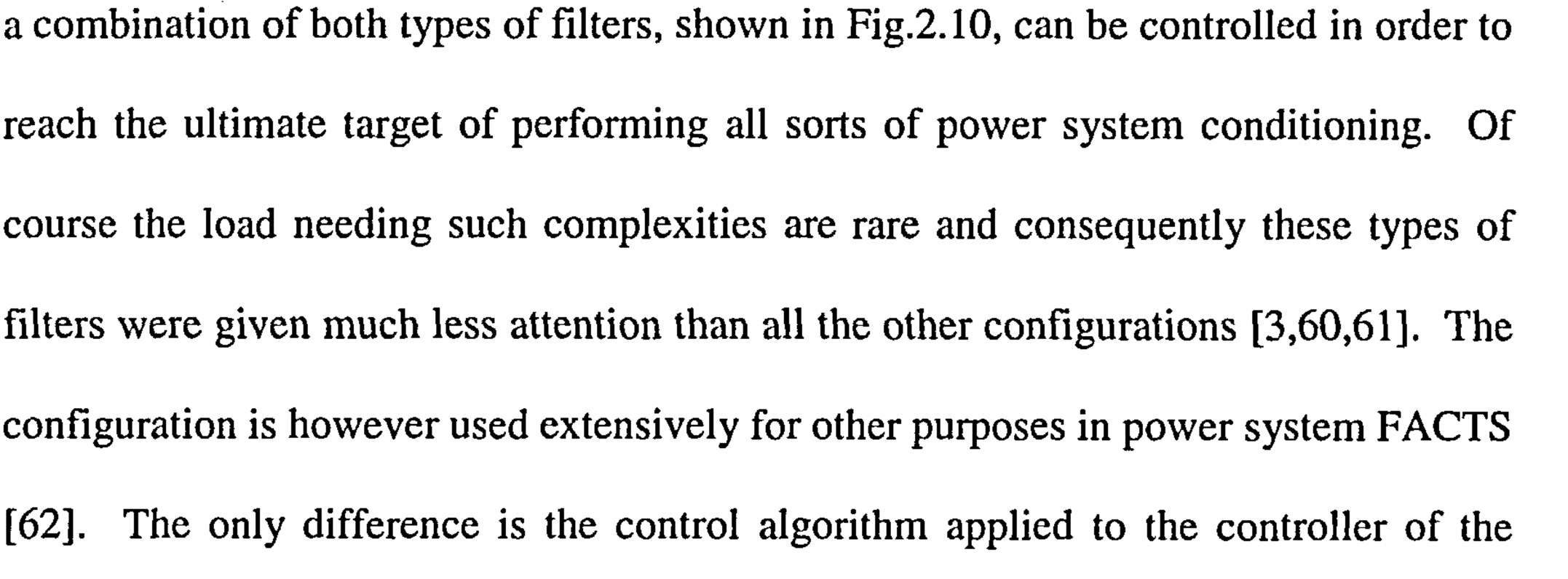



Fig.2.10 : Shunt/Series active filter configuration

## Combination of series active and shunt passive filters

To reduce the complexity of the last type of filters, the inverter type series active filter, which constitutes a high impedance for the high frequency harmonics, is accompanied by a shunt passive filter to provide the path for the harmonics currents of the load [41,61]. This combination, represented by the single line diagram of Fig.2.11, enables the improvement of the characteristics of plain series active filters and the extension of their capabilities to include current harmonic reduction as well as voltage harmonic elimination [41,61]. The configuration, however appealing, is not yet thoroughly studied due to the lack of interest in series active filters.

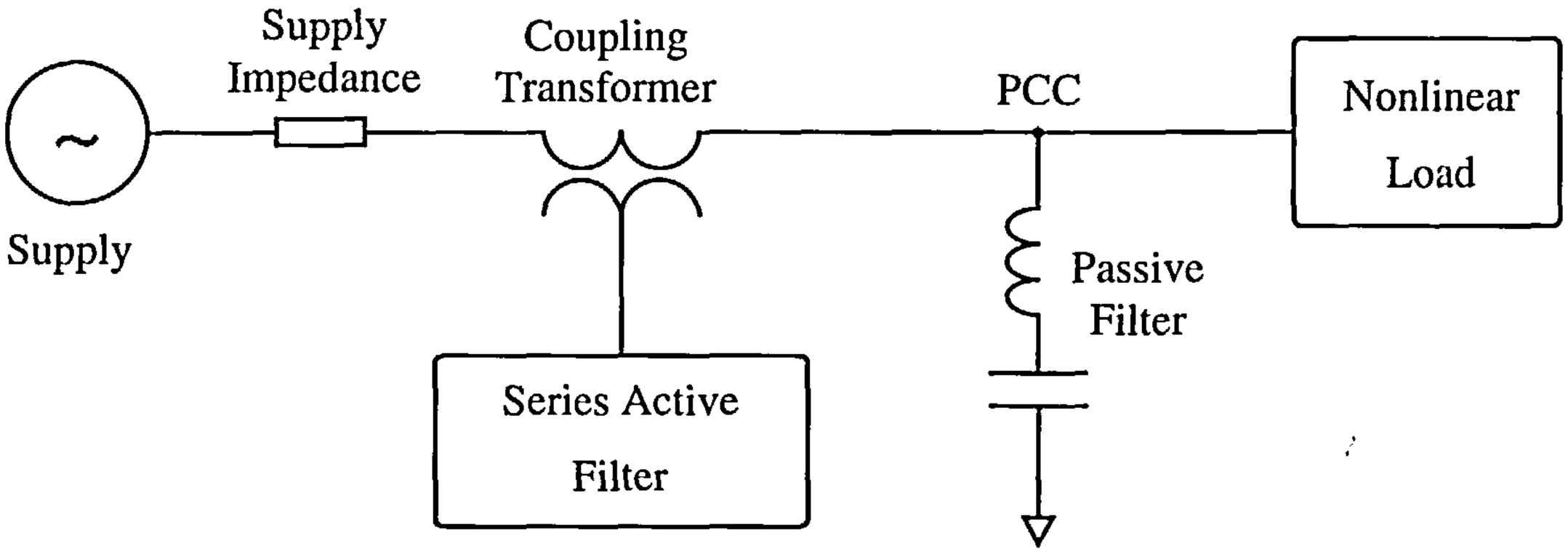



Fig.2.11 : Series active and shunt passive filter combination

## Combination of shunt active and shunt passive filters

This combination, shown by the single line diagram of Fig.2.12, constitutes one very important mixture of the passive and active inverter type filters. It relieves the active filter from some of the initial high value harmonics and hence the filter is operating on a basis of lower current value, which implies less losses and higher efficiency [42,61]. The main drawback for this technique is that it contains too many power

components especially for the static filter, which is a great disadvantage from the point of view of size and initial cost of the filter.

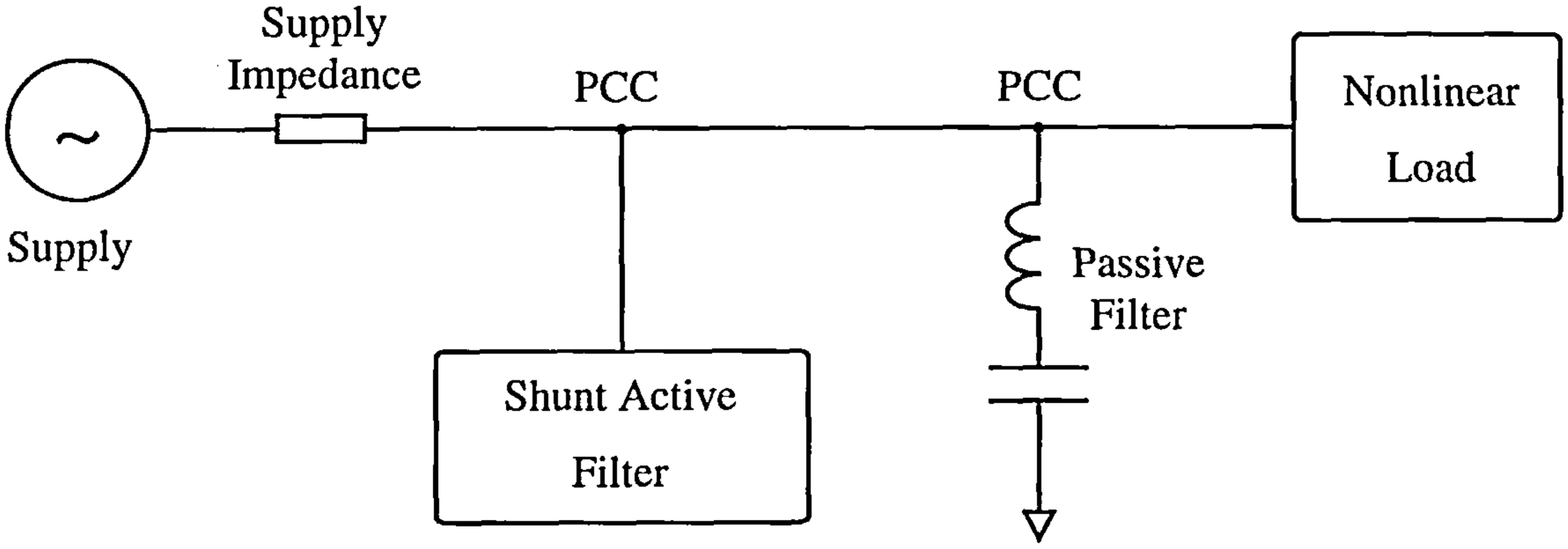



Fig.2.12 : Shunt active and shunt passive filter combination

**Active filter in series with shunt passive filters**

The single line diagram of this configuration is shown in Fig.2.13. It is considered in several publications of the literature [43,61,63] and is quite important especially for the case of medium and high voltage applications to reduce the maximum voltage withstand of the devices and static components. The idea is quite promising for

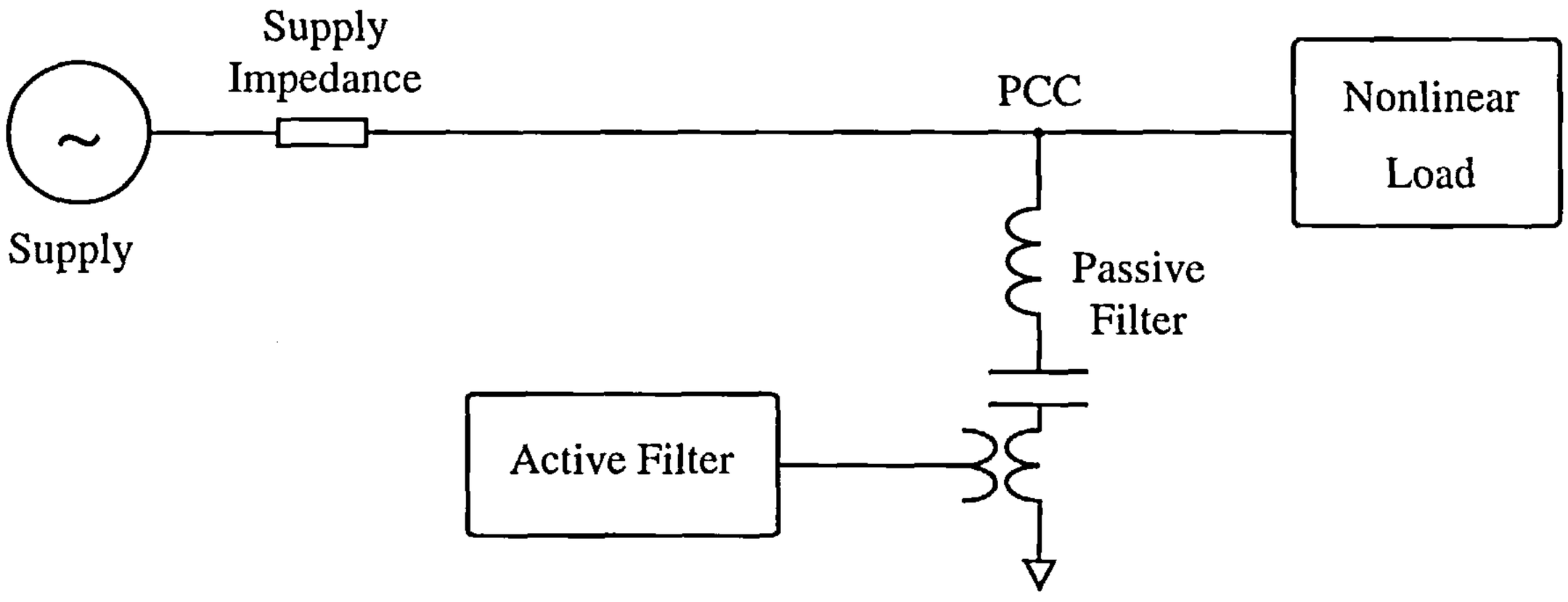



Fig.2.13 : Active filter in series with shunt passive filter combination

higher voltage applications but further research is still needed to decide the exact effectiveness of the configuration.

## 2.5. Classification according to the compensated variable

The power filtering techniques are built to improve some of the characteristics of the power system under question. These characteristics are considered as being the manipulated variables for the filter under consideration leading to the subdivisions presented in Fig.2.14 and discussed in the next paragraphs.

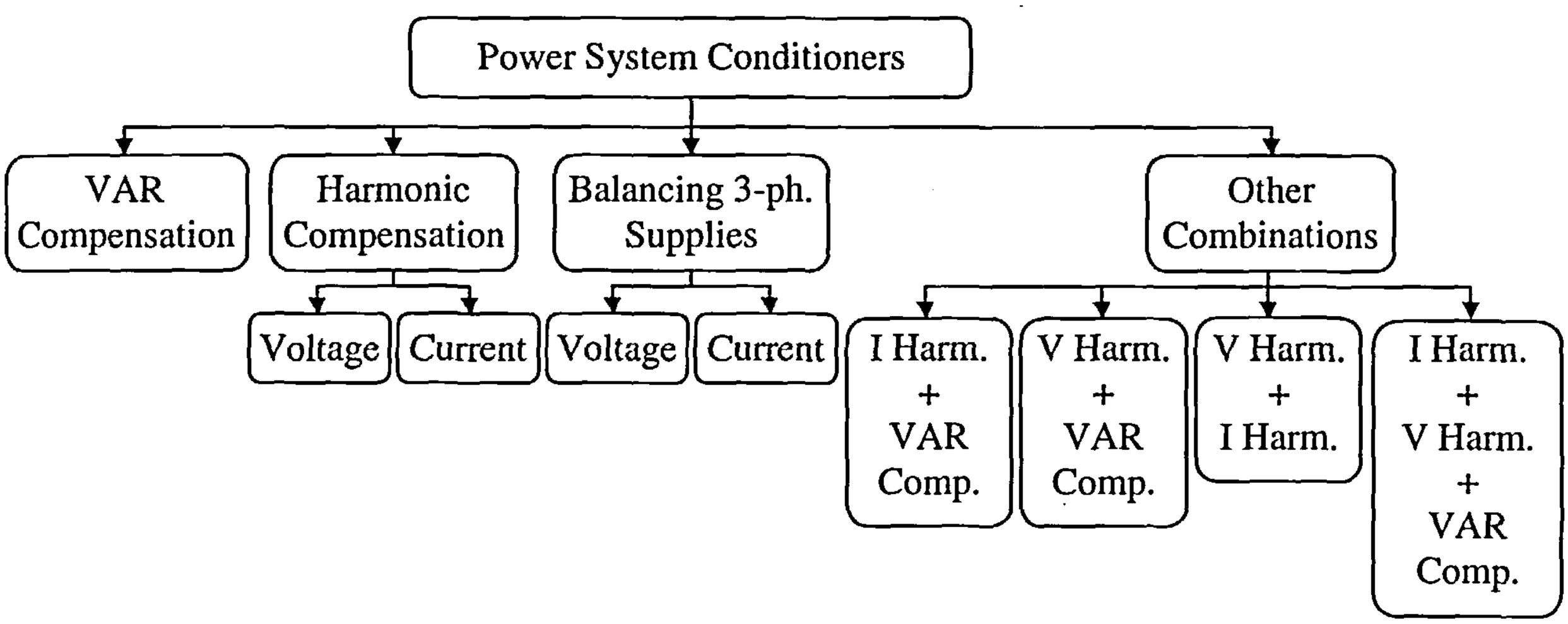



Fig.2.14 : Subdivision according to compensated variables

### 2.5.1 Fundamental reactive power compensation (VAR correction)

This compensation [36-38,40,45] is normally considered by most researchers as not being active filtering; however, the inherent compensation of the power factor in conjunction with the current harmonics is very simple and is addressed by many publications in the literature. On the other hand, active filter configurations rarely include the process of power factor correction on its own, due to the fact that other

quasi dynamic, cheaper and slower in response reactive power compensators are available in the market. This technique if applied would normally be suited for low power applications, especially in single-phase system configurations.

### 2.5.2 Harmonic compensation

This is the most important compensated variable in the power system and it is subdivided into voltage and current harmonic compensation as follows.

#### Compensation of voltage harmonics

The subject of compensating the voltage harmonics [3,22,39,55] is not common as normally power supplies are quite strong. The terminal voltage at the consumer PCC is normally restricted within the limits of the standards for sag and total harmonic distortion (THD) and does not normally change much with loading due to the relatively small supply impedance. This problem is normally addressed in the case of voltage sinusoidality sensitive devices, which require the supply to be purely sinusoidal without any higher order harmonics, such as power system protection devices and super conducting magnetic energy storage [8].

#### Compensation of current harmonics

The problem relating to current harmonics is very important in low and medium power applications and it is mostly addressed by most of the available publications [3,4,13-15,19-21,23-31,33-35,41-43,49] as it is the value of the current and its waveform that determines many of the power system design criteria. It is always recommended to decrease the rms value of current as much as possible. This would certainly imply reducing as much as possible of the accompanying harmonics.

### 2.5.3 Balancing of three-phase supplies

This problem mainly exists in low and medium voltage distribution systems, where the currents and consequently the voltages in the three phases are not balanced and are not spaced in time by 120° apart. This is described in the following two subsections.

**Balancing of mains voltages in three phase systems**

The magnitude of the mains voltage unbalance is of course dependent upon the amount of current unbalance and the amount of supply impedance. These can cause the three phase voltages to be unequal in magnitudes and unequally spaced in time. The remedy to this problem is of course to add to each phase the corresponding amount of instantaneous voltage to force it to follow the reference sinusoidal waveform. The system in such cases is normally of the low power category as in medium and high power systems, the supply impedance does not have any dominant effect on the system performance [3,63].

**Balancing of mains currents in three phase systems**

Similar to the above, this compensation is mainly concerned with the three phase systems of low power applications. The reason is that the magnitudes of currents to be supplied to the grid depends completely on the amount of unbalance in the system which is mostly pronounced in low voltage distribution systems to residential loads. The compensator under consideration [3,46,63] would sometimes be forced to supply the full rated value of current of the load power, which limits its power capabilities. The power circuit relating to this system is normally of the three single-phase type.

### 2.5.4 Multiple Compensation

Any combination of the above subdivisions is also applicable for the main and intuitive ideas of filtration techniques. The following are the mostly addressed combinations.

**Harmonic currents with reactive power compensation**

The most common and popular filters are those which compensate for both the reactive power and the harmonic currents in order to keep the supply current completely free of harmonics and in phase with the supply voltage [11,12,16-18,47,48]. These techniques are of course very advantageous over almost all other alternatives, as only one filter is needed to compensate for everything, which is much more appealing than using many different types of compensators. However, faced by the power switch ratings, one can not extend this application except for certain ranges of low powers. The resulting filter switching frequency would need to be lowered for higher power applications, which restricts the filter under consideration into small power handling capabilities. It would be a waste for the highly sophisticated and the state of the art techniques into a task of limited requirements.

**Harmonic voltages with reactive power compensation**

This combination [3], however rare, takes place in certain configurations for controlling the voltage harmonics, which would normally affect indirectly (using suitable feedback) the reactive power compensation. This compensation system is only suitable for low power applications.

### Harmonic currents and voltages

The problem of addressing harmonic currents and voltages together can also be treated by using the series/shunt combination of active filter configurations. This of course is very important and very beneficial in making both the supply and the load free from harmonic effects [3,46]. However, this complex type is normally used for very sensitive devices such as power system protection equipment as well as super-conductive magnetic energy storage.

### Harmonic currents and voltages with reactive power compensation

This manipulation scheme is the ultimate of all as it controls harmonics and reactive power presented by the system to both the supply and the load [3,46]. This technique requires the use of the shunt/series active filter combination. It is not very common in the applications of active filtering. However feasible, the control of this system is considered quite difficult and hence, is not heavily addressed in the literature.

## 2.6. Classification according to the control technique

From the point of view of control techniques, the power filters can be classified into the subdivisions shown in Fig.2.15 and discussed in the following.

### 2.6.1 Open-loop control systems

Open loop systems do not sense the load current or the harmonics it contains. It simply injects a fixed amount of reactive power in the form of reactive current into the system, which would, "hopefully" compensate most of the harmonics and/or reactive power available. This was mostly the case for some of the old filtering

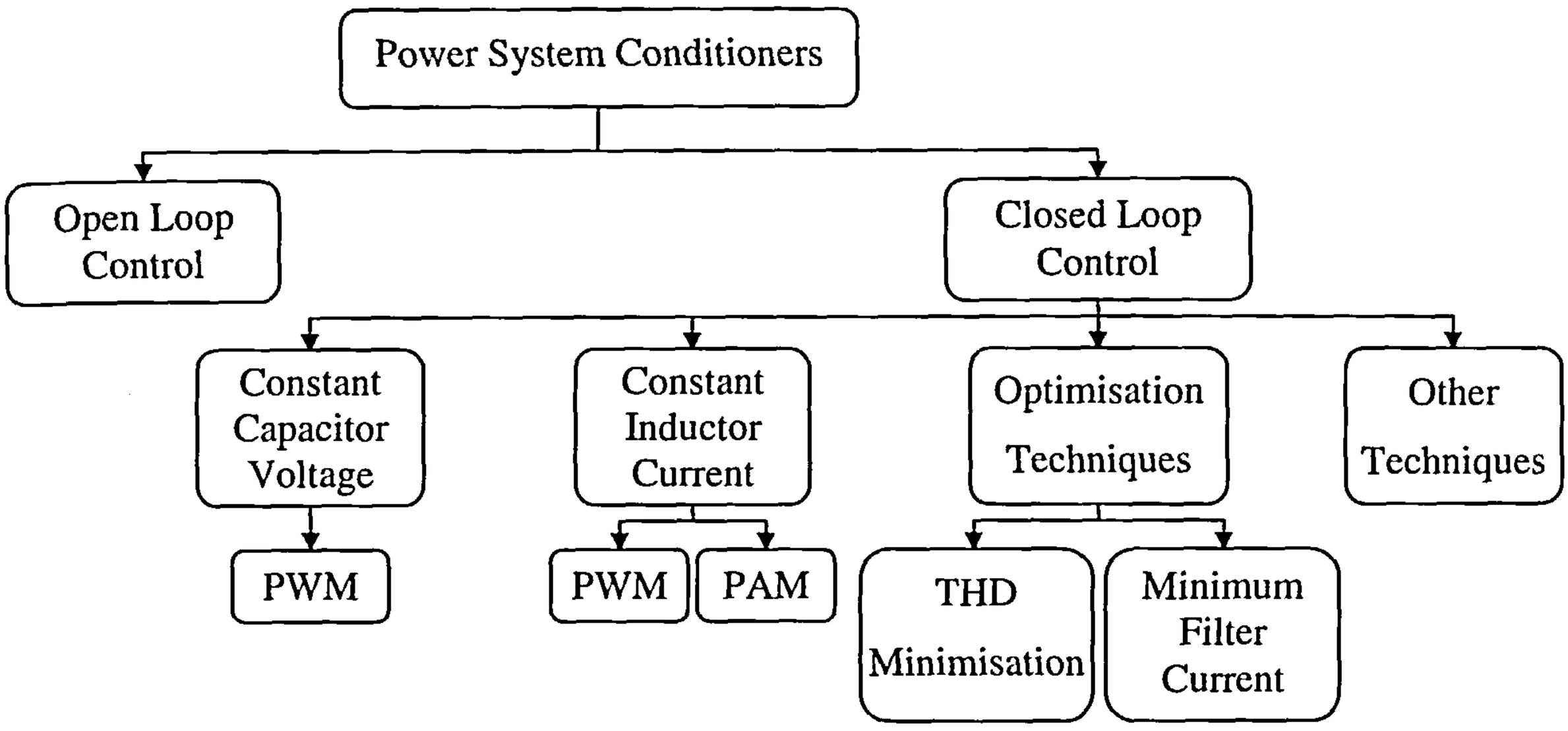



Fig.2.15 : Subdivision according to control techniques

techniques. Such techniques may include the passive filtering systems, which are not discussed here, in addition to the following techniques:

- Harmonic elimination by third harmonic injection [26,64].
- Harmonic cancellation devices [26].
- Systems with known constant load harmonic pattern [29].

### 2.6.2 Closed-loop control systems

As opposed to open-loop systems, the closed loop techniques incorporate a feedback loop, which senses the required variables that are under consideration. These systems would thus be more accurate from the point of view of the amount of harmonics and reactive power reduction they contribute to the power system under consideration. Almost all newly implemented techniques are of this type of closed loop filters; as a reference command signal is needed for the implemented tracking mechanism.

Hysterisis current controllers are nowadays implemented for most cases of current controlled voltage source inverters. They constitute the main control tool into nowadays power filters, which implies that the closed loop system can not deny the fact that these hysterisis current controllers, constitute by themselves an internal and inherent control loop apart from the main control loop under consideration. The compensation strategies can be subdivided into the following main four techniques.

### 2.6.2.1 Constant capacitor voltage technique

This technique, which is only suitable for single- and three-phase inverter configurations with a capacitor on the dc link, relies on the fact that the capacitor voltage is the main driving function which can synthesise any current waveform simply by connecting the capacitor to the mains supply through the smoothing inductor. The resulting current is then controlled by ordinary PWM technique. The error difference between the actual capacitor voltage and its reference value constitutes the active component of power necessary to compensate the power losses in the filter. This error difference is added to the current controller error signal to constitute the overall system error to be processed by the system current controller [3,4,11,12,15-20,22,37,39,40,43-45,47,48,55,63]. This technique is very popular as is clear from the large number of references provided.

### 2.6.2.2 Constant Inductor current technique

This controltechnique on the other hand is suitable for the case of standard inverters with an inductor on the dc-link. The operation of the system is then very similar to the previous case by simply replacing the capacitor voltage with the inductor current. Two main methods are used to implement this technique.

- **Current pulse-width modulation:** Similar to the case of the constant capacitor voltage, the PWM is used to give the appropriate timing to average the current signal in a specific time interval [4,13,14,21,33-36,38,41,42,46].

- **Current amplitude modulation:** This new control method suggested in [49] helps providing the active filters with a basis for amplitude modulation of the required current waveform. It also demonstrates that the concept is quite established, however, the state of the art power electronics technology may not, at the time being, be able to implement it practically.

### 2.6.2.3 Optimisation techniques

The optimisation of the switching angles of the power electronic switches of the circuits of both switched capacitor and lattice structure filter configurations [23-30] is almost the same. The rate of rise of the current and the amplitude depend mainly on the size of the capacitors and the initial voltages on them. These factors are function of the switching patterns and they provide considerable flexibility in shaping the waveform of the current drawn by the filter. The key to controlling these filter configurations is to determine the appropriate switching function for the switches. The main task of the system controller is to minimise a predetermined number of individual load current harmonics; in addition to the minimisation of either the THD or the fundamental component of the filter current. However, this task is not performed instantaneously. A time delay exists between the detection instant of the harmonic current change and the application of the new set of switching states

obtained from the optimisation. This system is mainly suitable for constant or slowly varying loads.

#### 2.6.2.4 Other techniques

Other control techniques exist [50,51]. These can not be constituted different from the point of view of the control strategy. They simply provide small changes to the aforementioned techniques providing simply newer or better performance over their predecessor techniques. Other techniques may include the state of the art adaptive and sliding mode controllers, which are normally difficult to implement without the presence of the special controlling hardware. These techniques can operate either in time or frequency domain.

## 2.7 Classification according to current estimation technique

As shown earlier in Fig.2.1, the reference current to be processed by the control loops constitutes an important and crucial measure of subdividing the active filtering techniques. Fig.2.16 illustrates these estimation techniques, which can not be considered to belong to the control loop as they perform an independent task by providing it with the required reference for further processing. Despite the fact that some publications do not mention their source of compensating-current reference, these estimation techniques can be classified as in the following subdivisions.

### 2.7.1 Current reference synthesis (Continuous time domain control)

This technique uses an analog signal filter to separate the harmonics from the main fundamental component. Thus obtaining the desired reference current to be

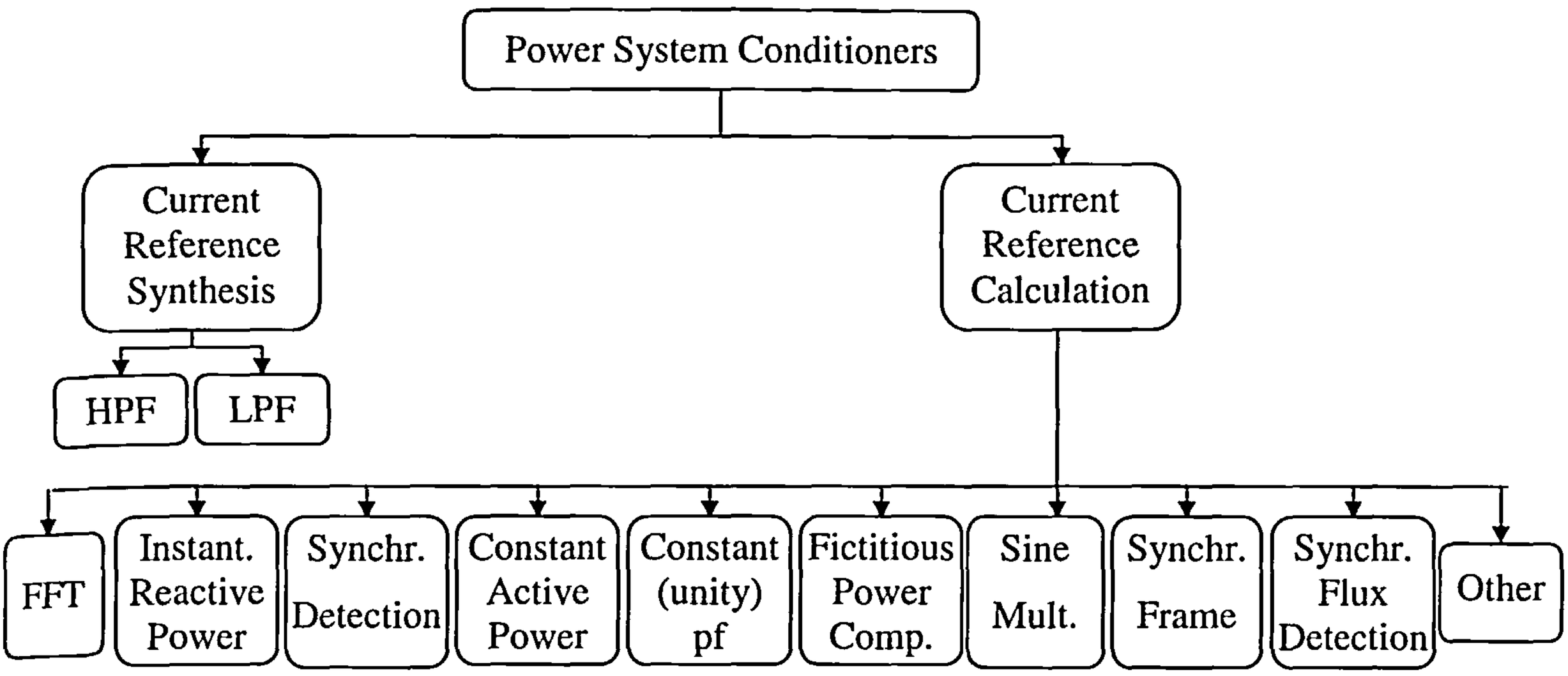



Fig.2.16 : Subdivision according to current estimation techniques

eliminated. This technique is only preferred due to the simplicity of implementation in the time domain using analog devices. It, however, suffers from a serious drawback, which is the phase and magnitude errors introduced by the signal active filter used in this method. Two main categories emerge.

- **High-pass filter method:** Using a high-pass filter is straightforward in taking the low order frequencies out of the load current signal. The resulting high frequency components constitute the desired reference current [4]. This filtering technique is considered to be equivalent to differentiation, which renders this technique vulnerable to noise.

- **Low-pass filter method:** However indirect, this method is preferred over the previous one as it reduces the effect of differentiation in the resulting filtered component. Filtering the fundamental component and then subtracting it from

the total load current yields the desired reference current [4,48,55]. As mentioned above, the system suffers from large magnitude and phase errors.

### 2.7.2 Current reference calculation (Discrete time or frequency domain control)

The calculation of harmonics is mostly adopted because of the main drawback of the previous technique, which incorporates phase angle and magnitude errors. The calculation methods can be classified as in the following subsections.

#### 2.7.2.1 FFT-Algorithms

Using fast Fourier transforms and the Fourier series expansion, the harmonic current can be reconstructed by eliminating the fundamental component from the transformed current signal and then the inverse transform is applied to obtain a time domain signal [4,21,34,36]. The main disadvantage of this system is the accompanying time delay. This analysis technique needs to take samples of one complete cycle (or an integral number of cycles) in order to generate the Fourier coefficients. This technique is mostly suitable for the case of slowly varying loads.

#### 2.7.2.2 Instantaneous reactive power algorithm

In this technique suitable only for three phase systems, the instantaneous power of the load is calculated and the oscillating component is then separated over a certain interval of time. The required reference currents are then calculated by equally distributing the current shares to each one of the three phases. This operation takes place only under the assumption that the three-phase system is balanced and that the voltage waveforms are purely sinusoidal [12,37,38,47].

### 2.7.2.3 Synchronous detection algorithm

This technique [12], which is very similar to the previous one, relies on the fact that the three phase currents are balanced. The average power is calculated and divided equally between the three phases. The signal is then synchronised relative to the mains voltage of each phase. This technique, however easy to implement, suffers from the fact that it is affected to a great extent by the harmonics in the voltage signal.

### 2.7.2.4 Constant active power algorithm

The instantaneous and average powers of the load are calculated. The active power component of the system is controlled to keep the instantaneous real power constant; while maintaining the imaginary power to zero. This technique performs quite well under ordinary conditions. However, the filter's performance deteriorates when the supply is contaminated [11].

### 2.7.2.5 Constant (unity) power factor algorithm

This is another technique, which is very similar to the above one, except in the fact that it only forces the instantaneous current signal to track the voltage reference waveform. This implies that the power factor would be fixed to unity and the system would only be suitable for the combined system of VAR and current harmonic compensation [11,12].

### 2.7.2.6 Fictitious power compensation algorithm

This technique relies on the principle of fictitious power compensation developed in [13-15]. Despite the opposition to the theory by [65-67], this principle was proven to operate properly. The system controller tries to minimise the undesired component of power. In this aspect, it is similar to the instantaneous reactive power algorithm but with a different concept of power definition. This technique is suitable for both single- and three-phase systems. However it involves a large amount of computations.

### 2.7.2.7 Sine multiplication technique

This technique relies on the process of multiplying the current signal by a sine wave of the fundamental frequency and integrating the result. This would result in a loss of all the high order harmonics using simple low-pass filtering techniques [16,31,43]. Nevertheless, the performance would still remain slow (more than one complete mains cycle). This technique is similar to the FFT algorithm presented earlier; it is however differently implemented.

### 2.7.2.8 Synchronous frame based algorithm

This algorithm relies on the Park transformations to transform the three phase system from a stationary reference frame into synchronously rotating direct, quadrature and zero sequence components which can be easily analysed since the fundamental frequency component is transformed into dc quantities [68]. The active component of the system is represented by the direct component, while the reactive component is shown by the quadrature component. The high order harmonics, still remain in the

signal, however modulated at different frequencies. These are the undesired components to be eliminated from the system and they represent the reference harmonic current. The system control in this case is very stable since the controller deals mainly with dc quantities. The computation is instantaneous but incurs time delays in filtering the dc quantities. This technique is only applicable to three-phase systems.

### 2.7.2.9 Synchronous flux detection algorithm

This technique is similar to the above one in applying the Park transformations to transfer the system into the synchronously rotating direct, quadrature and zero sequence frames of reference. It however applies the transformation on the flux linkage of the filter inductance, which is then controlled using the system output voltages and currents in different integral loops [69]. The presence of these integral loops incorporates system time delays, which depend on the frequency response of the special feedforward and feedback integrators.

### 2.7.2.10Other algorithms

The harmonic optimisation and estimation techniques are numerous and all the utilities and libraries of the mathematical estimation can be used to perform this task. However certain new methods arise such as the neural network and the adaptive estimation techniques which are quite accurate and have of course a much better response [50,51,70-72]. Unfortunately, the available nowadays hardware implementations are not adequate to fulfil the needs of these new techniques.

## 2.8 Summary

The subdivisions outlined in this chapter present a quick review of the state of the art technology presented in the surveyed published literature. It constitutes the basis of a global subdivision of the state of the art techniques used in the field of active power filtering. This subdivision is very useful from the point of view of recognising the merits and drawbacks of each type and configuration of active filters. These points will lead to the definition of the performance criteria necessary for designing the proposed power circuit and its control strategy. These criteria will be discussed further in the following two chapters.

# Chapter 3

# Proposed Power Circuit

# Chapter 3

# Proposed Power Circuit

## 3.1 Introduction

The previous chapter outlined the basic principles on which most of the active filter configurations are based. The majority of the available techniques are shown to employ the conventional single- or three-phase inverter circuit configurations. The first section of this chapter outlines the main problems and disadvantages that these configurations suffer from. This leads to the identification of the main requirements for improving the active filter circuits and the associated control techniques. These requirements are subsequently developed, during the course of this chapter, in the form of control principles that will be used for the proposed filter circuit. The choice of the control strategy is developed and backed up with the frequency response analysis of the filter both as a standalone device and in conjunction with the other power system components. The simulation results of this overall circuit performance are also presented in the course of this chapter.

## 3.2 Disadvantages of inverter-based active-filter configuration

In order to study the problems of inverter type active filters, a typical single-phase inverter circuit is considered here for simplicity as shown in Fig.3.1. The voltage ($v_C$) across the dc link capacitor ($C_{dc}$) is used to drive current through the inverter switches into the smoothing inductor ($L_f$) of the filter. The rate of change of the current flowing through this inductor ($di_f/dt$) is directly proportional to the instantaneous

voltage difference between the supply voltage ($v_s$) and the voltage at the inverter terminals ($v_f$). The requirement of the circuit is that the inductor current ($i_f$) follows its desired reference. In order for the inverter to perform its task as an active filter, the capacitor voltage ($v_C$) is required to be constant and much higher than the peak value of the supply voltage. This fact represents the main weakness of inverter-type configurations of active filters.

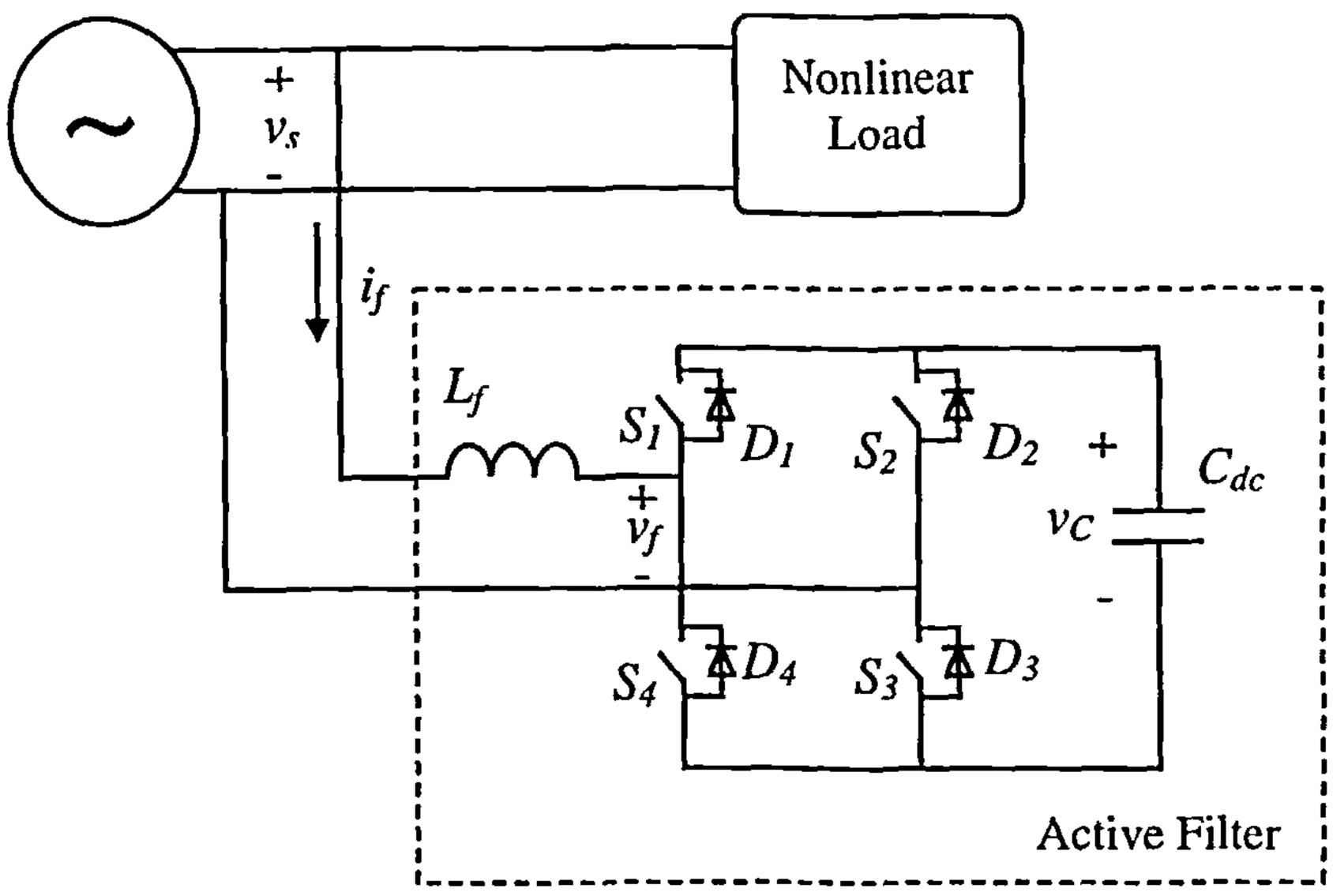



Fig.3.1 : Single phase voltage source inverter

As stated in [29], the main disadvantages of the inverter configuration circuits are that they employ relatively large high-voltage dc-link capacitors (4000-9000 μF) to serve as a stiff dc voltage source. In addition, they use relatively high switching frequencies (20-30 kHz) to control the filter current. These two aspects are analysed and demonstrated in the following two subsections.

### 3.2.1 Constant dc-bus voltage

The problem of dc bus voltage is dominant in all systems employing voltage source inverter configurations (the same applies for the case of CSI regarding the dc-side inductor current). The ideal case for the voltage control from the dc-side of the switches is of course to use a battery, which would allow the current to be controlled as required by the controller; while the voltage across its terminals is fixed. This case is shown in Fig.3.2, which incorporates the inverter-type active filter with a nonlinear load. The corresponding PSPICE schematic circuit diagram is presented in Appendix A (Fig.A.1). Fig.3.2. The simulation results of the circuit for a dc supply of 200 Volts are given in Fig.3.3. It is of course seen that the performance of the filter at this range of low switching frequencies is quite satisfactory. The major drawback of the

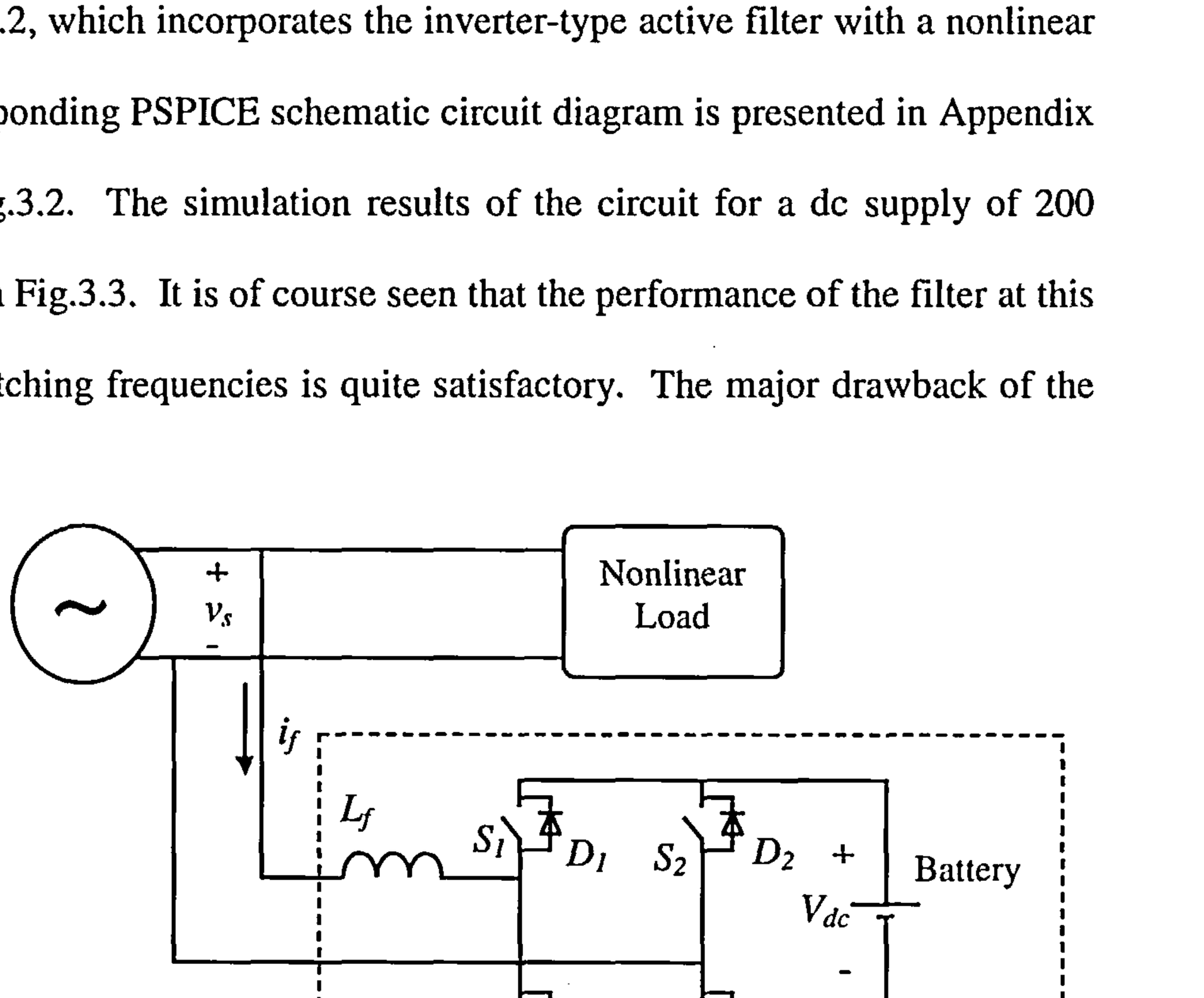



Fig.3.2 : PSPICE representation of inverter filters with a secondary dc-supply

above circuit is the use of the external dc supply, which adds to the circuit complexity. The practical system is to use a very high value of capacitance, which would emulate the performance of the battery. This is shown in the inverter circuit diagram of Fig.3.1, represented by the dc-bus capacitor ($C_{dc}$). This capacitor can be charged using the bridge formed by the fast recovery diodes ($D_1$ *to* $D_4$), which also serve for freewheeling action across the switches.

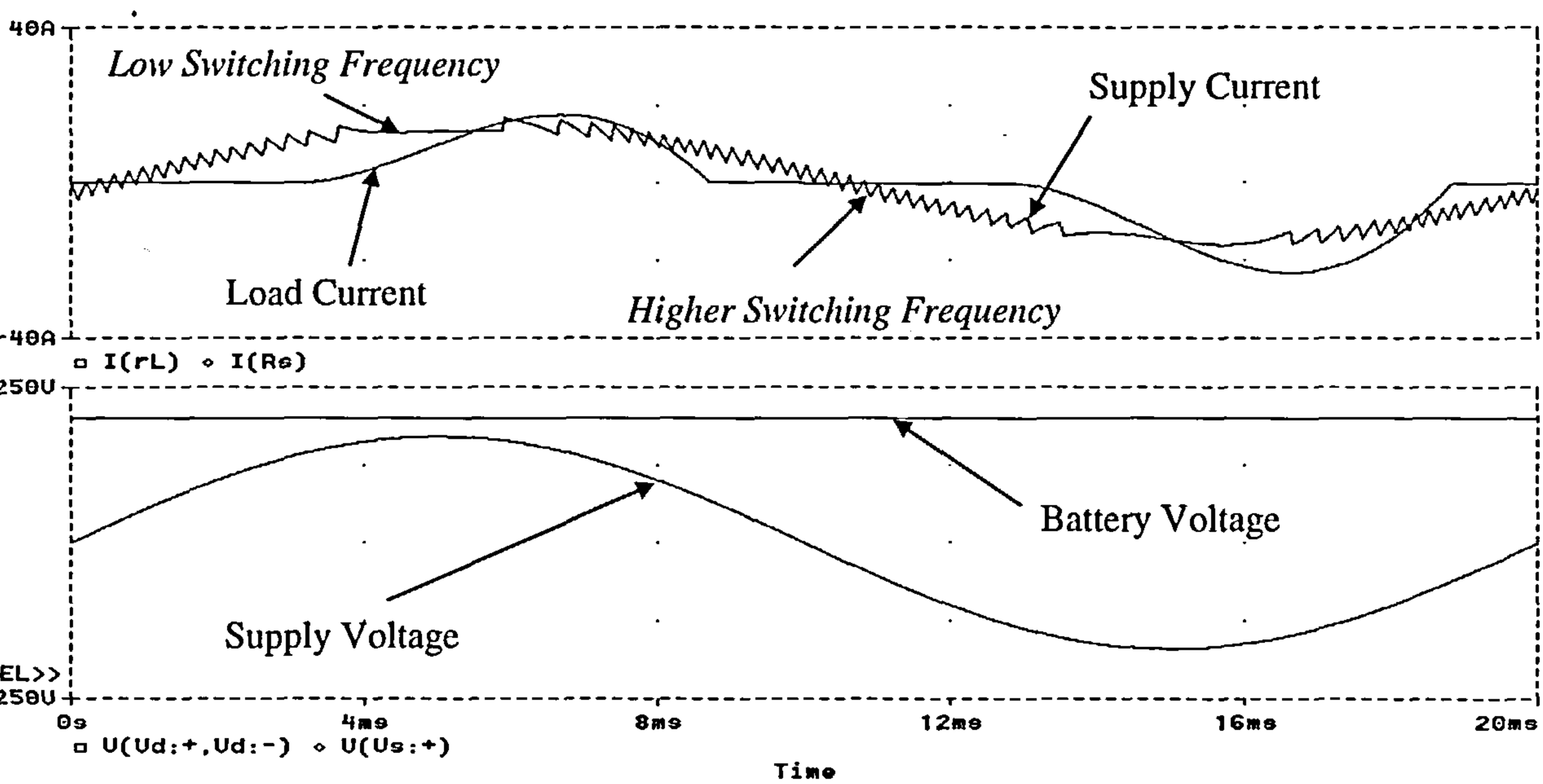



Fig.3.3 : PSPICE simulation results for inverter filters with a secondary dc supply (200Volts)

The maximum voltage to which $C_{dc}$ can charge, without any auxiliary mean, is the peak of the supply voltage ($V_{s\,\max}$) as shown in Fig.3.1. However, due to voltage drops in the circuit, the voltage across the inverter terminals ($v_f$) is less than $V_{s\,\max}$. This implies that the filter circuit would not be able to force enough current into the supply at those instants of time when $v_s$ is near its peak value. To overcome this problem, the dc-link capacitor is overcharged using the inverter switches as a boost

converter. The inverter current paths, shown in Fig.3.4, explain this process clearly. The figure shows one of the possible combinations of current paths, indicated in thick lines, for charging the filter inductor (Fig.3.4-a), releasing the charge to the dc-link capacitor (Fig.3.4-b)and finally the discharge process of the capacitor into the mains (Fig.3.4-c).

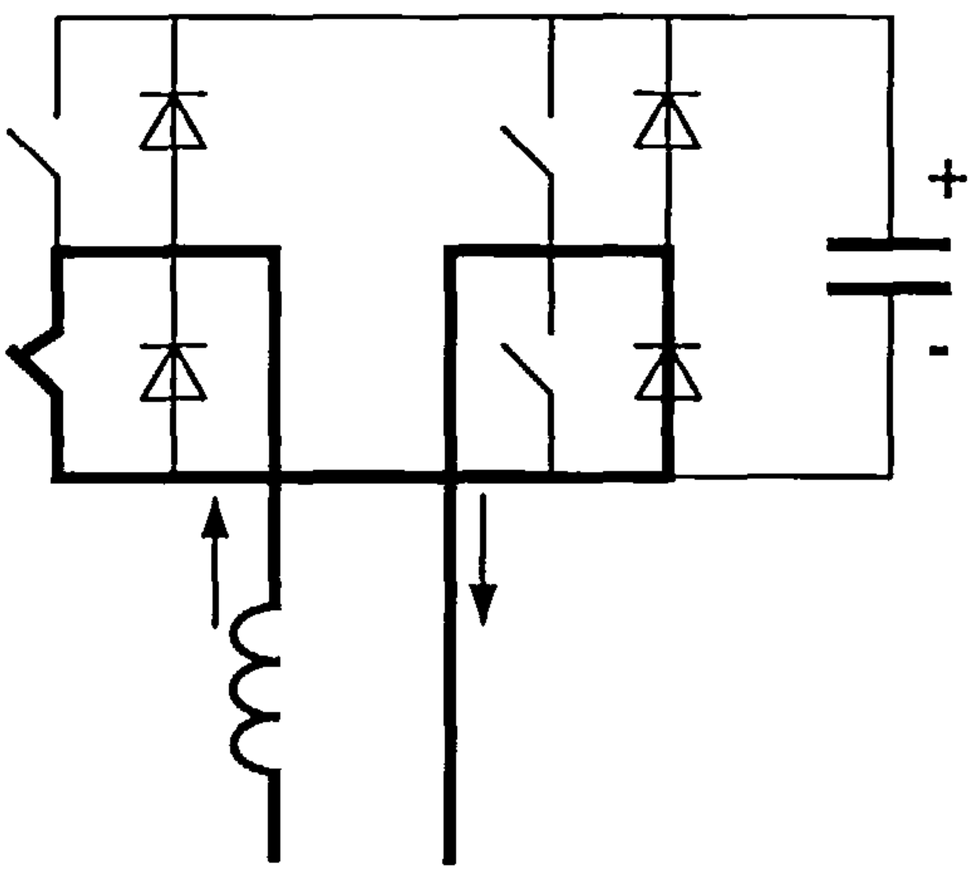



Fig.3.4-a : Charging the filter inductance

(positive current slope)

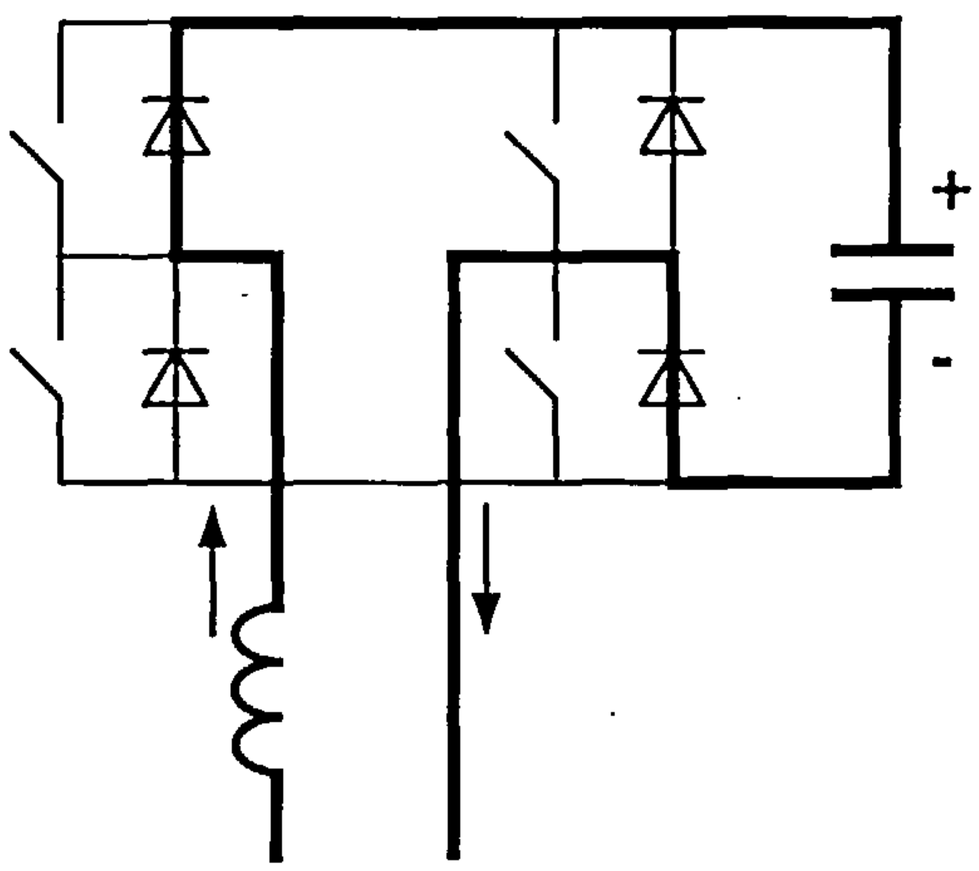



Fig.3.4-b : Releasing the inductor charge to the capacitor

(decaying positive current slope)

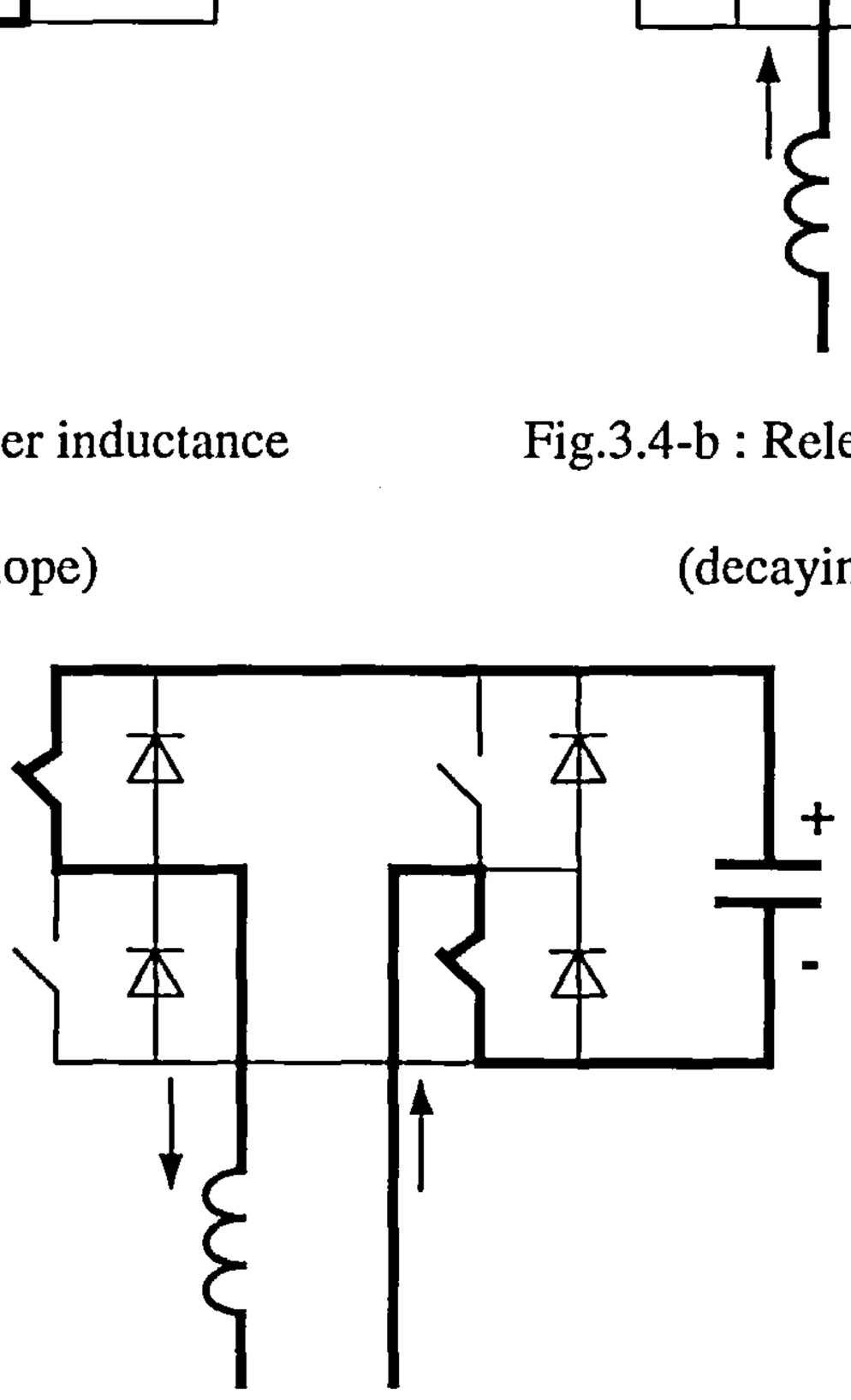



Fig.3.4-c : Capacitor voltage driving current into the supply

(negative current slope)

The operation of the filter-inverter with a dc-link capacitor is simulated using PSPICE as shown in the circuit diagram of Fig.3.5. The corresponding PSPICE detailed diagram is presented in Appendix A (Fig.A.2). The simulation results are shown in

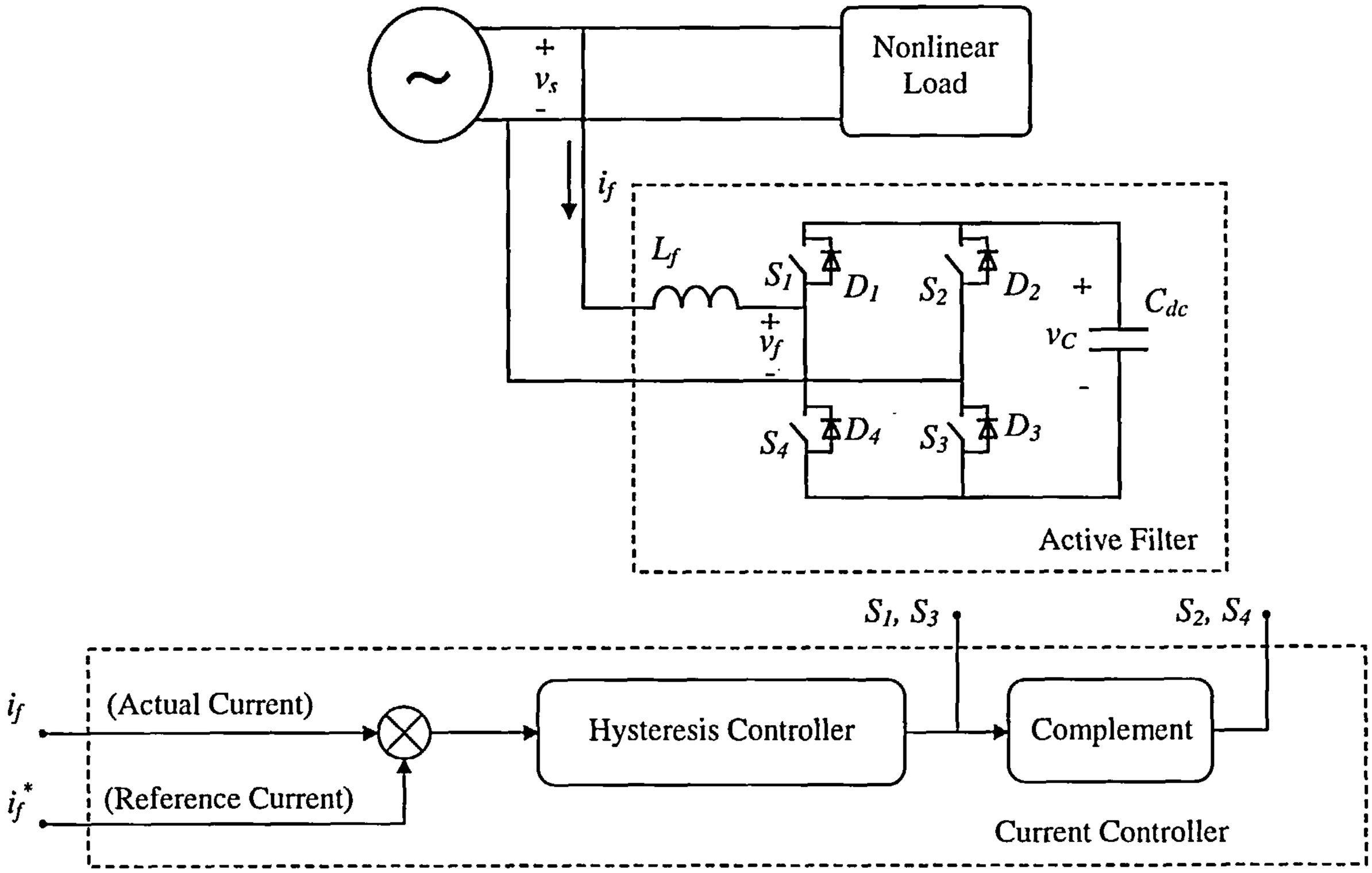



Fig.3.5 : PSPICE representation of inverter filters with a secondary capacitor

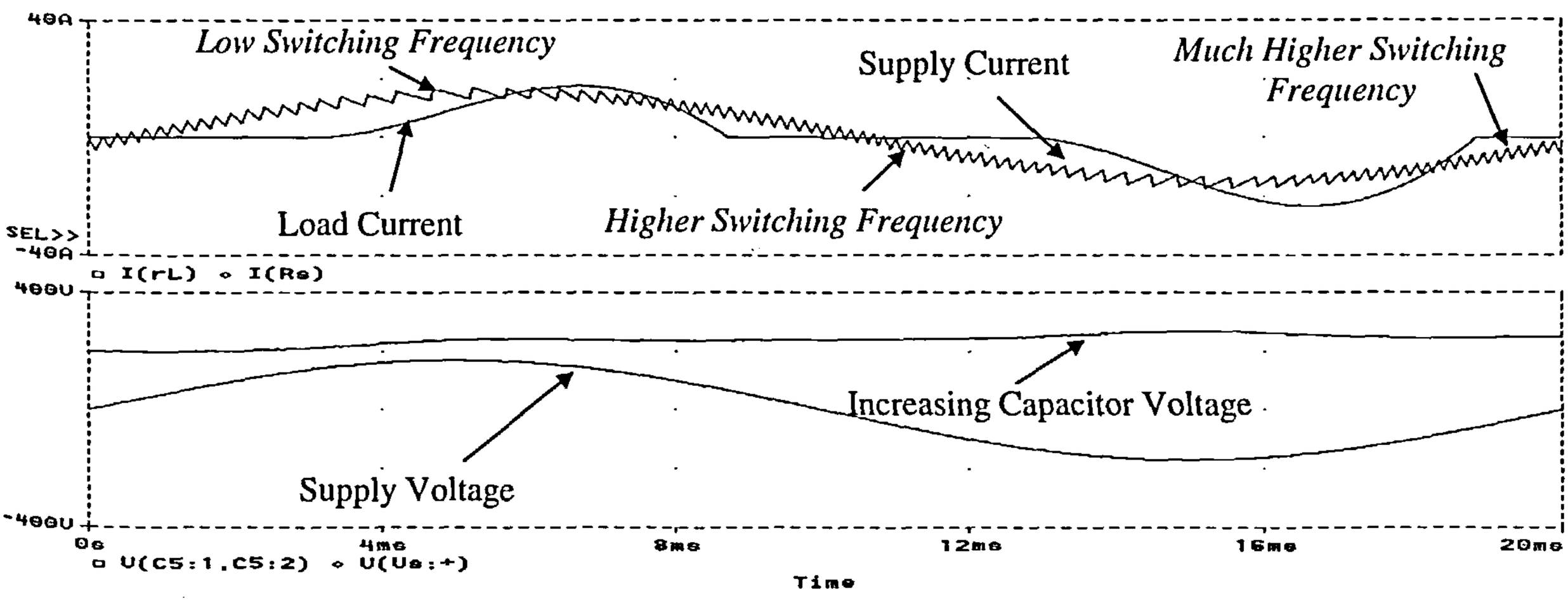



Fig.3.6 : PSPICE simulation results for inverter filters with a secondary capacitor

Fig.3.6. The response is somehow different from the ideal dc-supply case outlined in Fig.3.3, from the point of view of the dc-capacitor voltage, which is seen here to increase. This voltage rise results in a corresponding increase in the switching frequency of the inverter as manifested in the supply current waveforms.

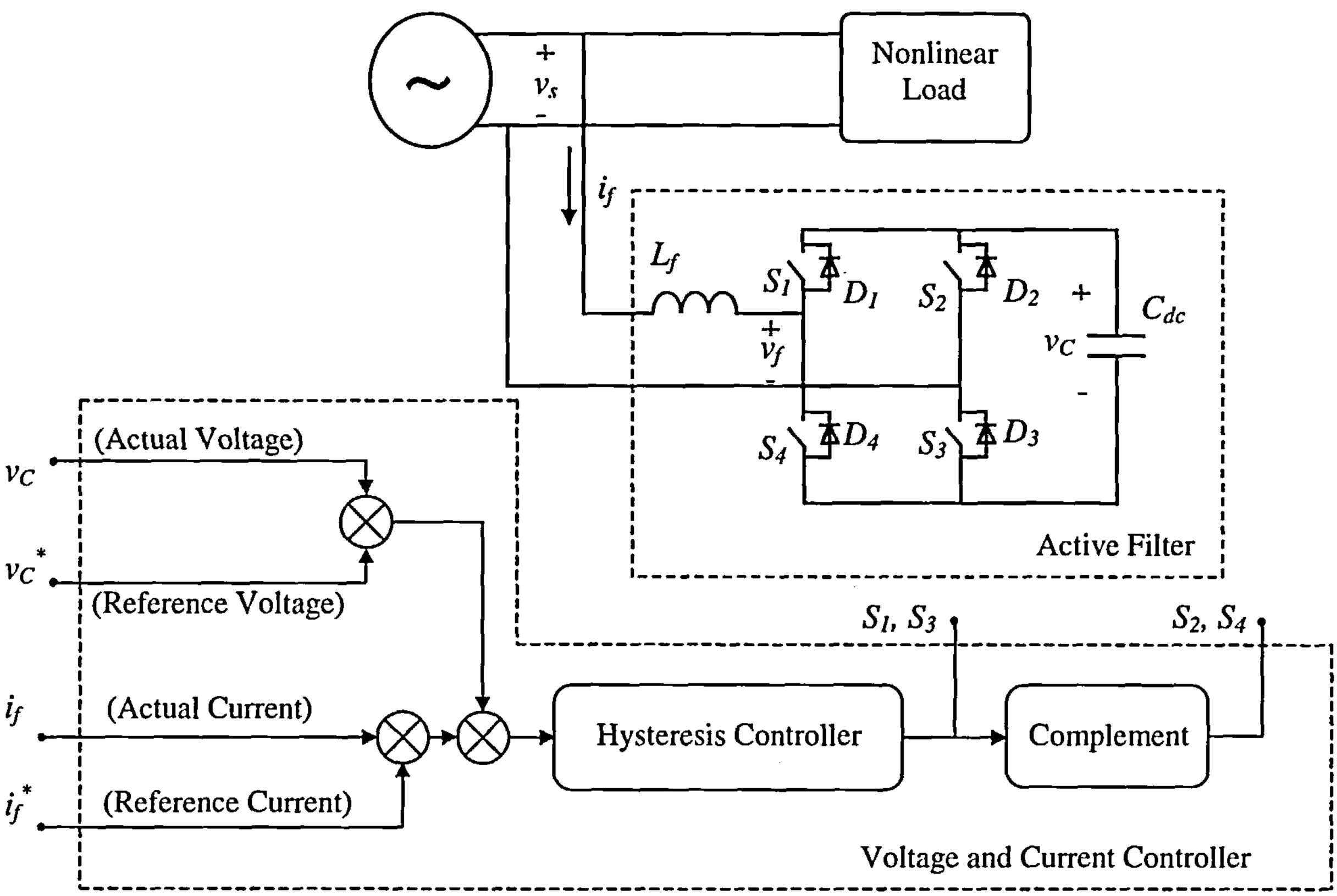



Fig.3.7 : PSPICE representation of inverter filters with a secondary capacitor and a capacitor voltage control loop

To avoid this problem, more complicated circuits using voltage feedback loops are used across the capacitor voltage. A simplified version of this circuit is modelled in Fig.3.7 for PSPICE simulation. The corresponding detailed PSPICE circuit diagram is presented in Appendix A (Fig.A.3). The simulation results are shown in Fig.3.8. It

can be seen that despite the superimposed oscillations, the capacitor voltage shows no long term drift as compared to Fig.3.6. However, the system performance is slightly degraded since the current tracking falls behind at the instants of the supply peaks. This performance degradation would eventually render this system inefficient since the feedback signal alters the error tracking process as discussed in the following paragraphs.

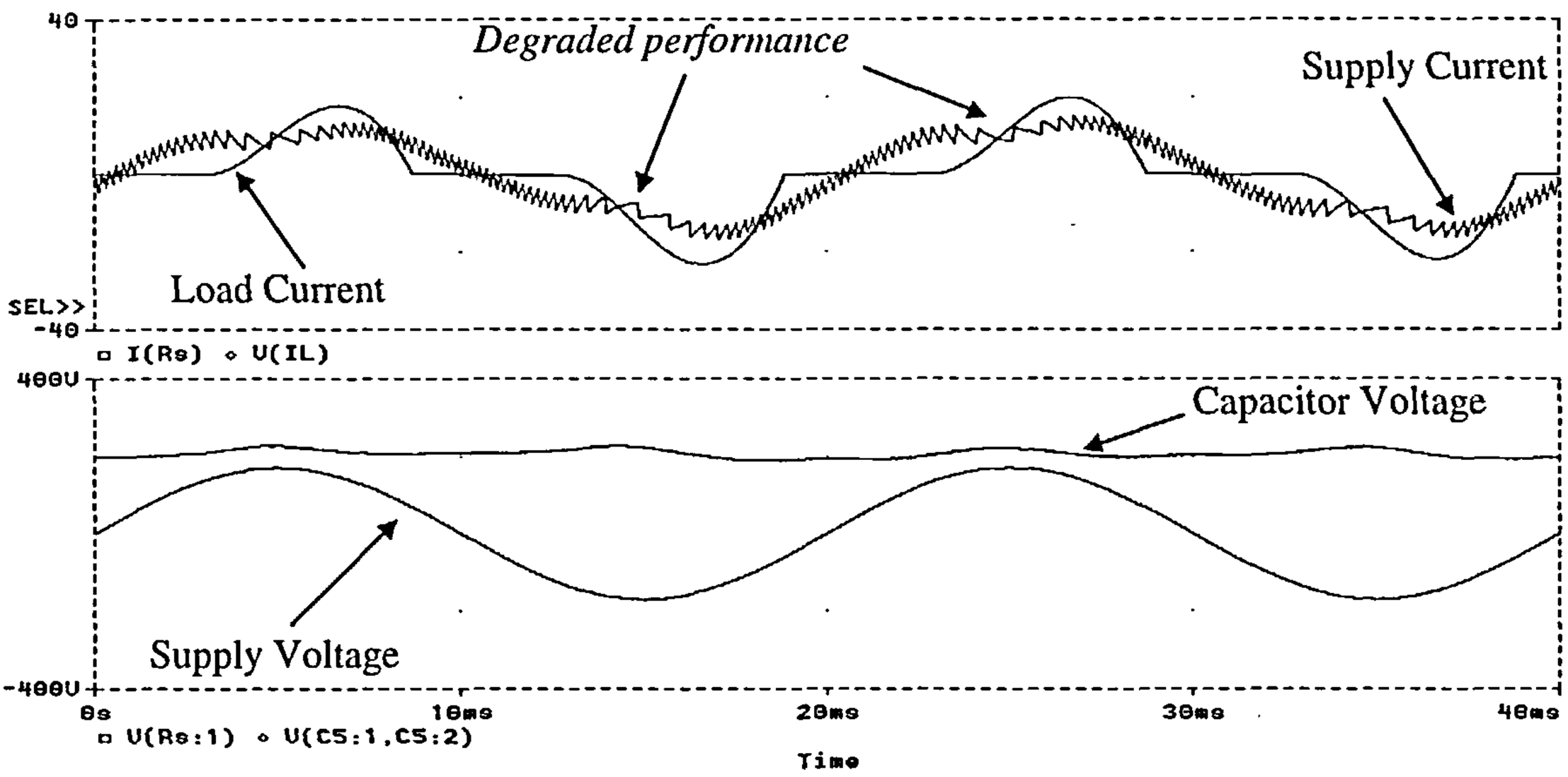



Fig.3.8 : PSPICE simulation results for inverter filters with a secondary capacitor and a capacitor voltage control loop

It is very important to note that the tracking of the reference current waveform must use all the time necessary for performing the control (the PWM process). This time is termed: the 'control time'. In order for the switches to perform the charging process a certain period of time is taken out of this control time. Moreover, the dc-link capacitor overcharging process is performed regularly to keep $v_C$ sufficient to force current back into the supply. This process is mainly dominant near the zero crossings of the supply voltage, where the amount of voltage is insufficient to properly control

the necessary overcharge across the capacitor. In other words, there exists a higher dc-link voltage error signal near the supply zero crossing than the PWM reference signal at this instant of time. Adding those two signals, forms the total error, which is used to drive the PWM modulator.

The system in this case suffers from a major problem. The continuous and forced application of the reverse or zero voltage vector states (where the current is being pumped into the inductor) is considered as being a main reason for the increase in the switching frequency. This fact can be observed in the case where the actual filter current error is much smaller than the value of the dc-link voltage error. For a proper system performance, the last switching state should then be kept unchanged for as long as the current error is within the allowable error-boundaries. Any switching performed using the inverter switches under this condition is quite inappropriate. However due to the addition of these two error signals, different switching pulses take place; hence unnecessarily increasing the switching frequency of the switches.

To alleviate the capacitor voltage variation problem, the system designers usually use larger dc-link capacitors in order to establish a relatively constant dc link voltage. This voltage is used by the controller without introducing errors to the PWM process due to voltage drops. The 470-500 μF capacitors used in the simulation are merely to explain the problem and it is noted that values higher than 4700 μF are in normal use [3,4]. These high values create other problems of size, cost, reliability and durability of the various components assembled together to form the desired large value of capacitance and to meet the high voltage ratings by series and parallel combinations.

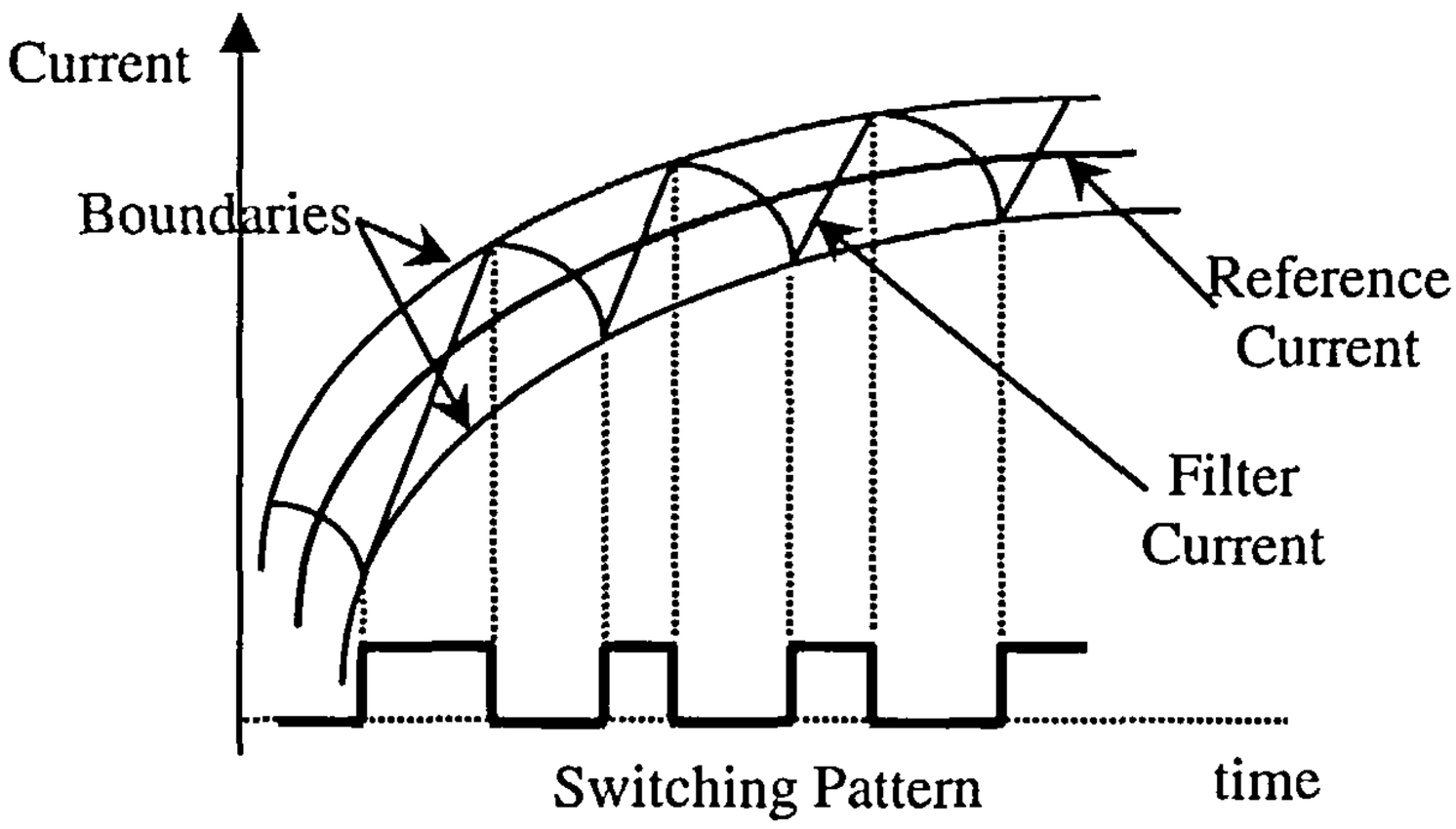
### 3.2.2 Higher switching frequency

The problem of the switching frequency of the inverter-type active-filter, shown in Fig.3.1, can be addressed by considering the accuracy with which the current waveform is to track its reference. The bandwidth of the tracking process is mainly controlled by the filter inductance, $L_f$ and the PWM switching frequency, $f_s$. The switching frequency also depends on the number of pulses used per cycle.

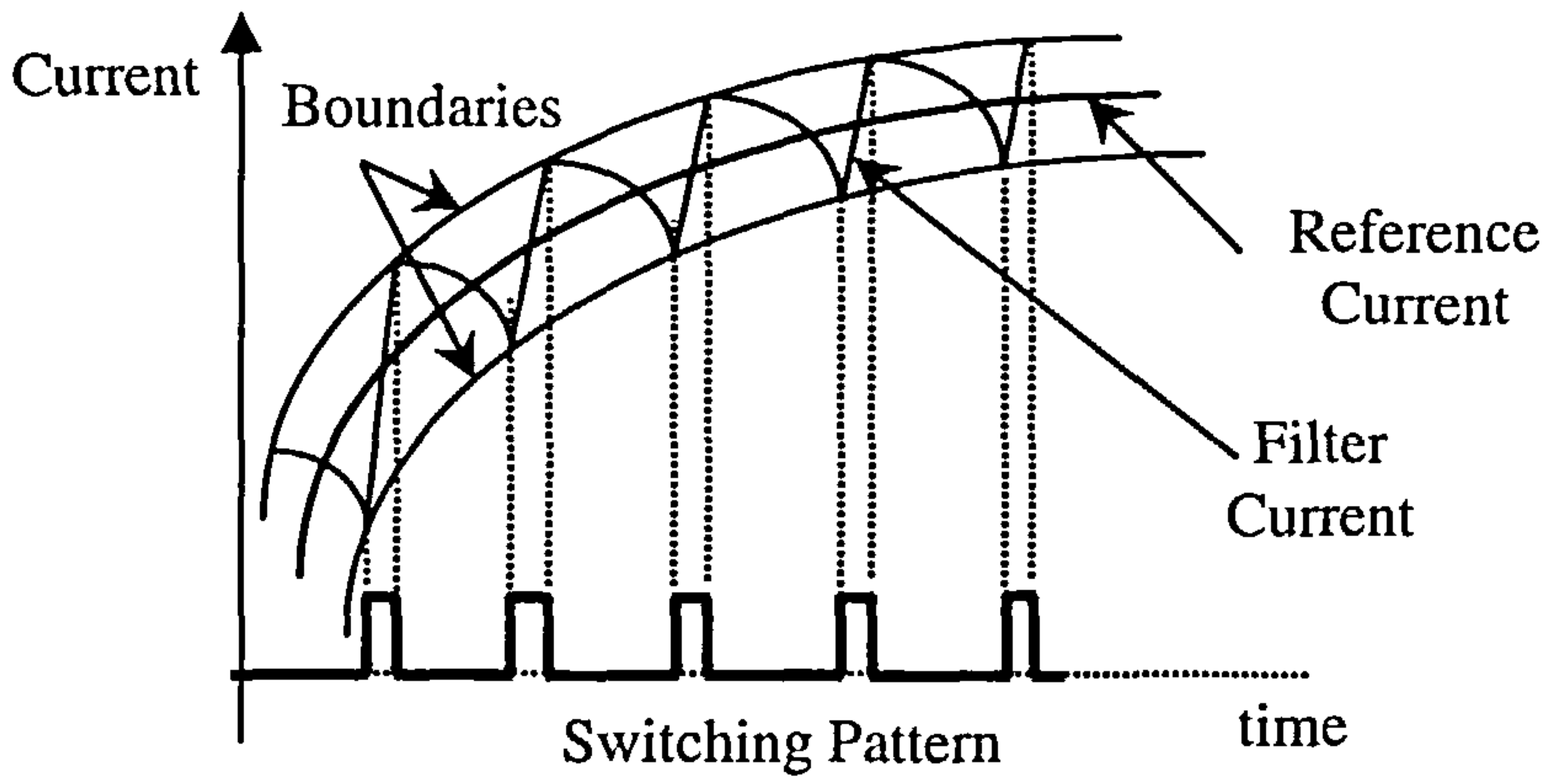
It is normally recommended to use low switching frequency since the switching losses would be considerably reduced as well as the fact that the semiconductor switches are able to handle larger values of currents. In order to choose the value of the switching frequency, use is made of Channon's theorem as applied to the highest frequency to be compensated ($20^{th}$ harmonic). The number of pulses to be used should be higher than double the order of the highest frequency of interest (40 pulses). A reasonable value for the number of pulses per cycle would then be between 80 and 160 pulses per cycle to synthesise a current waveform [29]. If an average value of around 120 is assumed, it implies a switching frequency of 6000 Hz and a maximum pulse width of about 166 μsec. This means that if the optimal switching pulses are applied to the inverter, the maximum switching frequency for the desired accuracy is not to exceed 6000 Hz. However, inverter configurations for active filters do not operate at such low frequencies due to two reasons.

One of these reasons is discussed in the previous section and includes the time taken by the switching mechanism to charge the dc-link capacitor. The other reason would be understood by considering the fact that the switching frequency near the zero-crossings of the supply voltage waveform is at its highest values (determined by the

type of switches used), while it is much lower elsewhere. This can be modelled by considering the fact that at the zero crossings, the full dc-link voltage is applied solely across the filter inductor. The rate of change of filter current is large, causing the current to cross the other boundary of the hysteresis error-controller used in the system quickly. This causes the system to transfer to a different switching state where the process repeats at a very high rate, forcing the controller to increase the switching frequency to very high values. This fact is shown by the current/time waveforms of Fig.3.9. Fig.3.9-b shows that a high switching frequency is required for high dc voltage, while a lower switching frequency is needed for a low dc voltage as shown in Fig.3.9-a. The same result can be visualised by taking a closer look at the




a - Lower dc voltage and lower switching frequency




b - Higher dc voltage and higher switching frequency

Fig.3.9 : Current variation at different applied voltages

switching frequency of the compensated waveform of Fig.3.3 and compare its switching frequency with that of the waveform of Fig.3.10, which was simulated for the same conditions except for the value of the dc-supply voltage which was taken as 300 Volts. The switching frequency in the second case is much higher than that of the first one (note that the allowable current error is the same for both cases). In addition, it should be noted that the current error will normally exceed the set boundaries and a persistent error would dominate especially at the instants of zero crossing of the supply voltage.

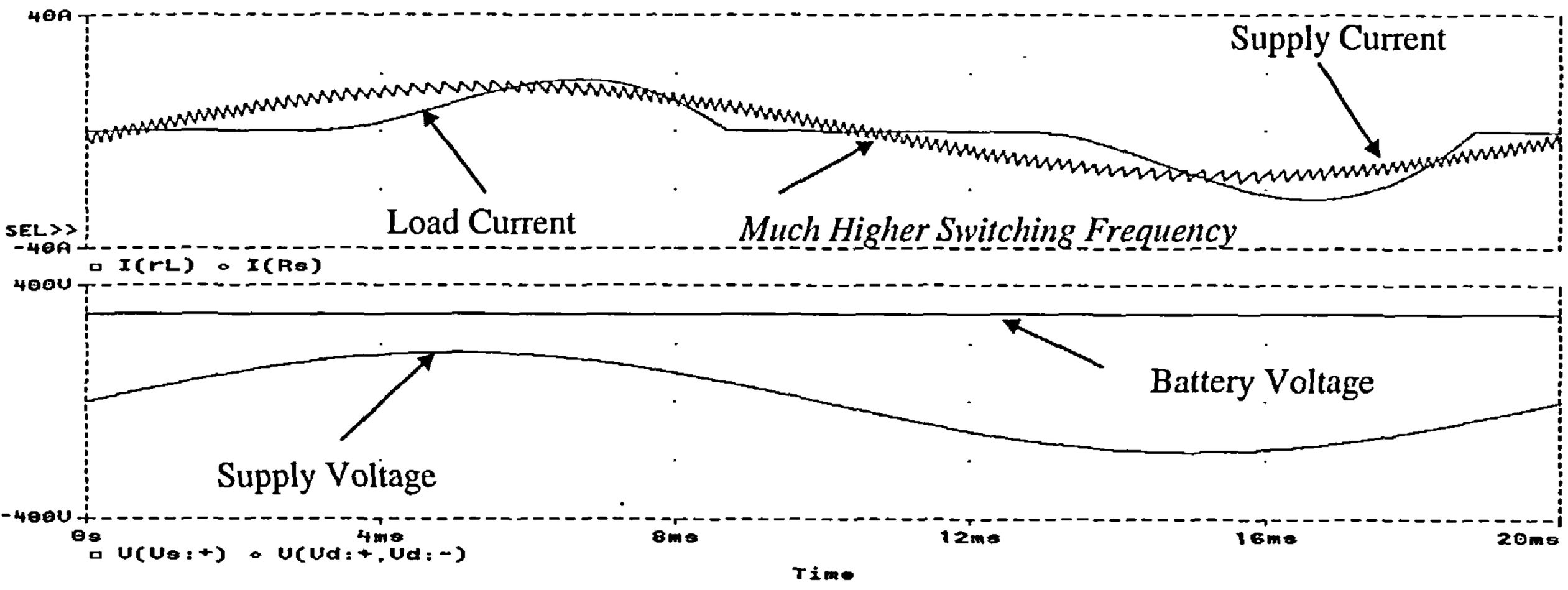



Fig.3.10 : PSPICE simulation results for inverter filters with a secondary dc supply (300Volts)

Under these conditions, the inverter switching frequency attains its upper limit, which is normally that of the switches. This cycle repeats continuously until the system supply voltage is large enough to lengthen the period of current rise, eventually reducing the switching frequency.

A worse case, similar to the above, occurs when the supply voltage is positive (or negative) and the dc link capacitor is applied to the circuit with negative (or positive)

polarity. The total voltage magnitude across the inductor is then ($V_{dc} + V_{s\,max}$) in either corresponding polarities. A higher switching frequency would then be required as shown by the above simulation results.

This problem is best explained in the work of Brod and Novotny in 1985 by their famous "switching diagram" drawn for the similar case of a stalled three-phase induction motor (no back emf) [73]. The paper proves analytically that the worst switching frequency of the inverter, which occurs at the absence of the motor back emf, is given by the following equation reproduced from [73] for convenience,

$$f_s = \frac{V_{dc}}{9hL} \tag{3.1}$$

The above equation implies the direct proportionality of the switching frequency ($f_s$) to the dc-link voltage ($V_{dc}$) and its inverse proportionality to the allowable hysteresis band ($h$) and the system inductance ($L$). These last two factors are not under control as the maximum allowable system error determines the hysteresis band; while the system inductance is a characteristic of the filter system and is governed by the desired frequency response. The only controllable variable in the above equation is then the dc-link voltage of the inverter system.

The solution to this problem would be to reduce the capacitor voltage to reasonable values (sufficient to drive current into the supply at the required rates) in order to allow a simpler control of the filter current. However, changing the capacitor voltage is rather difficult to achieve using the inverter configuration. This is due to the limitations of charging and discharging times of the large value dc-link capacitance, which can not be reduced otherwise the voltage ripple across the capacitor terminals would assume large values.

From the above discussion, it can be concluded that the structure of the power circuit needs to be altered. The requirements of the "new system" need to be specified. This takes place in the following sections, which will present a different analysis technique leading to the target.

## 3.3 Alternative solutions

To overcome the above problems, other techniques such as the switched-capacitor system [23-26,29-31] and the filters incorporating lattice-structures [27-29] were introduced, offering better performance with fewer component numbers and much smaller values. Despite this fact as an achievement compared with the circuits using the inverter configurations, the control algorithm of the PWM switching strategy is quite complicated since these circuits depend, in their operation, on optimisation techniques for the generation of the pulse widths. The fact that this optimisation takes up a considerable amount of computational time to converge to the optimal switching patterns within the allowable limits, makes these systems unsuitable for on-line control of fast changing harmonic loads. These configurations would be ideal for the harmonic elimination in high and medium voltage distribution systems, where the harmonic current patterns change relatively slowly. On the other hand, these circuits would be inadequate for the fast changing loads (such as high-power drives) with fast dynamic response.

The above discussion shows the need for a radically different method considering the point of view of the power circuit and the control technique of the switching strategy. This would be further clarified in the following sections.

## 3.4 Theoretical analysis of active filter performance

The power circuit configuration of any active filter can be thought of as being composed of two sources that are interconnected through a coupling inductor, as shown in Fig.3.11. The main source, representing the supply, is assumed to have a sinusoidal voltage waveform. The auxiliary active nonlinear source, which represents the filter, provides a pulse width modulated waveform, which controls the current flowing through the filter inductor ($L_f$) and consequently reduces the supply current harmonics [29]. This concept can be extended in this chapter by considering this nonlinear source as being a fictitious and continuously-varying controllable voltage source. This fictitious voltage source will provide an output waveform necessary to drive the required filter compensating current into the supply; hence removing the effects of the load current harmonics.

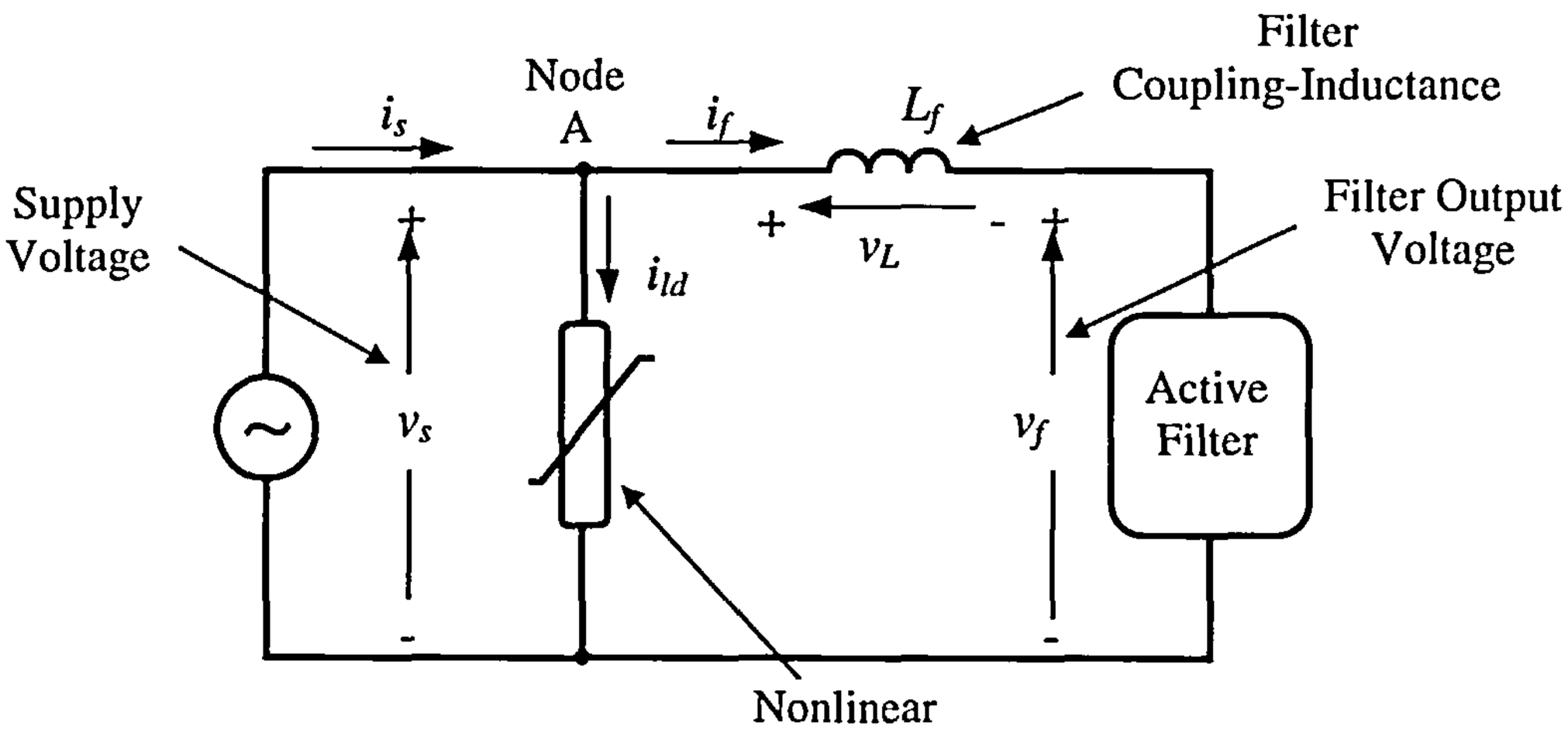



Fig.3.11 : General filter representation

### 3.4.1 Circuit representation

The PSPICE circuit representation of Fig.3.11 is shown here in Fig.3.12, where the nonlinear load is represented by two current-sources each operating during a mains half cycle and generating a square wave load current. On the other hand, the filter circuit is represented by three ideal current sources generating the required waveform to compensate the load current harmonics and generate the required sinusoidal supply current. Fig.3.13, shows the simulation results of this circuit on PSPICE. The upper traces show the filter, the load and the resulting supply current waveforms; while the lower graph represents the voltage waveforms of the supply and the filter output ($v_f$). $v_f$ is considered in this case to be the filter voltage waveform necessary to accomplish the compensation process. This voltage is presented here as a shifted sinusoidal waveform, which incorporates two voltage spikes of very high magnitudes.

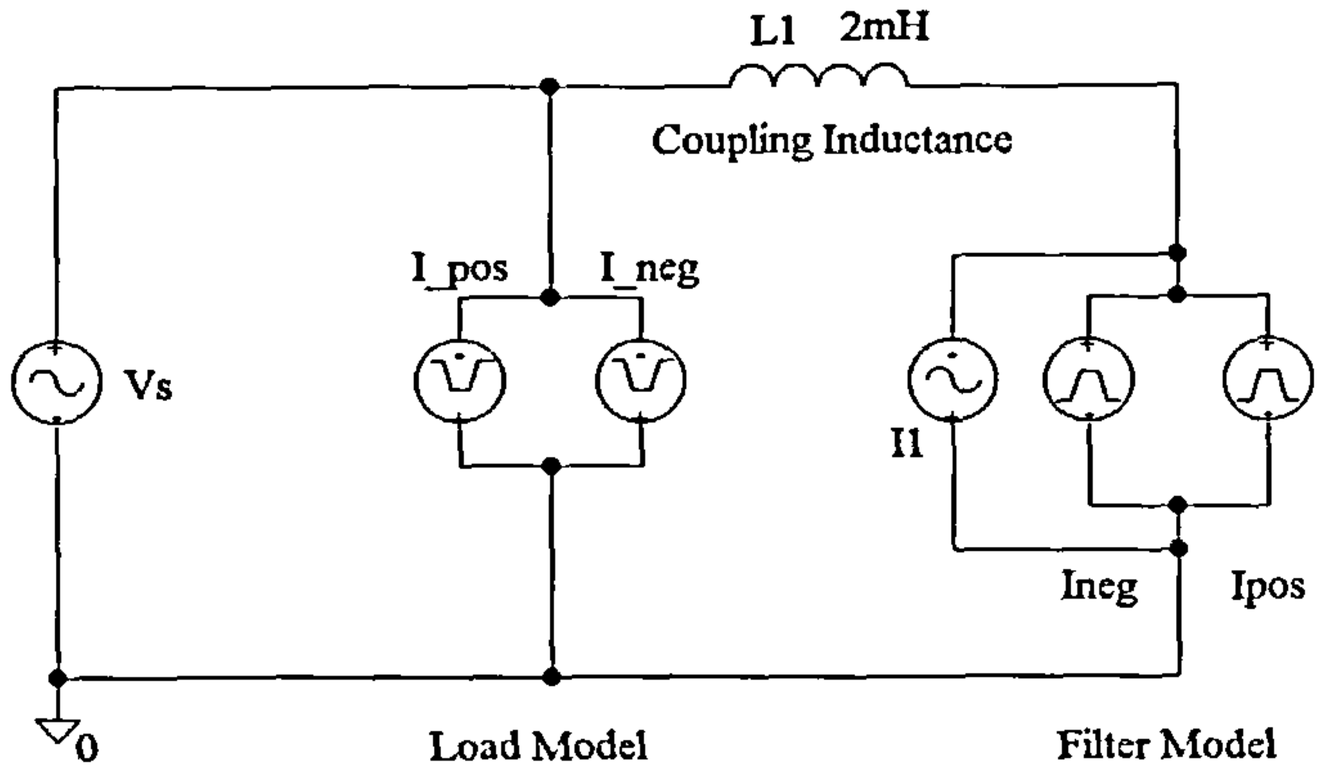



Fig.3.12 : PSCPICE representation of the filter system

These spikes can be related to the fact that for the inductor current to follow its reference, the inductor voltage has to be sufficiently high to perform this task. Of course, this severe case can never occur in practical power electronic circuits since currents can not take up such high rates of change. A more practical case can

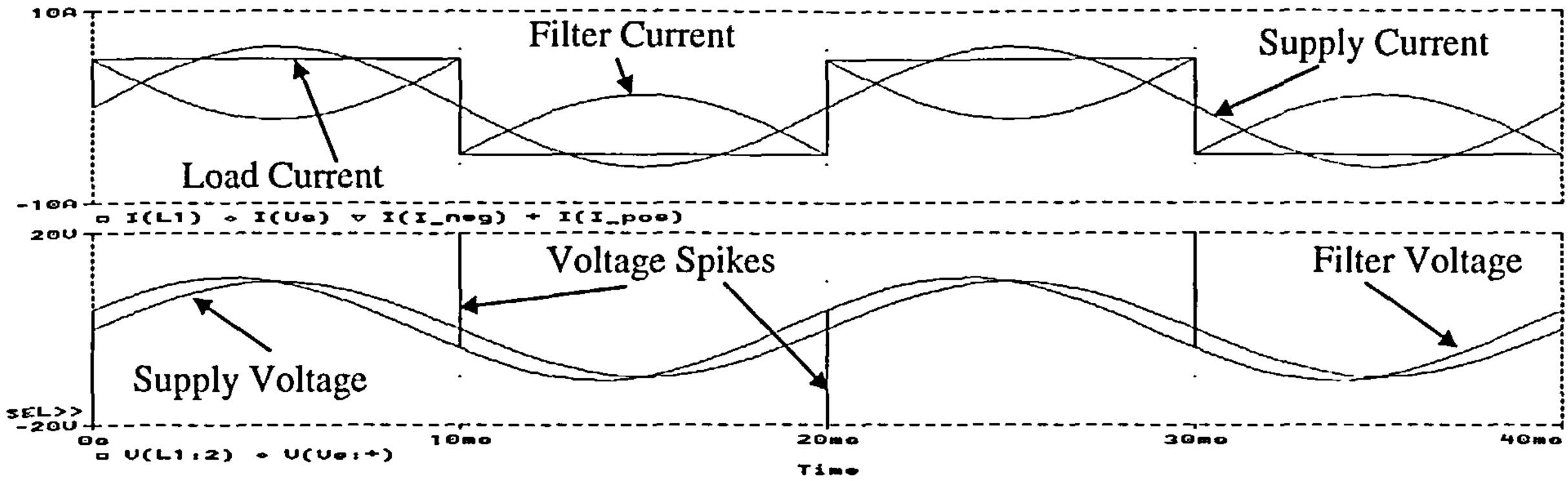



Fig.3.13 : Severe square wave loading condition

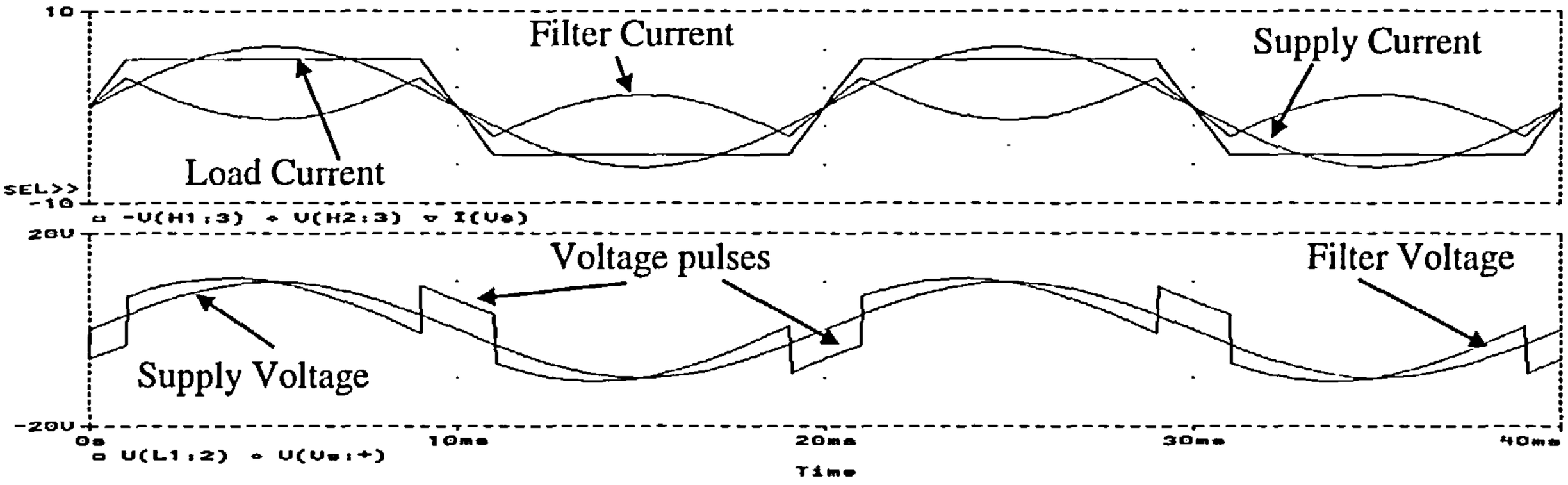



Fig.3.14 : Normal inductive loading condition

therefore be simulated by the waveforms of Fig.3.14, which shows the modified square wave load current, in addition to the other voltage and current waveforms of the system as above. The accompanying voltage waveforms are quite important due to the fact that they can be seen, for this case of a typical purely inductive square wave load current, as being a modified shifted sinusoidal waveform with superimposed pulses. It is worthwhile to note that the amount of energy supplied during the period of the superimposed pulses is proportional to the product of the pulse width and the square of its amplitude. The pulse width is in turn directly dependent upon the slope of the current harmonic signal at the same instant of time. This in fact dictates the limiting value of the operating frequency of the circuit used,

based upon the amount of controlling voltage available for the waveform manipulation process. If this voltage waveform is generated by any mean, the ultimate aim of achieving the optimum power active filter is then fulfilled.

### 3.4.2 Modelling equations of the generalised active filters

The analysis of the above model is quite simple. Considering the reference circuit diagram shown in Fig.3.11, we can write the following Kirchoff's voltage equation for the filter circuit

$$v_s = v_L + v_f \tag{3.2}$$

where,

$$v_L = L_f \frac{di_f}{dt} \tag{3.3}$$

Hence,

$$v_f = v_s - L_f \frac{di_f}{dt} \tag{3.4}$$

The load current is assumed to have the form

$$i_{ld} = i_1 + i_h \tag{3.5}$$

Applying Kirchoff's current law at node 'A' of the circuit,

$$i_s = i_{ld} + i_f \tag{3.6}$$

If it is assumed that the filter current in the above equation is the same as the reference harmonic current, i.e.,

$$i_f = -i_h \tag{3.7}$$

then compensation is achieved. This would result in the supply current containing no harmonics.

Following the above reasoning, it can be seen that by controlling the output voltage of the filter ( $v_f$ ) to follow the reference voltage calculated from equation (3.4), the filter would generate the required load current harmonics as imposed by equation (3.7).

From equation (3.4), it can be noted that the control variable in the equation is the rate of change of the reference current. The process of involving the derivative incorporation of the filter current is shown in [29] to give better performance compared with the case where the instantaneous value of the current is controlled without knowing the magnitude and polarity of its derivative. This way the control algorithm would incorporate the value of the rate of change of the reference current (which is the scaled version of the voltage across the filter inductor) that will predict the next expected change in the harmonic current magnitude and will react towards it. Implementing the above technique will cause a reduction in the switching frequency of the filter circuit.

## 3.5 Proposed Power Circuit

In order to reach a good design, it is highly recommended to start with identifying and defining the main requirements for the proposed circuit. This is performed in the next section, while the circuit layout and operation discussions follow.

### 3.5.1 Main requirements for the proposed circuit

The main criteria for an active filter can be identified as follows:

1. Inductors, capacitors and other components should be acceptable in sizes for a given application.

2. Low switching frequency to maintain acceptable losses.

3. Linear voltage control of the voltage at the filter output ( $v_f$ )

4. Use of the rate of change of the filter current in order to maintain a low switching frequency.

5. Better and faster synthesis of reference signal waveform

6. Easy on line control (without the need for optimisation)

7. The same circuit may be used for both harmonics compensation and reactive power control (as well as balancing three phase systems in the case of three phase configurations).

### 3.5.2 Circuit layout

The proposed power circuit configuration of the filter uses the same number of switches as single-phase inverter circuits. It, however, employs these switches in a completely different manner. As shown in Fig.3.15, the circuit consists mainly of four unidirectional power switches, two dc capacitors, one ac capacitor and two inductors.

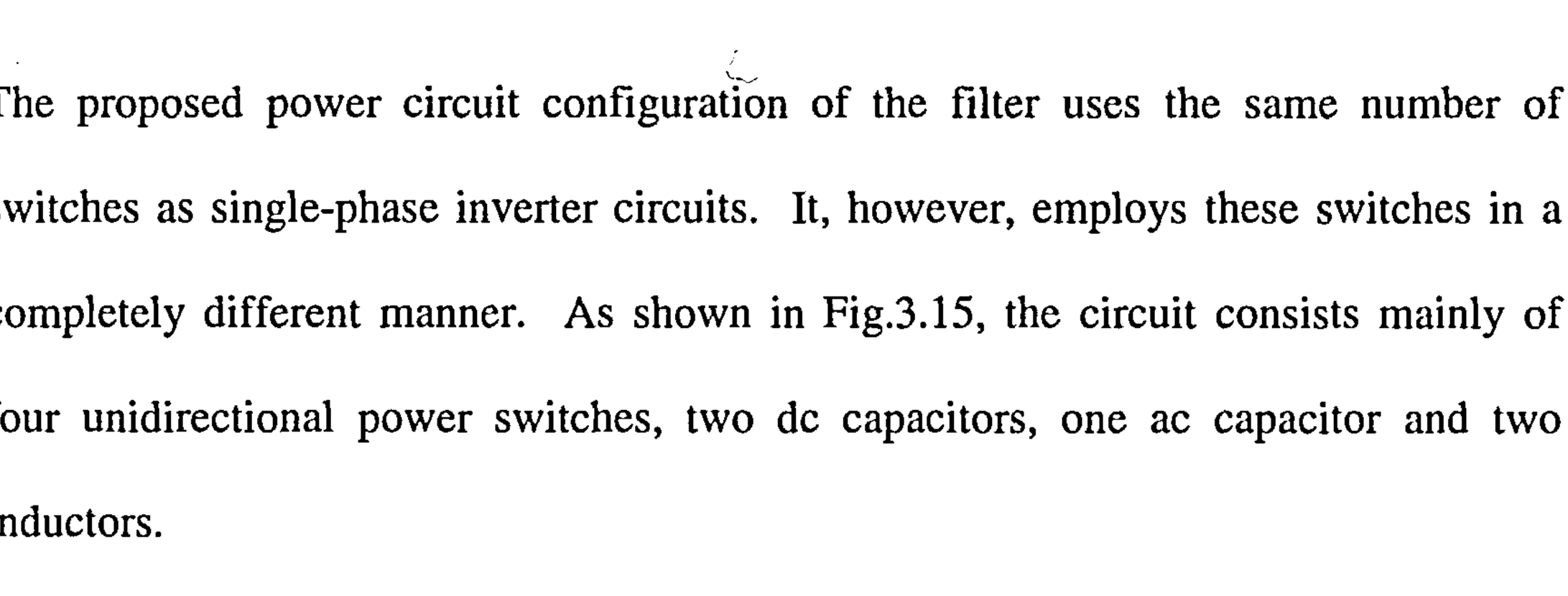


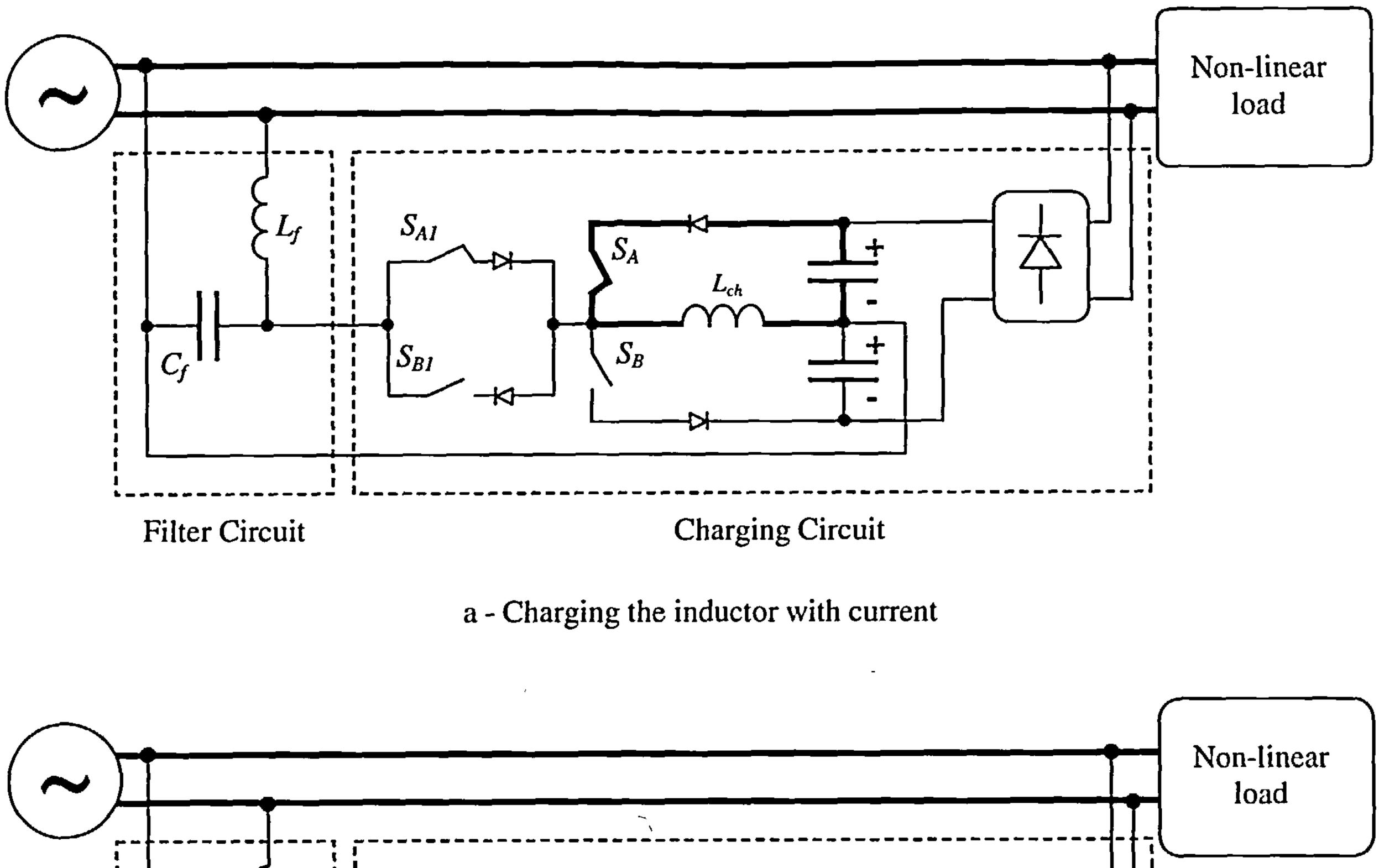

Fig.3.15 : Power circuit of the proposed active filter

### 3.5.3 Operating principle

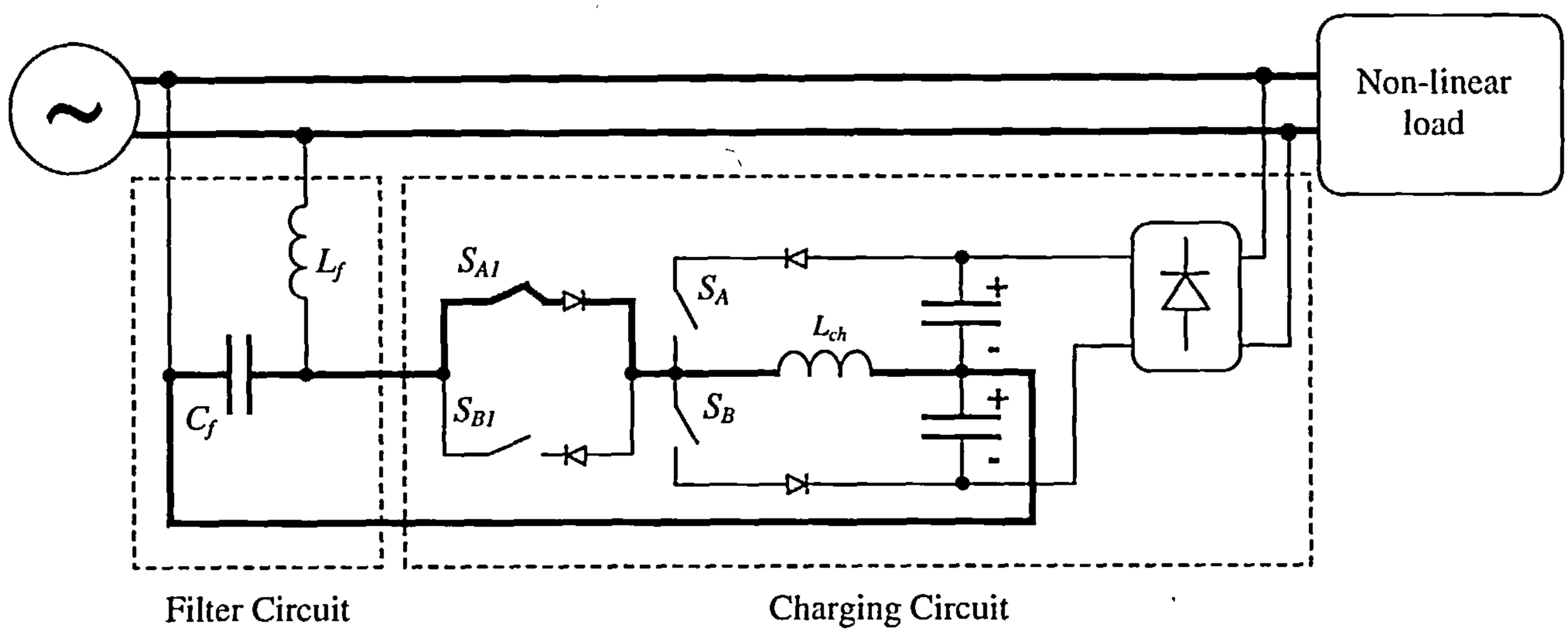
The dc capacitors, $C_{dc1}$ and $C_{dc2}$, can be charged from the supply via a diode rectifier bridge, providing a source of constant dc voltage which is used to supply the dc power needed by the circuit. The charging inductor, $L_{ch}$, is used to pump the charge to the main part of the circuit. This part consists of the filter Capacitor, $C_f$, which is charged with either a positive or a negative polarity with predetermined amplitudes to control the filter output voltage. This voltage is in turn applied across the filter inductor, $L_f$, to generate, in conjunction with the supply voltage, the filter current. This resulting current will conform to the reference current determined in order to eliminate the current harmonics in the load for this particular loading condition.

Thus, the filter capacitor, $C_f$, acquires the necessary and appropriate charge from the reservoir capacitors, $C_{dc1}$ and $C_{dc2}$. The stored energy in the filter capacitor will not be dissipated into the load in case of change of polarity; instead, it will be fed back to the other dc capacitor that will then be overcharged by this amount of energy. This implies that throughout a complete mains cycle, the charge on the two dc-capacitors will not be dissipated except for the only case of supplying the losses to the switches. Hence, these reservoir capacitors can have relatively small values (220 μF or less).

The two switches, $S_A$ and $S_B$, are modulated (6 kHz) to pump the required charge into the filter capacitor, which is of a relatively low value (40-80 μF). Fig.3.16 shows the charging and discharging processes of the inductor $L_{ch}$ and the capacitor $C_f$, which are demonstrated by the current paths (in thick lines) for a positive capacitor output voltage, using $S_A$ and $S_{A1}$. The filter inductance, $L_f$, connected between $C_f$ and the ac supply, acts as a coupling and smoothing inductor for the output filter current. It




a - Charging the inductor with current




b - Releasing the inductor current to charge the capacitor

Fig.3.16 : Current paths for the proposed power circuit

plays the same role as in any other filter configuration. For a negative capacitor output voltage, $S_B$ and $S_{B1}$ will have a similar role. The two switches, $S_{A1}$ and $S_{B1}$, are low-frequency switches (less than 1 kHz switching frequency) that decide the direction of the charging current flowing from the reservoir capacitor to the filter capacitor. The four switches act as a controllable-output, bipolar, bidirectional buck-

boost regulator, thereby performing the required role of a continuously controllable voltage source.

### 3.5.4 Exact model of the proposed circuit

From Fig.3.16, it can be noted that there exists four possible current paths for the proposed circuit in positive and negative modulation. In order to model the circuit mathematically, the number of possible modes of operation, can be figured out from the circuit diagram shown in Fig.3.17 (switches are represented by resistors), as well as by considering the fact that the switching system operates either positively or negatively at any instant of time. This implies that the positive and negative modulation switches ($S_A$ and $S_B$) or their direction counterparts ($S_{A1}$ and $S_{B1}$) would never operate simultaneously. This cuts down the possibilities by half from sixteen to become only eight. Two of these are in fact the same since they incorporate the cases when the positive and negative sets of switches ($S_A$ & $S_{A1}$ and $S_B$ & $S_{B1}$) are off respectively. In this way, we end up with seven different modes of operation, which

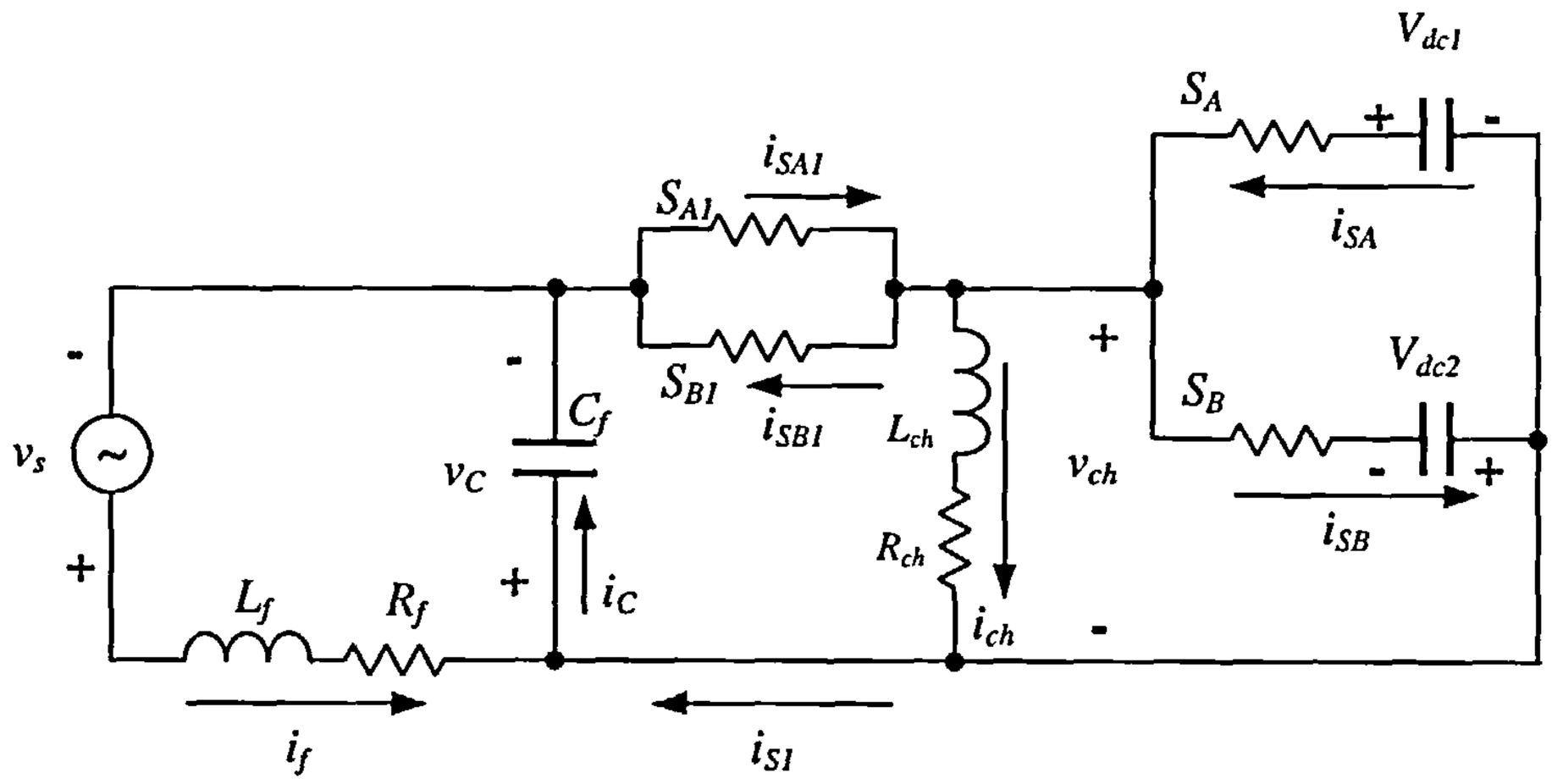



Fig.3.17 : Model of the proposed circuit

are discussed in the following subsections. It is worthwhile to note that some of the equations are identical between different modes. These are repeated here only for convenience.

**Mode A (All switches are OFF)**

This case, shown in Fig.3.18, applies as mentioned above to both the cases of positive and negative modulation when all switches are off. The circuit then reduces to a second order system with the following set of two first order differential equations

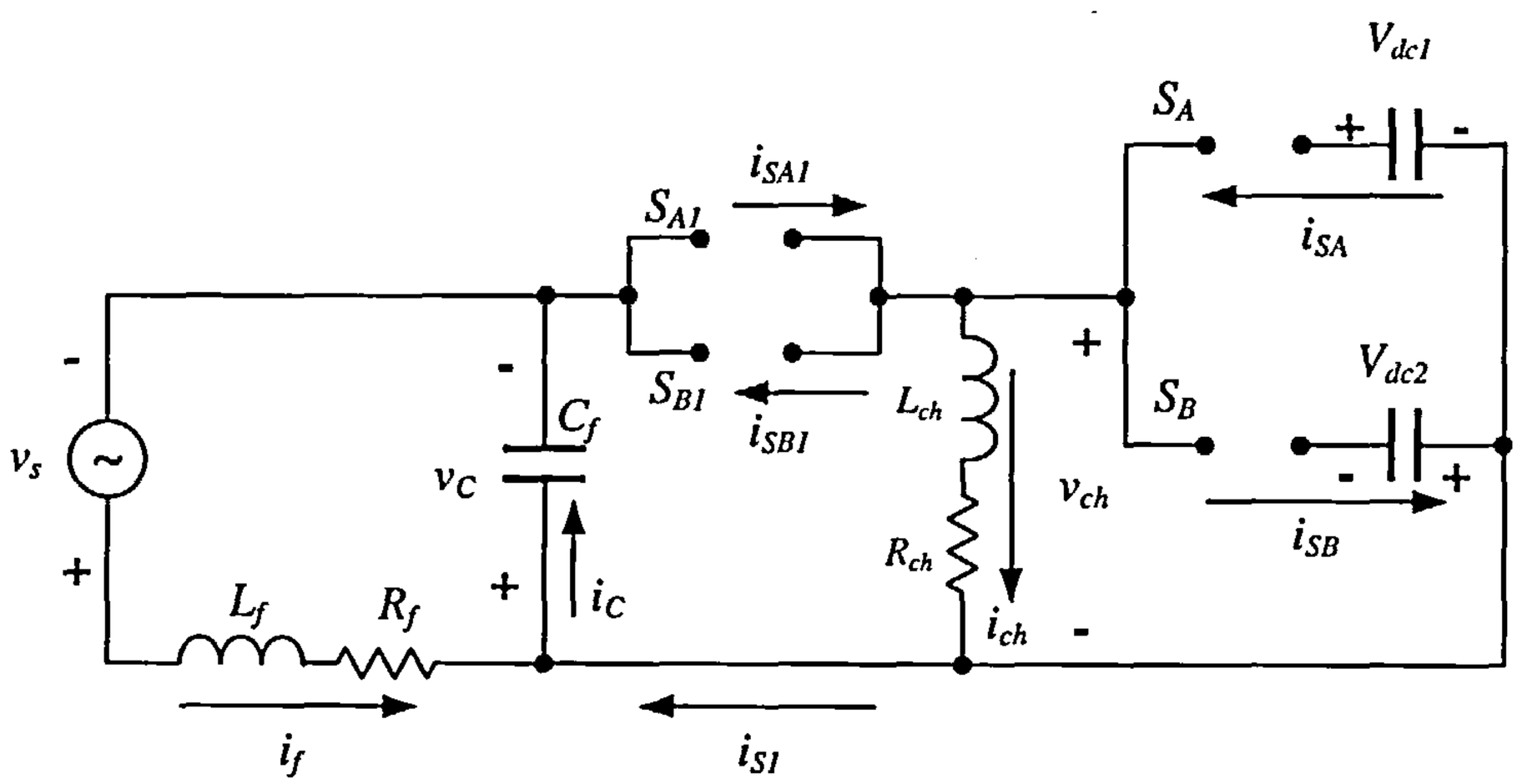



Fig.3.18 : Operation in mode A

$$\frac{di_f}{dt} = \frac{(v_s - v_c - R_f\, i_f)}{L_f} \tag{3.8}$$

$$\frac{dv_C}{dt} = \frac{i_f}{C_f} \tag{3.9}$$

The remaining system variables can then be solved for using the following linear equations

$$i_{ch} = i_{SA\,1} = i_{SB\,1} = i_{S\,1} = i_{SA} = i_{SB} = 0 \tag{3.10}$$

$$i_C = i_f \tag{3.11}$$

$$v_{ch} = 0 \tag{3.12}$$

## Mode B ($S_A$ is ON)

This case, shown in Fig.3.19, applies only to the case where only the positive modulation switch is on while all other switches are off. The circuit then reduces to a third order system with the following set of three first-order differential equations

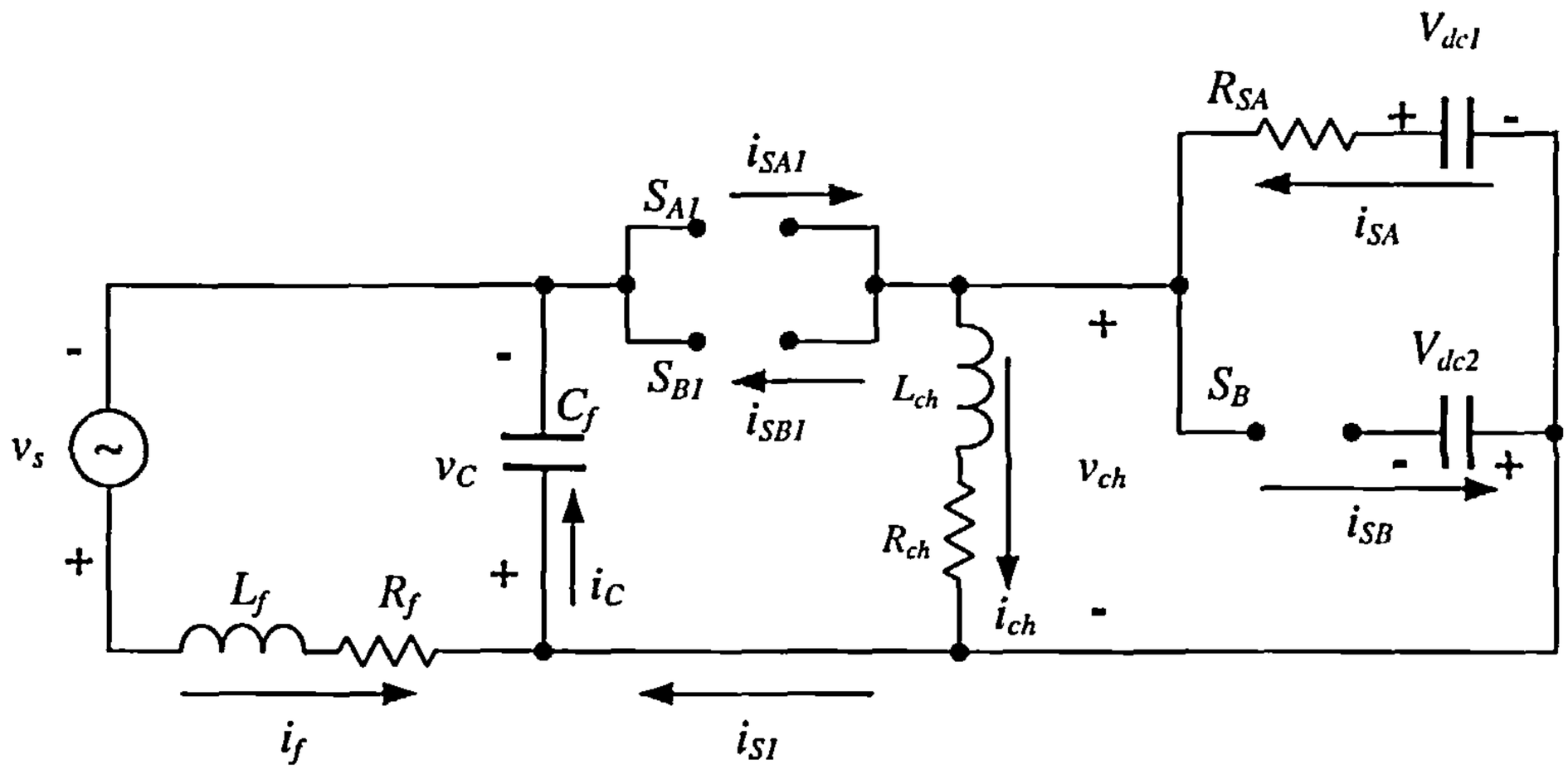



Fig.3.19 : Operation in mode B

$$\frac{di_f}{dt} = \frac{(v_s - v_c - R_f\, i_f)}{L_f} \tag{3.13}$$

$$\frac{dv_C}{dt} = \frac{i_f}{C_f} \tag{3.14}$$

$$\frac{di_{ch}}{dt} = \frac{(V_{dc1} - R_{SA}\, i_{ch} - R_{ch}\, i_{ch})}{L_{ch}} \tag{3.15}$$

The remaining system variables can then be solved for using the following linear equations

$$i_{SA1} = i_{SB1} = i_{S1} = i_{SB} = 0 \tag{3.16}$$

$$i_{SA} = i_{ch} \tag{3.17}$$

$$i_C = i_f \tag{3.18}$$

$$v_{ch} = V_{dc1} - R_{SA}\, i_{SA} \tag{3.19}$$

**Mode C ($S_B$ is ON)**

This case, shown in Fig.3.20, is the complement of the previous mode. It applies to the case where only the negative modulation switch is on while all other switches are off. The circuit then reduces to a third order system with the following set of three first-order differential equations

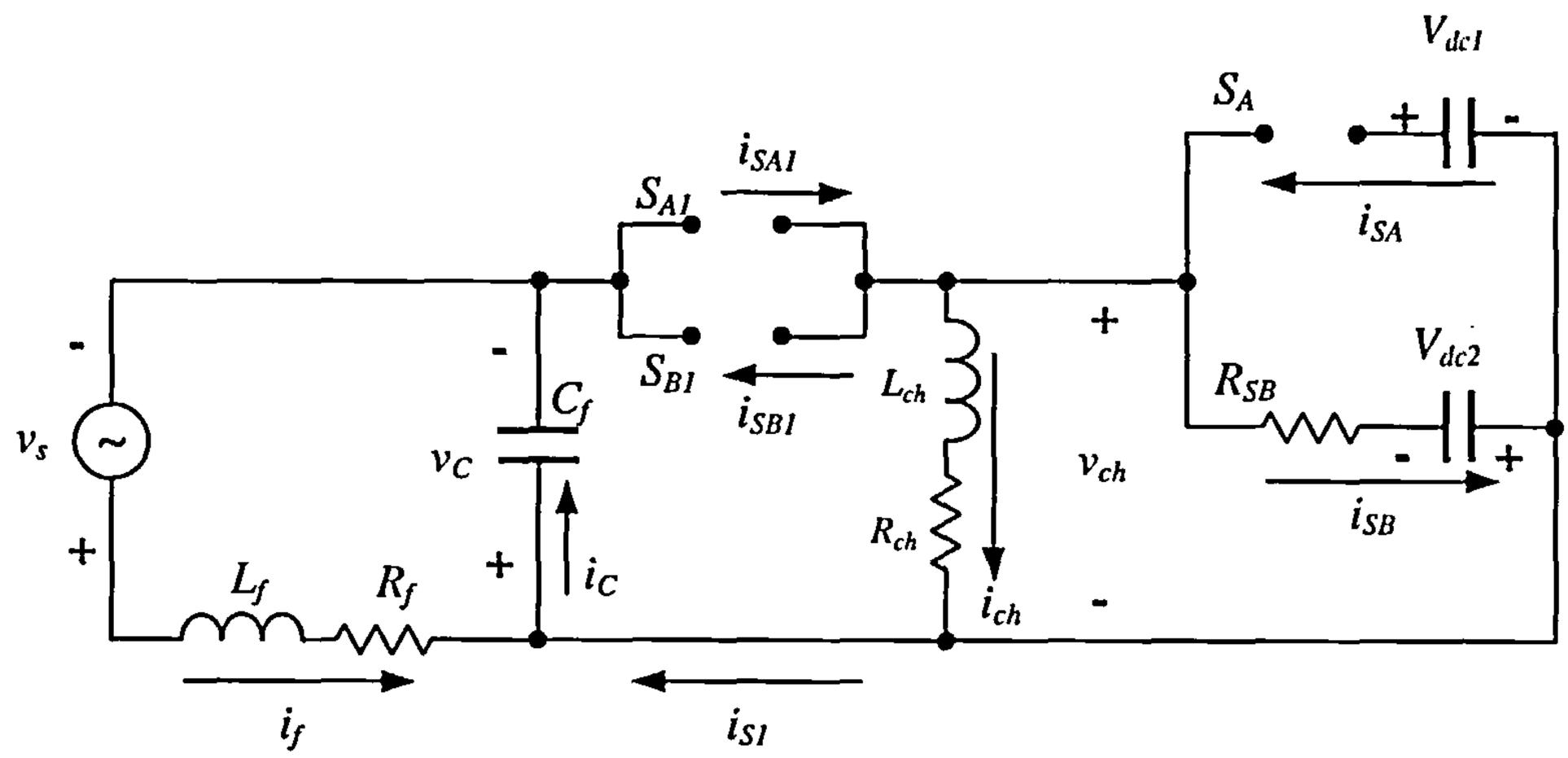



Fig.3.20 : Operation in mode C

$$\frac{di_f}{dt} = \frac{(v_s - v_c - R_f\, i_f)}{L_f} \tag{3.20}$$

$$\frac{dv_C}{dt} = \frac{i_f}{C_f} \tag{3.21}$$

$$\frac{di_{ch}}{dt} = \frac{(V_{dc2} - R_{SB}\, i_{ch} - R_{ch}\, i_{ch})}{L_{ch}} \tag{3.22}$$

The remaining system variables can then be solved for using the following linear equations

$$i_{SA1} = i_{SB1} = i_{S1} = i_{SA} = 0 \tag{3.23}$$

$$i_{SB} = -\, i_{ch} \tag{3.24}$$

$$i_C = i_f \tag{3.25}$$

$$v_{ch} = V_{dc2} + R_{SB}\, i_{SB} \tag{3.26}$$

**Mode D ($S_{A1}$ is ON)**

This case, shown in Fig.3.21, applies to the case where only the positive direction switch is on while all other switches are off. The circuit then reduces to a third order system with the following set of three first-order differential equations

$$\frac{di_f}{dt} = \frac{(v_s - v_c - R_f\, i_f)}{L_f} \tag{3.27}$$

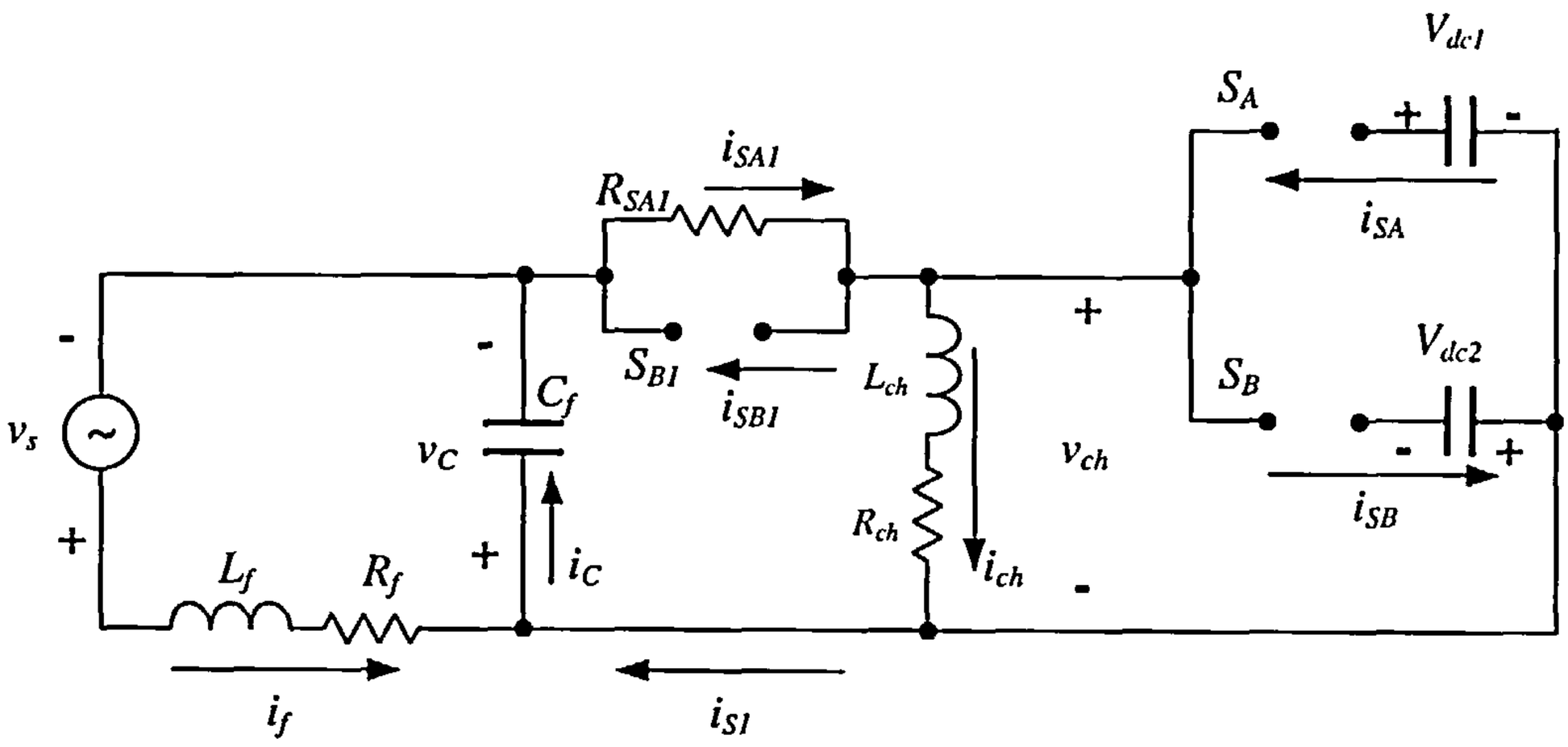



Fig.3.21 : Operation in mode D

$$\frac{dv_C}{dt} = \frac{(i_f + i_{ch})}{C_f} \tag{3.28}$$

$$\frac{di_{ch}}{dt} = \frac{(-v_C - R_{SA1}\, i_{ch} - R_{ch}\, i_{ch})}{L_{ch}} \tag{3.29}$$

The remaining system variables can then be solved for using the following linear equations

$$i_{SB1} = i_{SA} = i_{SB} = 0 \tag{3.30}$$

$$i_{SA1} = i_{ch} \tag{3.31}$$

$$i_{S1} = i_{SA1} \tag{3.32}$$

$$i_C = i_f + i_{S1} \tag{3.33}$$

$$v_{ch} = -v_C - R_{SA1}\, i_{SA1} \tag{3.34}$$

**Mode E ($S_{B1}$ is ON)**

This case, shown in Fig.3.22, applies to the case where only the negative direction switch is on while all other switches are off. The circuit then reduces to a third order system with the following set of three first-order differential equations

$$\frac{di_f}{dt} = \frac{(v_s - v_c - R_f\, i_f)}{L_f} \tag{3.35}$$

$$\frac{dv_C}{dt} = \frac{(i_f + i_{ch})}{C_f} \tag{3.36}$$

$$\frac{di_{ch}}{dt} = \frac{(-v_C - R_{SB1}\, i_{ch} - R_{ch}\, i_{ch})}{L_{ch}} \tag{3.37}$$

The remaining system variables can then be solved for using the following linear equations

$$i_{SA1} = i_{SA} = i_{SB} = 0 \tag{3.38}$$

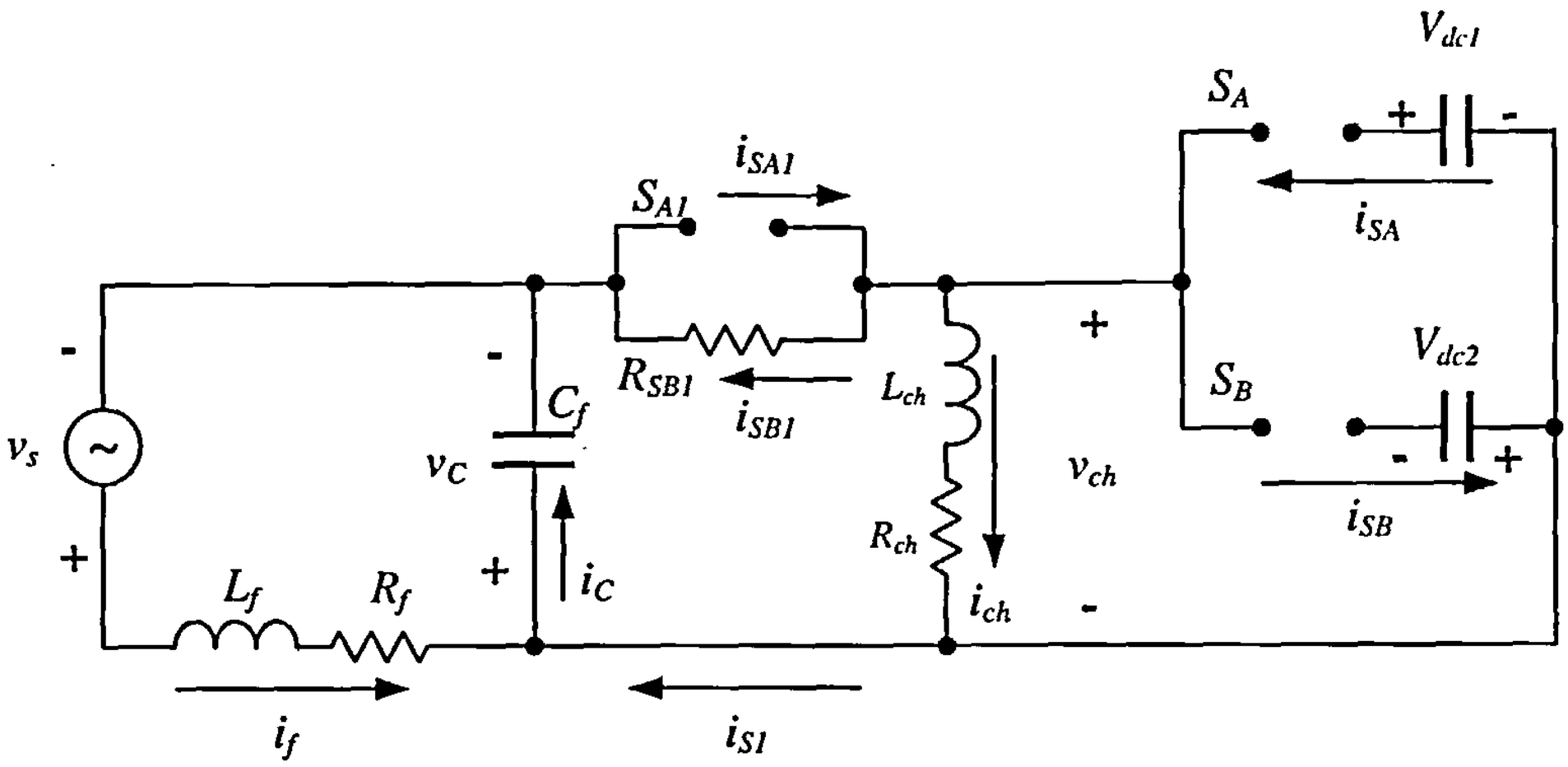



Fig.3.22 : Operation in mode E

$$i_{SB\,1} = - i_{ch} \tag{3.39}$$

$$i_{S\,1} = - i_{SB\,1} \tag{3.40}$$

$$i_C = i_f + i_{S\,1} \tag{3.41}$$

$$v_{ch} = - v_C + R_{SB\,1}\, i_{SB\,1} \tag{3.42}$$

**Mode F ($S_A$ and $S_{A1}$ are ON)**

This case, shown in Fig.3.23, applies to the case where both the positive modulation and direction switches are on while all other switches are off. The circuit then reduces to a third order system with the following set of three first-order differential equations

$$\frac{di_f}{dt} = \frac{(v_s - v_c - R_f\, i_f)}{L_f} \tag{3.43}$$

$$\frac{dv_C}{dt} = \frac{i_f}{C_f} - \frac{(V_{dc1} + v_C - R_{SA}\, i_{ch})}{C_f\,(R_{SA} + R_{SA\,1})} \tag{3.44}$$

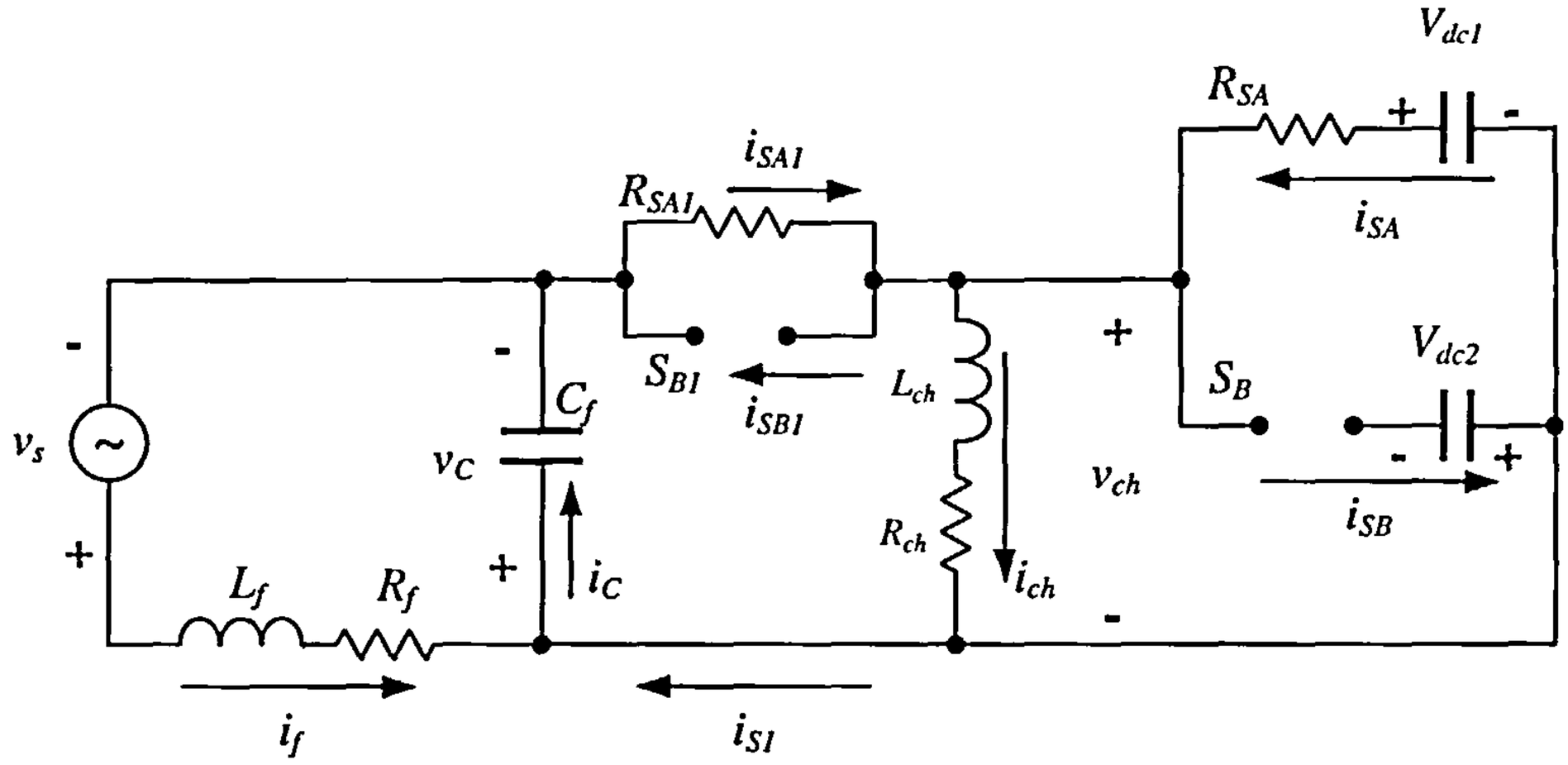



Fig.3.23 : Operation in mode F

$$\frac{di_{ch}}{dt} = \frac{(V_{dc1}\, R_{SA\,1} - v_C\, R_{SA} - (R_{SA\,1}\, R_{ch} + R_{SA}\, R_{SA\,1} + R_{ch}\, R_{SA})\, i_{ch})}{L_{ch}\,(R_{SA} + R_{SA\,1})} \quad (3.45)$$

The remaining system variables can then be solved for using the following linear equations

$$i_{SB\,1} = i_{SB} = 0 \quad (3.46)$$

$$i_{SA\,1} = \frac{(-V_{dc1} - v_C + R_{SA}\, i_{ch})}{(R_{SA} + R_{SA\,1})} \quad (3.47)$$

$$i_{S\,1} = i_{SA\,1} \quad (3.48)$$

$$i_{SA} = i_{ch} - i_{S\,1} \quad (3.49)$$

$$i_C = i_f + i_{S\,1} \quad (3.50)$$

$$v_{ch} = V_{dc1} - R_{SA}\, i_{SA} \quad (3.51)$$

**Mode G ($S_B$ and $S_{B1}$ are ON)**

This case, shown in Fig.3.24, applies to the case where both the negative modulation and direction switches are on while all other switches are off. The circuit then

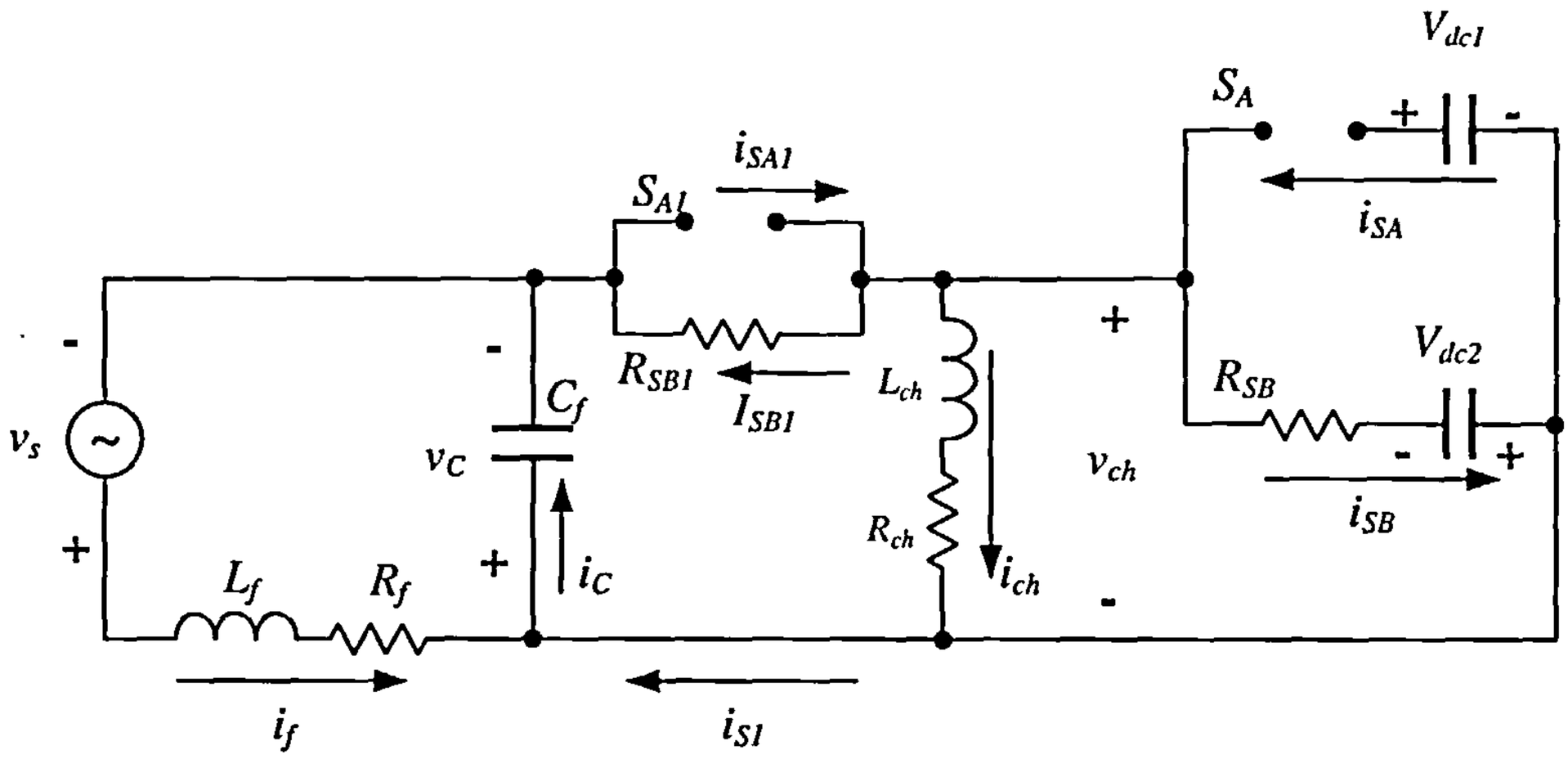



Fig.3.24 : Operation in mode G

reduces to a third order system with the following set of three first-order differential equations

$$\frac{di_f}{dt} = \frac{(v_s - v_c - R_f\, i_f)}{L_f} \tag{3.52}$$

$$\frac{dv_C}{dt} = \frac{i_f}{C_f} - \frac{(V_{dc2} + v_C - R_{SB}\, i_{ch})}{C_f\,(R_{SB} + R_{SB\,1})} \tag{3.53}$$

$$\frac{di_{ch}}{dt} = \frac{(V_{dc2}\, R_{SB\,1} - v_C\, R_{SB} - (R_{SB\,1}\, R_{ch} + R_{SB}\, R_{SB\,1} + R_{ch}\, R_{SB})\, i_{ch})}{L_{ch}\,(R_{SB} + R_{SB\,1})} \tag{3.54}$$

The remaining system variables can then be solved for using the following linear equations

$$i_{SA\,1} = i_{SA} = 0 \tag{3.55}$$

$$i_{SB\,1} = \frac{(-V_{dc2} + v_C - R_{SB}\, i_{ch})}{(R_{SB} + R_{SB\,1})} \tag{3.56}$$

$$i_{S\,1} = -\, i_{SB\,1} \tag{3.57}$$

$$i_{SB} = -\, i_{ch} + i_{S\,1} \tag{3.58}$$

$$i_C = i_f + i_{S\,1} \tag{3.59}$$

$$v_{ch} = V_{dc2} + R_{SB}\ i_{SB} \tag{3.60}$$

### 3.5.5 Parameter determination

The criteria for the determination of the component values are based on two main factors. These are namely, the switching frequency of the charging circuit and the response time of the filter. The former factor decides the optimal values of the charging inductor, $L_{ch}$, and the filter capacitor, $C_f$, depending on the charging and discharging times of the circuit formed by $C_{dc1}$, $S_A$ and $L_{ch}$ for the charging process. The discharging process takes place in the circuit formed by the loop $L_{ch}$, $S_{A1}$ and $C_f$. The internal resistive losses in the capacitors and the inductor must be chosen to be as minimum as possible. The on-resistances of the switches contribute a great deal to this process, which should normally be taken into consideration for the calculations of the time constants of the two cases.

The other factor of influence on the circuit parameters is the filter capacitor, $C_f$, in addition to the filter inductance, $L_f$. The time constant is then determined by the maximum response time of the capacitor discharging process. This is at least double the maximum frequency to be eliminated in the load current. Care should also be taken to select the resonant frequency as far as possible from the switching and the supply frequencies. The necessary approximate equations for analysing the parameter values are presented in the following analysis.

### 3.5.5.1 Approximate equations

To determine the magnitudes of the circuit components, a simplified model of the filter can be analysed as in the following paragraphs. The equations derived serve as guidelines for choosing the component values of the power circuit. The following general assumptions apply:

- System is lossless
- Switches are ideal
- Critically continuous current in the inductor is assumed
- The voltage across $C_f$ is assumed to be linear during charging (neglect $L_{ch}$)
- The voltage across $C_f$ is assumed to be linear during discharging (neglect $L_f$)
- Severest loading conditions are applied ($I_f{}^{max}$ is considered constant)
- DC link voltage is assumed constant during a typical switching cycle

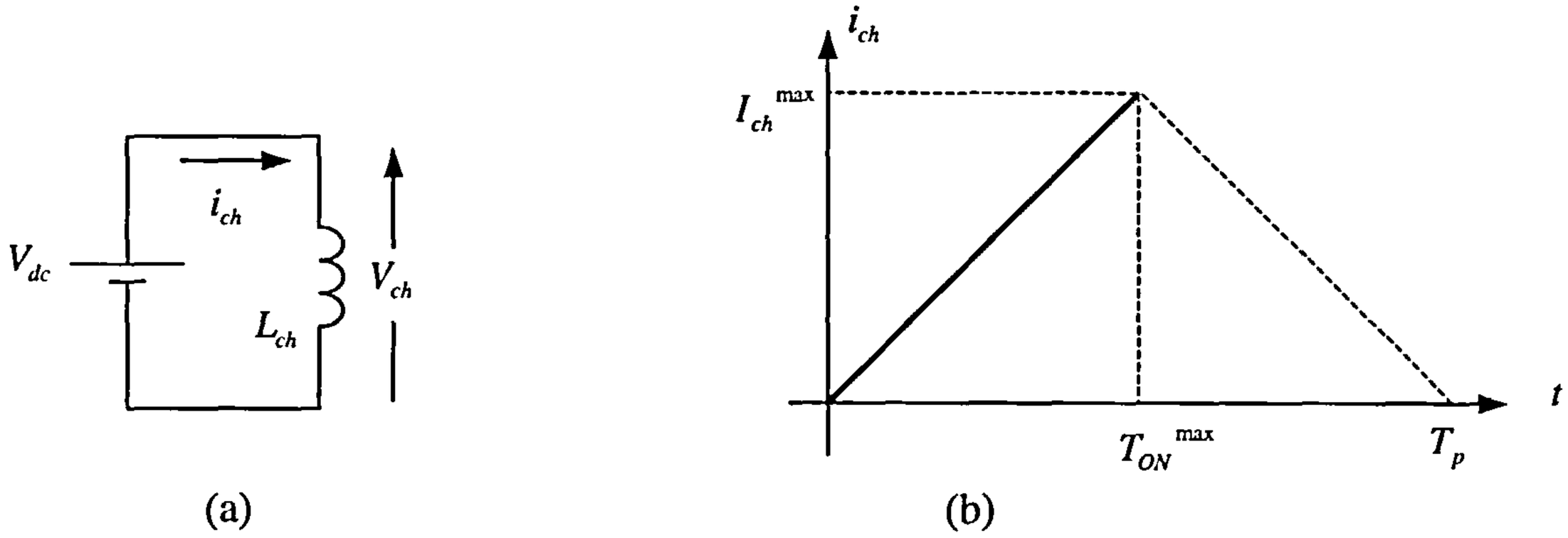



Fig.3.25 : Inductor charging circuit

Consider the charging period from $t = 0$ to $t = T_{ON}{}^{max}$, shown in Fig.3.25,

$$V_{dc} \approx L_{ch} \frac{di_{ch}}{dt} \tag{3.61}$$

hence,

$$L_{ch} \approx \frac{V_{dc}\,\Delta t}{\Delta i_{ch}} \tag{3.62}$$

Assuming the charging current to be linear as shown in Fig.3.25-b

$$L_{ch}^{\min} \approx \frac{V_{dc}\,T_{ON}^{\max}}{I_{ch}^{\max}} \tag{3.63}$$

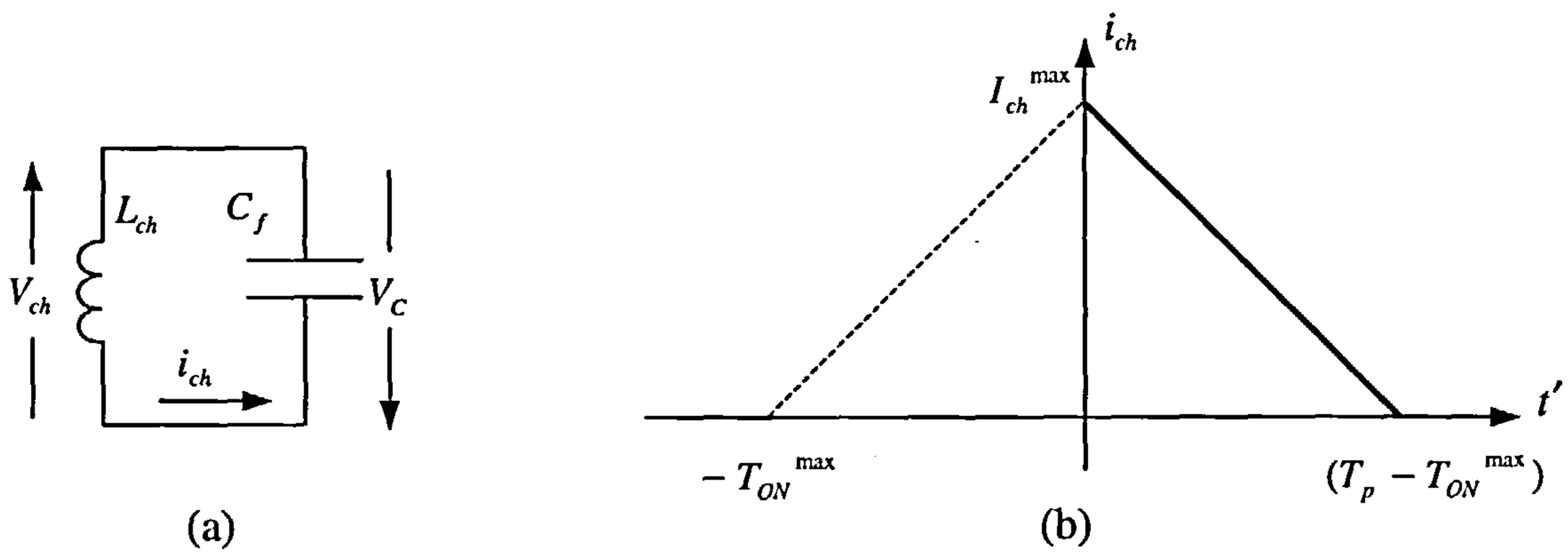



Fig.3.26 : Capacitor charging circuit

Consider the discharging period, Fig.3.26.

$$i_{ch} \approx C_f \frac{dv_C}{dt'} \tag{3.64}$$

which can be rewritten as

$$\Delta V_C^{tot} \approx \frac{1}{C_f} \int_0^{(T_p - T_{ON}^{\max})} i_{ch}\, dt' \tag{3.65}$$

and the inductor current, as in Fig.3.26-b, can be expressed as

$$i_{ch} \approx I_{ch}^{\max} \left( 1 - \frac{t'}{(T_p - T_{ON}^{\max})} \right) \tag{3.66}$$

Substituting (3.66) into (3.65) and integrating, yields,

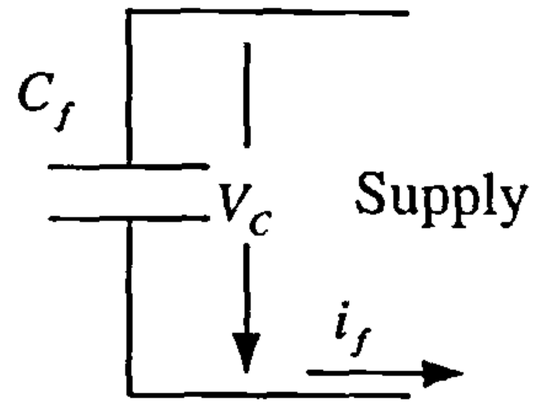



Fig.3.27 : Capacitor discharging circuit

$$C_f{}^{\max} \approx \frac{1}{2} \cdot \frac{I_{ch}{}^{\max}}{\Delta V_C{}^{tot}} \cdot \left(T_p - T_{ON}{}^{\max}\right) \tag{3.67}$$

During the discharge of $C_f$ into $L_f$, Fig.3.27,

$$i_f \approx C_f \frac{dv_C}{dt} \tag{3.68}$$

Assuming the load current during this short period to be constant at its maximum value ($I_f{}^{\max}$)

$$C_f{}^{\max} \approx \frac{I_f{}^{\max} \cdot T_p}{\Delta V_C{}^{drop}} \tag{3.69}$$

which simplifies to

$$I_f{}^{\max} \approx \frac{C_f{}^{\max} \cdot \Delta V_C{}^{drop}}{T_p} \tag{3.70}$$

The above equation determines the maximum allowable filter current fed back into the supply. In certain cases the magnitude of $I_f{}^{\max}$ is known. This can be treated by eliminating $C_f{}^{\max}$ from equations (3.67) and (3.69); then substituting the result into equation (3.63) to obtain the following relation necessary to calculate $L_{ch}{}^{\min}$.

$$L_{ch}{}^{\min} \approx \frac{V_{dc}}{2} \cdot \frac{T_{ON}{}^{\max}}{I_f{}^{\max}} \cdot \frac{\left(T_p - T_{ON}{}^{\max}\right)}{T_p} \cdot \frac{\Delta V_C{}^{drop}}{\Delta V_C{}^{tot}} \tag{3.71}$$

The value of $C_f{}^{max}$ can then be calculated from equation (3.69).

To determine the value of $L_f$, consider the circuit diagram shown in Fig.3.28. Under such a condition

$$v_s - v_C \approx L_f \frac{di_f}{dt} \tag{3.72}$$

The criterion for determining the maximum value of $L_f$ is to define the maximum rate of change of current for the maximum voltage across the inductor terminals, yielding

$$L_f{}^{max} \approx \frac{V_s{}^{max} + V_C{}^{max}}{\left(\frac{di_f}{dt}\right)_{max}} \tag{3.73}$$

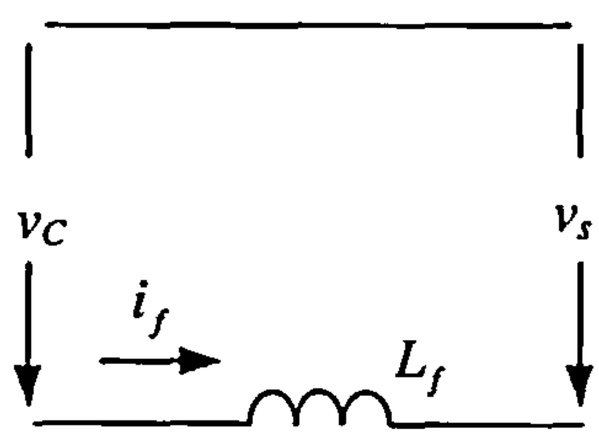



Fig.3.28 : Output filtering inductance

It is essential to ensure that no resonance is associated with $L_{ch}$ and $C_f$. The resonant angular frequency is given by

$$\omega_{r1} = \frac{1}{\sqrt{L_{ch}\, C_f}} \tag{3.74}$$

This value of resonance frequency ( $f_{r1} = 1/T_{r1}$ ) is related to the period of operation ($T_p - T_{ON}{}^{max}$) of this equivalent circuit as shown in Fig.3.26 and by the following expression

$$T_{r1} = \frac{2\pi}{\omega_{r1}} = 2\pi\sqrt{L_{ch}\,C_f} >> \left(T_p - T_{ON}{}^{\max}\right) \tag{3.75}$$

i.e., $$L_{ch}\,C_f >> \frac{\left(T_p - T_{ON}{}^{\max}\right)^2}{4\pi^2} \tag{3.76}$$

Similarly, to avoid the effect of resonance between the filter capacitor and the filter inductor at the switching frequency,

$$L_f\,C_f >> \frac{T_p{}^2}{4\pi^2} \tag{3.77}$$

Finally, to avoid the effect of resonance between the filter capacitor and the filter inductor at the supply frequency,

$$L_f\,C_f << \frac{T_s{}^2}{4\pi^2} \tag{3.78}$$

The above equations provide the necessary guidelines to determine the circuit parameters. The actual components used in the system may differ slightly from the calculated ones due to nonlinearities, which are not considered in the above analysis.

### 3.5.5.2 Component magnitudes

The calculation of the component magnitudes reduces now to the simple task of substituting into the above equations. This is performed in the following few lines. For a filter system of the proposed type with a dc link voltage of 300 Volts and a switching frequency of 6 kHz ($T_p = 166.6\,\mu\text{sec}$), it can be assumed that the maximum loading current of the filter is around 5 Amps. For a symmetrical charging and discharging subcycle, the value of the on-time is taken to be 83.33 μsec. It is assumed that the allowable percentage voltage drop due to loading is approximately

5% of the dc link voltage magnitude and that the charging capability of the filter is around 10% per subcycle ($T_p$). The output circuit is also assumed to be able to reverse the current magnitude within one switching subcycle. Substituting the above into equations (3.71), (3.69) and (3.73), it is found that

$$L_{ch}^{\min} \approx 0.6\,mH \qquad \text{(16.16 Amp rms)}$$

$$C_f^{\max} \approx 55\,\mu F \qquad \text{(640 Volts peak and 10 Amp peak ripple current)}$$

$$L_f^{\max} \approx 10\,mH \qquad \text{(5 Amp peak)}$$

It is worthwhile to note that the magnitude of the filter inductance is quite large compared to the values normally used in practical cases. These values are normally in the range of 3 to 5 mH. It is also important to note that these component magnitudes are merely presented here as guidelines for the choice of the optimal values which are normally improved by further trial and error during the simulation and the practical implementations.

The equations, proved above, are used to check the resonance frequencies as in:

Equation (3.76) $\quad 3.3 \times 10^{-8} \gg 1.76 \times 10^{-10}$

Equation (3.77) $\quad 5.5 \times 10^{-7} \gg 7.04 \times 10^{-10}$

Equation (3.78) $\quad 5.5 \times 10^{-7} \ll 1.01 \times 10^{-5}$

The above inequalities hold for all the cases with around two orders of magnitudes, which proves that the estimated values are far from resonance bands. This ensures a safe operation of the circuit.

## 3.6 Frequency response analysis of the proposed system

The frequency response analysis is only intended for linear bilateral and time invariant systems, which can be analysed analytically using ordinary Fourier techniques. These techniques are not intended for nonlinear systems with switching devices. This implies that for systems incorporating different time varying switching states, the modelling would not be straightforward. However by linearising the system around a certain mid-range operating point, the approximate frequency analysis can be performed. The case presented here for the proposed system lies under this category. The system frequency domain analysis is presented in the following subsections.

### 3.6.1 Simulated frequency response

Another view of the active filter can be studied by interpreting the block diagram representing the basic idea of active filters shown in Fig.3.29. One can note that the power circuit of the active filter is mainly operating as a power amplifier, while the control system in this case is mainly concerned with generating a reference signal. The switching control circuit is now incorporated inside the power amplifier block itself in conjunction with the PWM control. The switching power amplifier, as it is normally termed in these cases, uses the same power circuit proposed above for the active filter to generate an amplified replica of the voltage reference across the output capacitor.

The proposed power amplifier circuit, in conjunction with an open loop control implementation of the system, was simulated with a dedicated Pascal program, using the same modelling equations outlined earlier (section 3.5.4) for the active filter

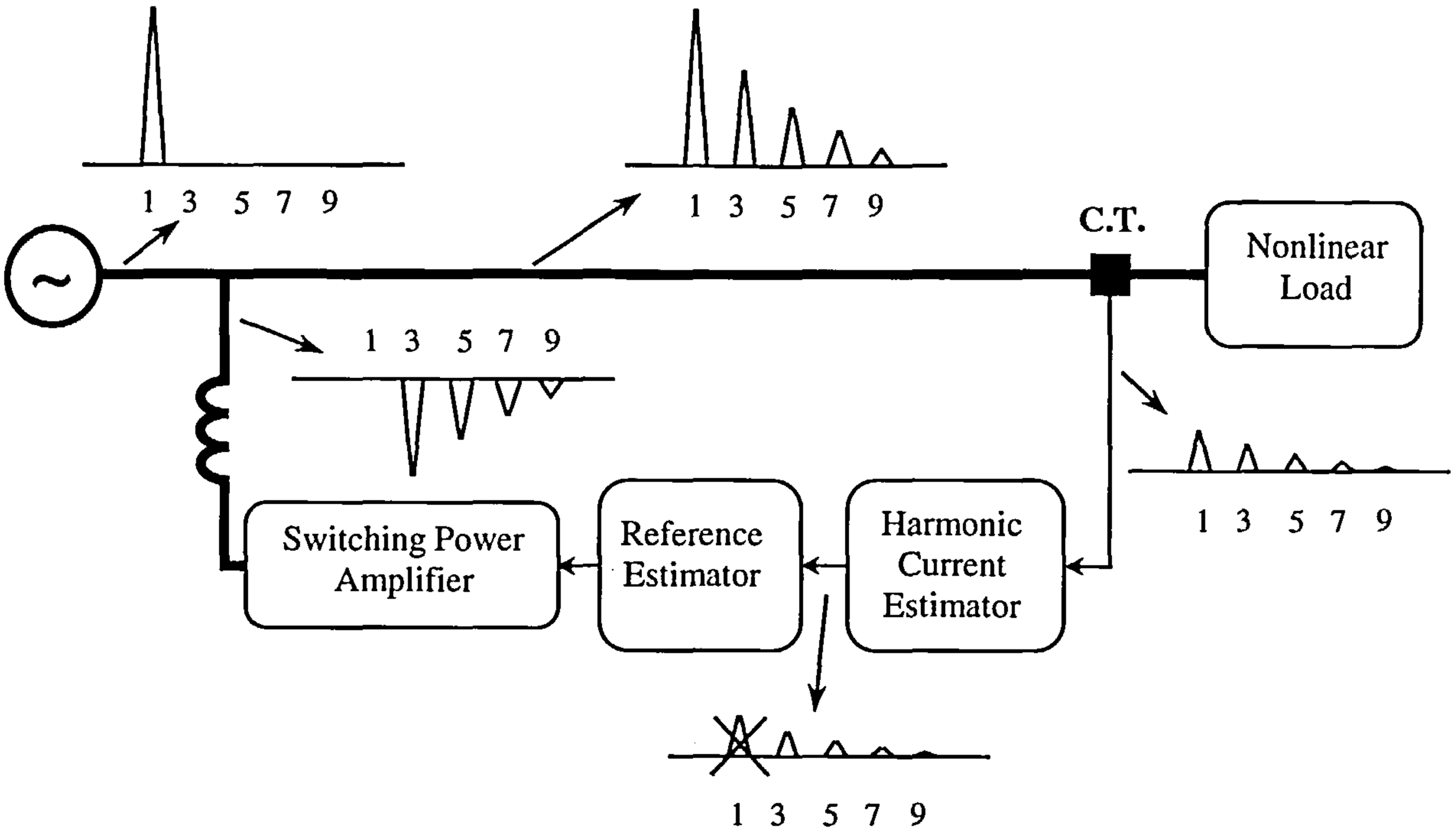
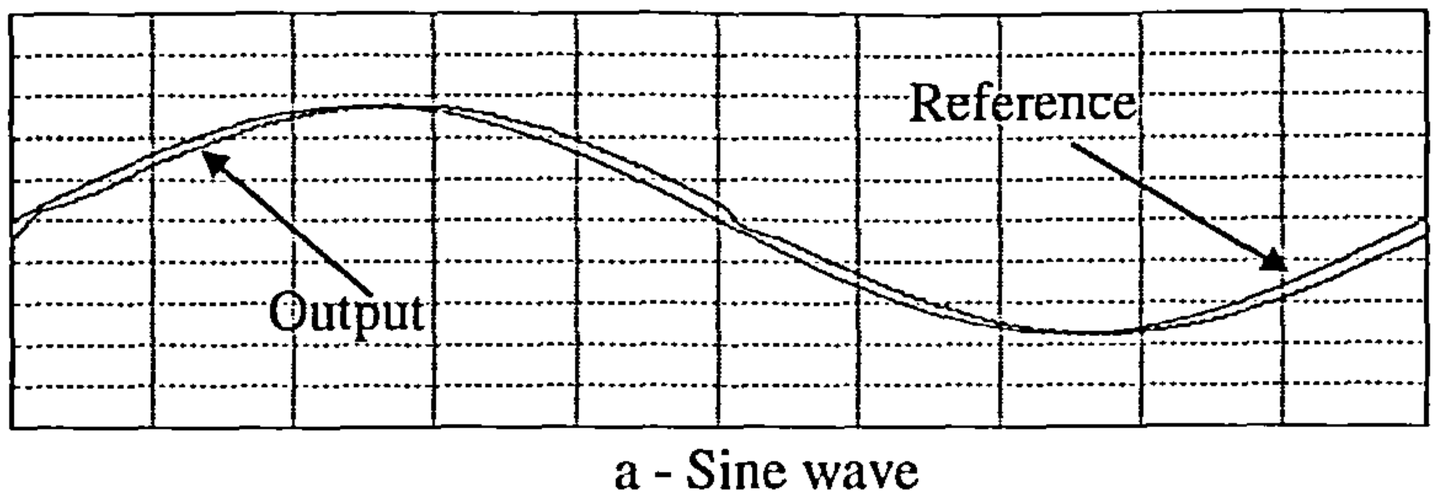


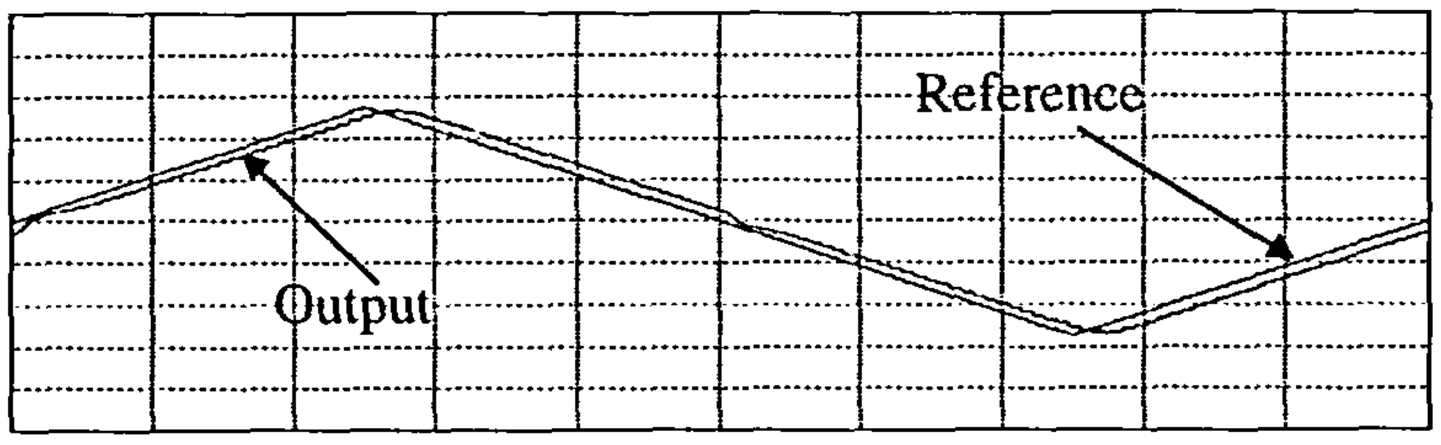

Fig.3.29 : Interpretation of active filter performance

performance. The simulation results are observed for the three cases of a sinusoidal, triangular and square wave references and outputs are presented in Fig.3.30. The open loop frequency response of the system can then be modelled by changing the frequency of a purely sinusoidal reference applied at the input terminals of the switching amplifier block as shown in Fig.3.31. The output of this block is the amplified signal. The average magnitude ratios and phase angle differences are recorded. The corresponding frequency response Bode plot is shown in Fig.3.32 with the solid lines.

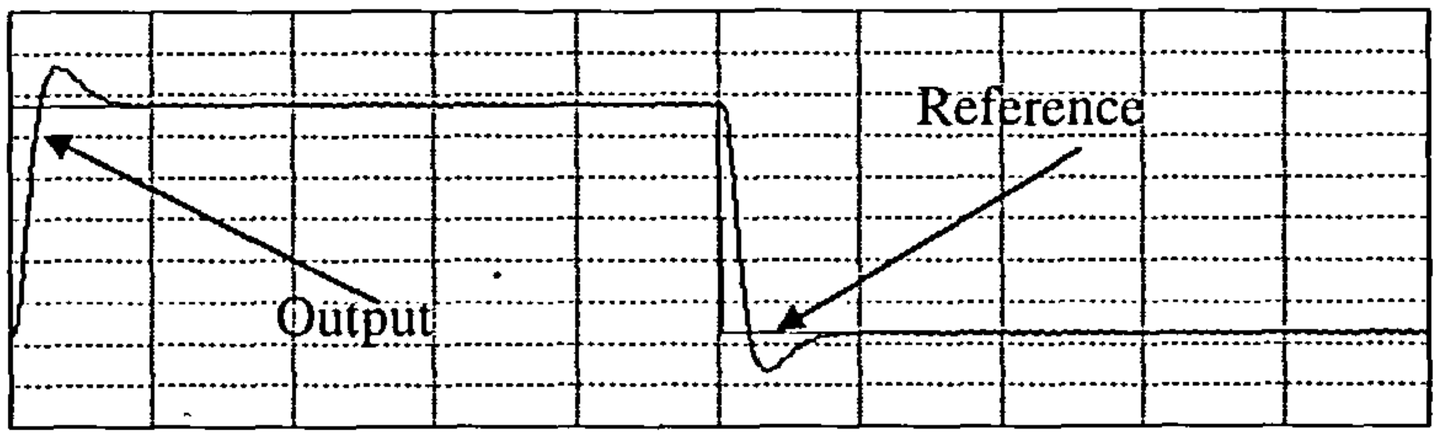
The results show that the system performance is acceptable from the bandwidth point of view. The 3 db bandwidth of the system is over 2 kHz, which is high enough compared to the rated 50 Hz operating frequency. This value is considered good from the point of view of a power amplifier. However, the phase shift incorporated at this




a - Sine wave




b - Triangular wave




c - Square wave

Fig.3.30 : Performance of the open loop switching amplifier

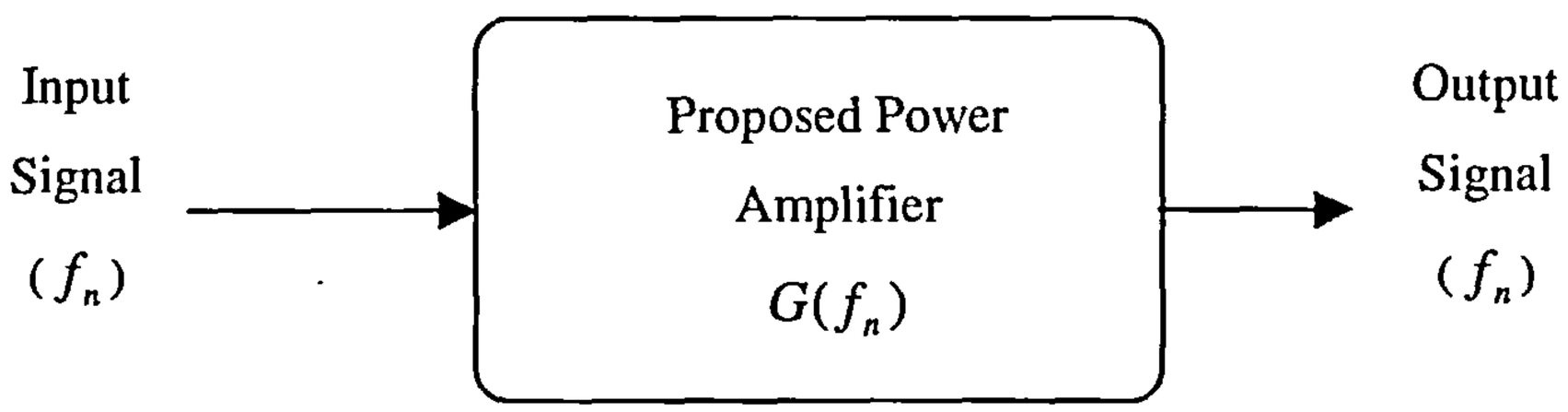
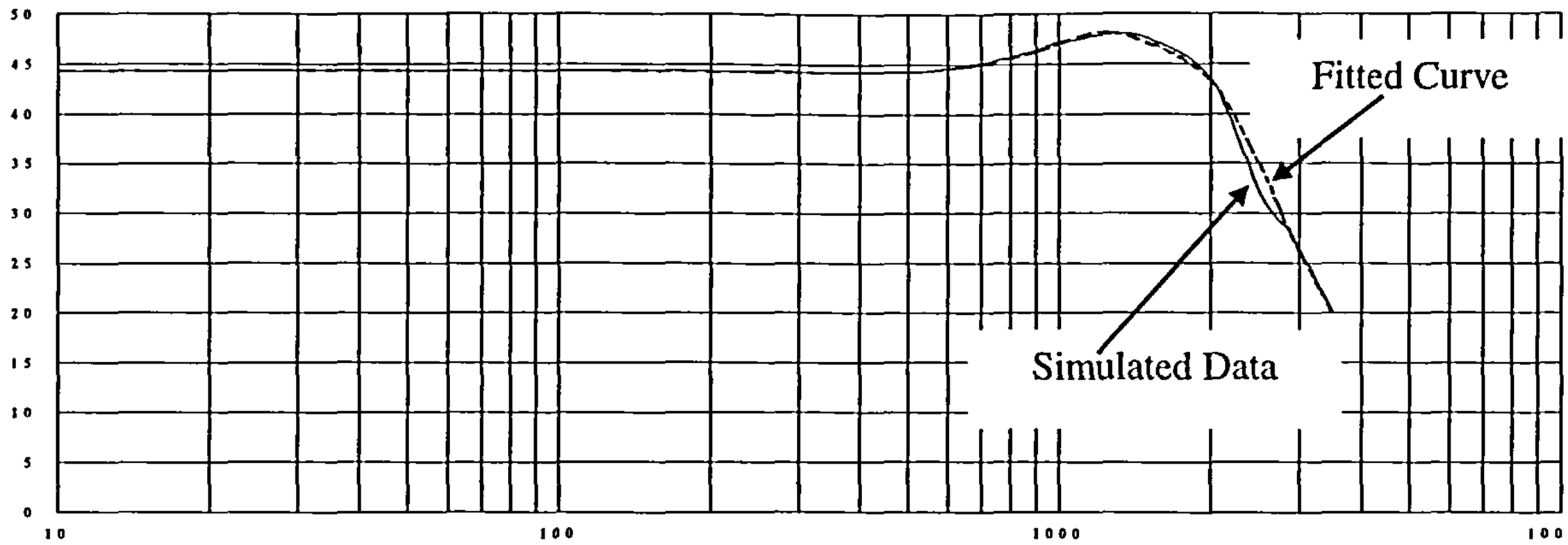
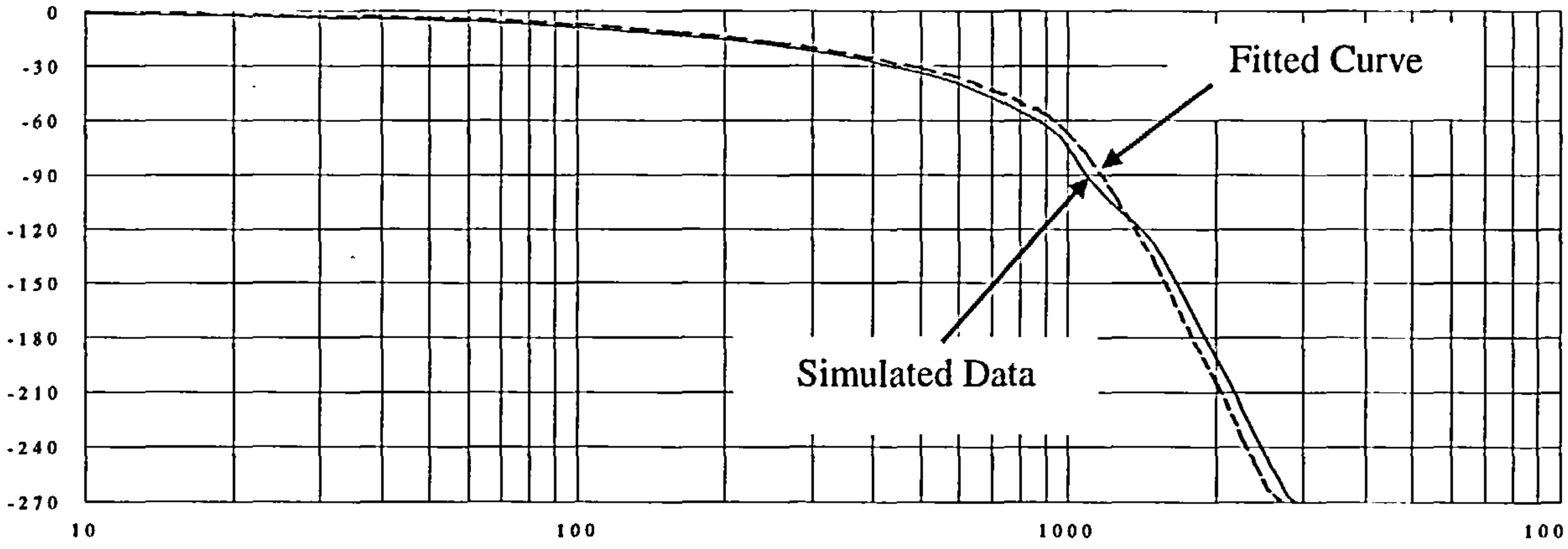



Fig.3.31 : Frequency response block diagram of the system

point is relatively high, which limits the application of this system as a power active filter in open loop mode to a frequency range of less than 500 Hz. It is very important to note that the frequency response of the filter is totally dependent on the parameter magnitudes especially the value of the filter smoothing inductance, $L_f$.




a - Magnitude Plots (dB) v/s frequency (Hz)




b - Phase Plots (degrees) v/s frequency (Hz)

Fig.3.32 : Simulated and modelled frequency response plots of the proposed system

## 3.6.2 Modelling of frequency response results

The frequency response obtained above, which applies to both cases of the switching power amplifier as well as the active power filter, can not be used in its present case to pursue the control analysis of the filter performance. The modelling of the above filter was performed using Mathcad. The modelling results are given by the fifth order system with two zeros expressed by the following equation

$$G(s) = K \frac{\left(1 + 2\frac{\xi_z}{\omega_z} s + \frac{s^2}{\omega_z^2}\right)}{\left(1 + 2\frac{\xi_{p1}}{\omega_{p1}} s + \frac{1}{\omega_{p1}^2} s^2\right)\left(1 + 2\frac{\xi_{p2}}{\omega_{p2}} s + \frac{1}{\omega_{p2}^2} s^2\right)\left(1 + \frac{1}{\omega_{p3}} s\right)} \quad (3.79)$$

The values of the parameters are given by

$$K = 165$$

$$\xi_z = 1.1 \qquad \xi_{p1} = 0.31 \qquad \xi_{p2} = 0.22$$

$\omega_x = 2\pi f_x$ where $x$ denotes the variable of interest

$$f_z = 2000 \qquad f_{p1} = 1300 \qquad f_{p2} = 2100 \qquad f_{p3} = 600 \quad (3.80)$$

The above values correspond to the simulated data and the resulting fitted curve is shown by the dotted lines in Fig.3.32.

The proposed system can now be approximated in any subsequent analysis by the model shown in equations (3.79) and (3.80). Further analysis of the system performance and stability now follows. The root locus analysis of the amplifier circuit is presented in Fig.3.33. The locus shows that two of the five branches of the system roots extend into the right hand side of the s-plane. This implies that for a stable closed loop operation care should be taken to place the closed loop poles well within the left-hand side of the s-plane.

### 3.6.3 Closed-loop modelling and operation

The above model of the filter can be rewritten in the form

$$G(s) = K \frac{(1 + a_1 s + b_1 s^2)}{(1 + a_2 s + b_2 s^2)(1 + a_3 s + b_3 s^2)(1 + a_4 s)} \quad (3.81)$$

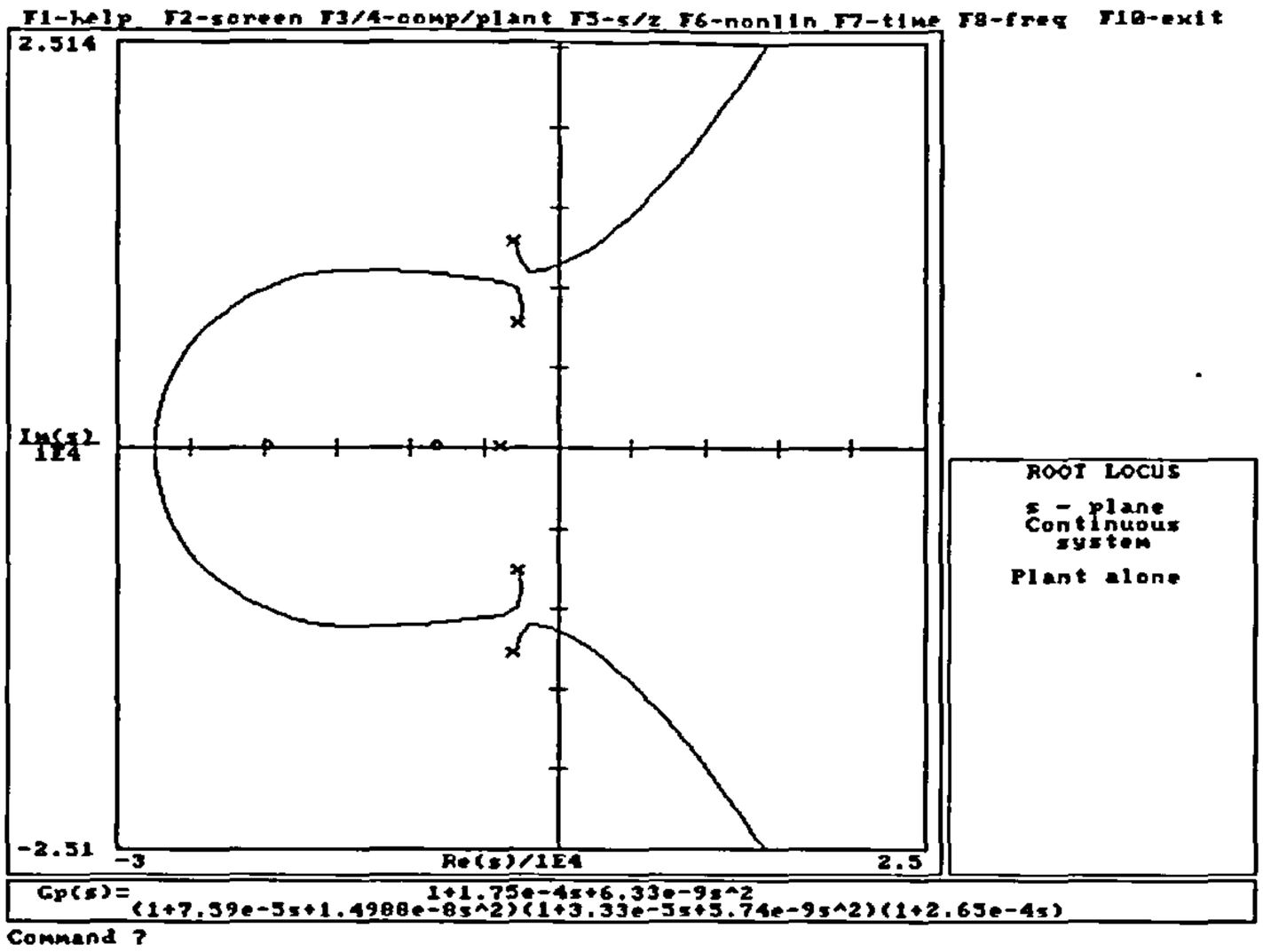



Fig.3.33 : Root Locus plot of the proposed system

where, $a_1 = 2\dfrac{\xi_z}{\omega_z}$ $b_1 = \dfrac{1}{\omega_z{}^2}$

$a_2 = 2\dfrac{\xi_{p1}}{\omega_{p1}}$ $b_2 = \dfrac{1}{\omega_{p1}{}^2}$

$a_3 = 2\dfrac{\xi_{p2}}{\omega_{p2}}$ $b_3 = \dfrac{1}{\omega_{p2}{}^2}$

$a_4 = \dfrac{1}{\omega_{p3}}$ (3.82)

Considering the block diagram of the closed loop system of Fig.3.34, the following equation can be written for the closed loop transfer function of the system with feedback gain of $K_f$ and a feedforward controller gain of $K_c$.

$$CLTF(s) = \frac{K_c\, G(s)}{(1 + K_c\, K_f\, G(s))} \tag{3.83}$$

which by substitution simplifies to the following monic denominator form

$$CLTF(s) = K_{system}\, \frac{(s^2 + \beta_1\, s + \beta_0)}{(s^5 + \gamma_4\, s^4 + \gamma_3\, s^3 + \gamma_2\, s^2 + \gamma_1\, s + \gamma_0)} \tag{3.84}$$

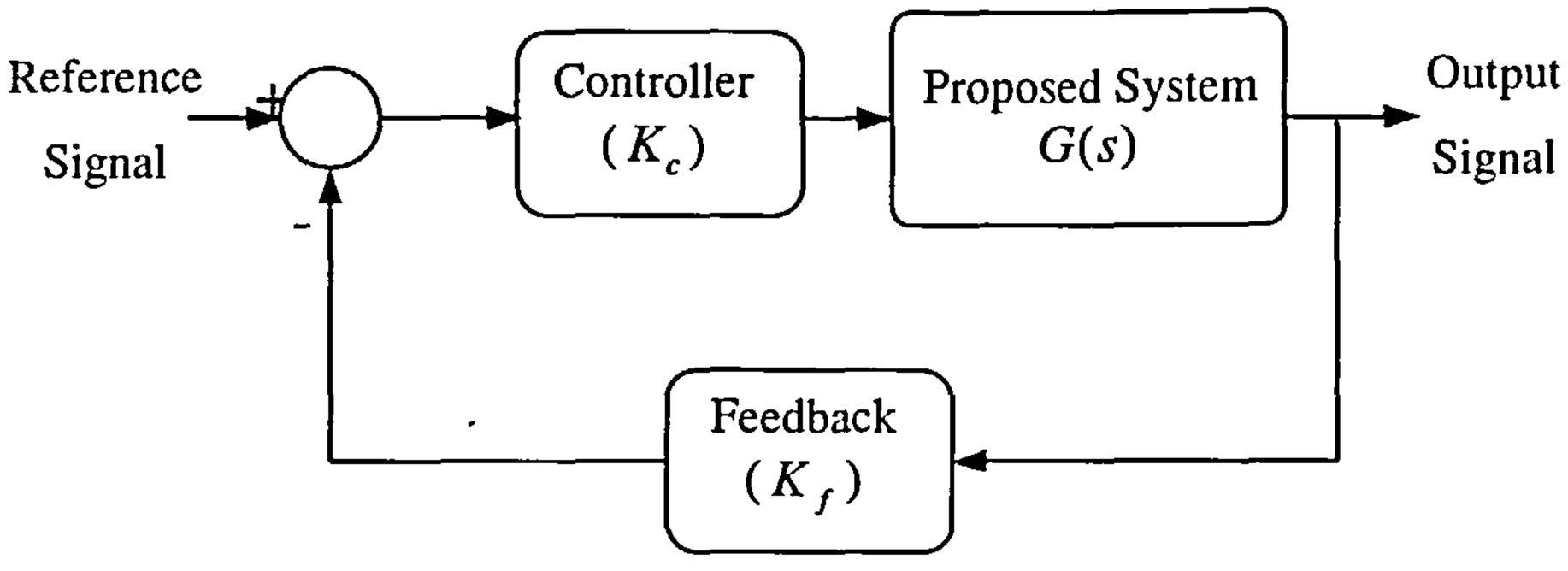



Fig.3.34 : Block diagram of the closed loop system

where the above variables are defined as,

$$K_{system} = \frac{K\ K_c\ b_1}{a_4\ b_2\ b_3}$$

$$\beta_1 = \frac{a_1}{b_1} \qquad \beta_0 = \frac{1}{b_1}$$

$$\gamma_4 = \frac{a_3\ a_4\ b_2 + a_2\ a_4\ b_3 + b_2\ b_3}{a_4\ b_2\ b_3}$$

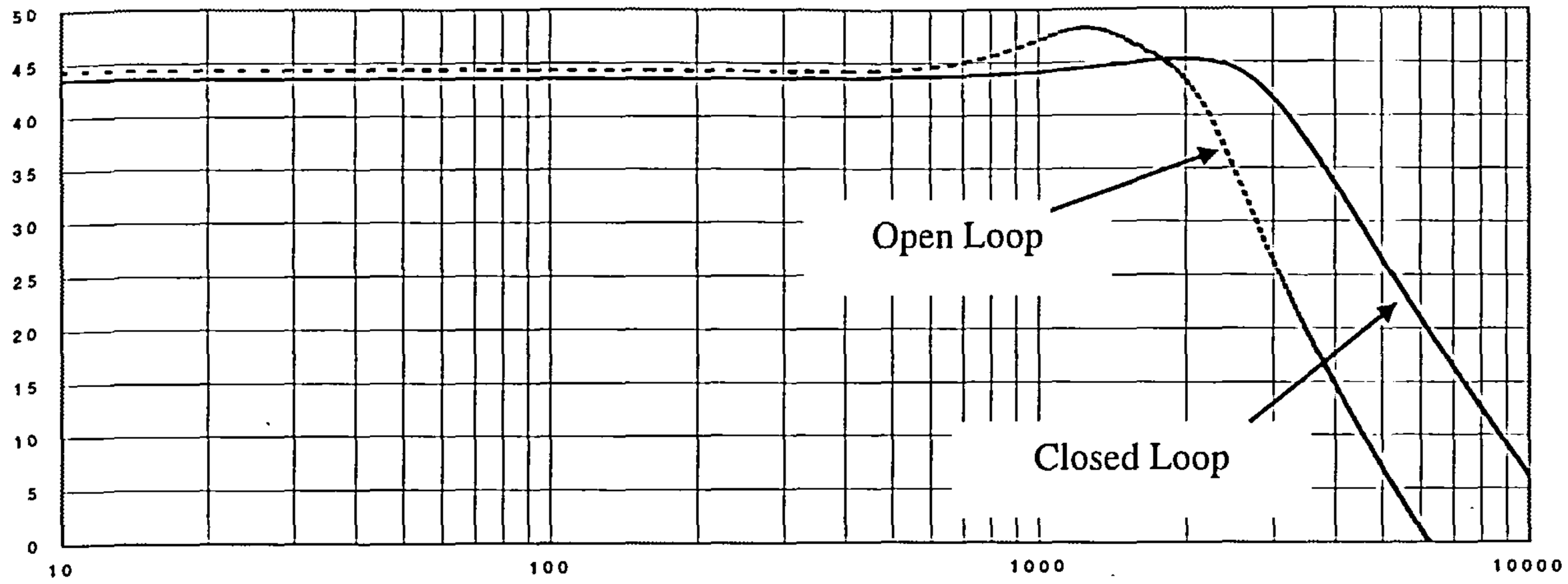
$$\gamma_3 = \frac{a_4\ b_2 + a_2\ a_3\ a_4 + a_4\ b_3 + b_2\ a_3 + b_3\ a_2}{a_4\ b_2\ b_3}$$

$$\gamma_2 = \frac{a_2\ a_4 + a_3\ a_4 + b_2 + a_2\ a_3 + b_3 + b_1\ K_c\ K_f\ K}{a_4\ b_2\ b_3}$$

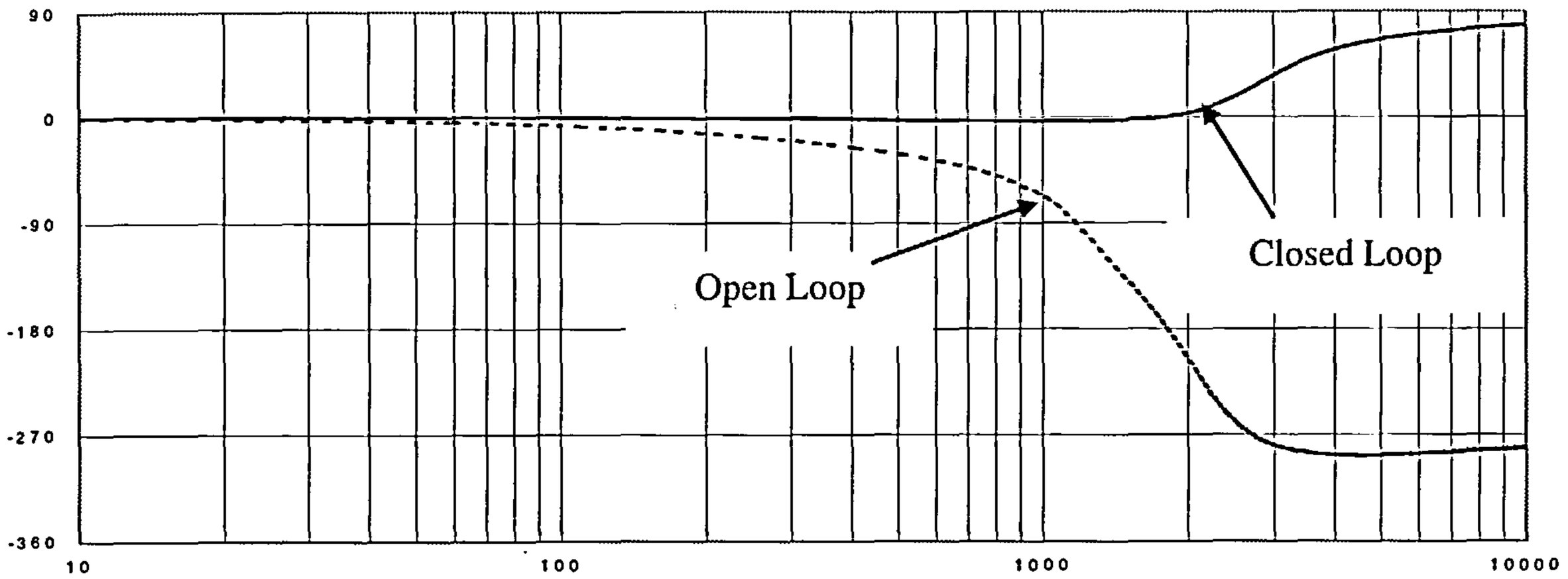
$$\gamma_1 = \frac{a_2 + a_3 + a_4 + a_1\ K_c\ K_f\ K}{a_4\ b_2\ b_3}$$

$$\gamma_0 = \frac{1 + K_c\ K_f\ K}{a_4\ b_2\ b_3} \qquad (3.85)$$

From the above model, the closed loop frequency response plot of the system is calculated. This then takes the form shown in Fig.3.35, where the open and closed loop modelled frequency responses are compared. The plot shows the system to have a flat gain with a negligible phase shift error up to frequencies above 2 kHz. The system parameters used in this case are




a - Magnitude Plots (dB) v/s frequency (Hz)




b - Phase Plots (degrees) v/s frequency (Hz)

Fig.3.35 : Open and closed loop frequency response of the system

$$K_c = 5$$

$$K_f = \frac{1}{165} \tag{3.86}$$

The closed loop simulation of the switching amplifier for a sinusoidal reference at a frequency of 50 Hz is shown in Fig.3.36. The system gain obtained from the simulation agrees with the predicted closed loop response as well as the negligible phase shift error which is approximately zero. The above frequency domain analysis shows that the system operated as an active power filter may be approximated by a

pure gain without any considerable phase shift. The analysis of the filter performance in the power system can now be processed.

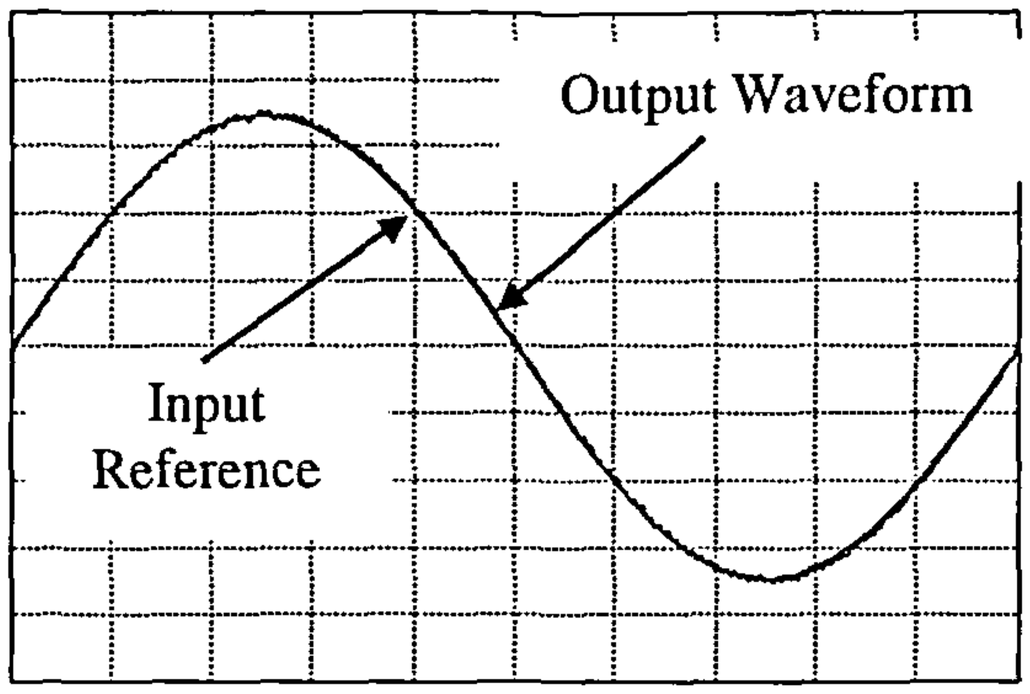



Fig.3.36 : Closed loop sinusoidal input and output waveforms of the system

## 3.7 Frequency domain analysis of shunt active power filters in power systems

The frequency characteristics of active power filters and their interconnections with passive filters are studied in [32,61]. However most of this analysis was intended for the series active filters. No analysis was provided for the basic case of a shunt active filters operating on the principle of current tracking mechanisms without the presence of any external tuned LC passive filters. The analysis provided in this case will give a broader idea about this system employing the voltage tracking mechanism outlined earlier in this chapter.

### 3.7.1 Modelling and evaluation of active filter performance in power systems

The active power filter circuit diagram, implemented in a power system with a nonlinear load, is shown in Fig.3.37. The figure outlines the harmonic circuit diagram

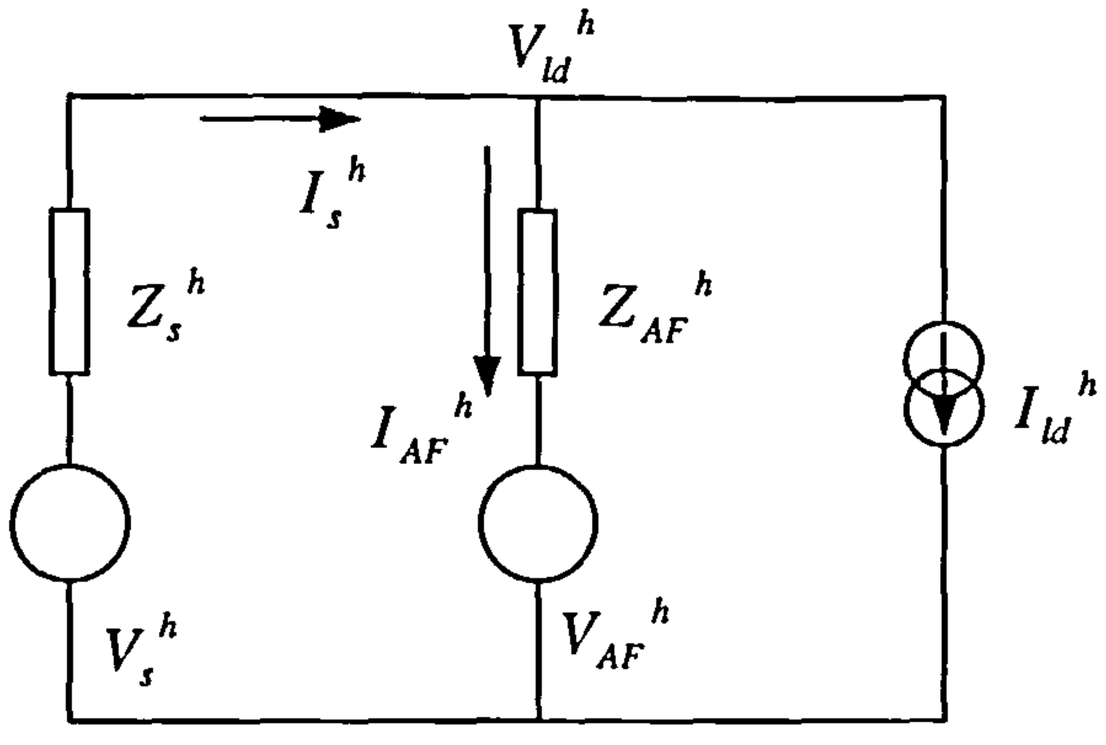



Fig.3.37 : Frequency domain analysis of shunt active filters in a power system

of the power supply represented in this case for the general harmonic frequency ($\omega_h$) by $V_s{}^h$ with an impedance of $Z_s{}^h$. The nonlinear load circuit is represented by a current source at the same harmonic order. The active filter is shown to consist of the controlled voltage source $V_{AF}{}^h$ in series with the filter impedance of magnitude $Z_{AF}{}^h$.

The following definitions apply

$$Z_{AF}{}^h = R_{AF} + j\,\omega_h\,L_{AF} \qquad \text{and} \qquad Z_s{}^h = R_s + j\,\omega_h\,L_s \tag{3.87}$$

The voltage loop-equation for the left hand side of the circuit can be written as

$$V_s{}^h = I_s{}^h \cdot Z_s{}^h + V_{ld}{}^h \tag{3.88}$$

Writing the current node equation at the upper node of the circuit yields

$$I_s{}^h = I_{AF}{}^h + I_{ld}{}^h \tag{3.89}$$

The third equation necessary for the solution of the system is the Kirchoff's voltage law applied to the active filter branch as follows

$$I_{AF}{}^h = \frac{V_{ld}{}^h - V_{AF}{}^h}{Z_{AF}{}^h} \tag{3.90}$$

Solving the above three equations for the output values of ${V_{ld}}^h$ and ${I_s}^h$ in terms of the inputs ${V_s}^h$ and ${I_{ld}}^h$ as well as the active filter voltage, ${V_{AF}}^h$, which is dependent on the other four system variables, the following two equations can be written

$$ {V_{ld}}^h = {V_s}^h \left( \frac{{Z_{AF}}^h}{{Z_s}^h + {Z_{AF}}^h} \right) + {V_{AF}}^h \left( \frac{{Z_s}^h}{{Z_s}^h + {Z_{AF}}^h} \right) - {I_{ld}}^h \left( \frac{{Z_s}^h \cdot {Z_{AF}}^h}{{Z_s}^h + {Z_{AF}}^h} \right) \qquad (3.91) $$

and

$$ {I_s}^h = {V_s}^h \left( \frac{1}{{Z_s}^h + {Z_{AF}}^h} \right) - {V_{AF}}^h \left( \frac{1}{{Z_s}^h + {Z_{AF}}^h} \right) + {I_{ld}}^h \left( \frac{{Z_{AF}}^h}{{Z_s}^h + {Z_{AF}}^h} \right) \qquad (3.92) $$

The model outlined by the two above two equations shows that the system can be represented by a $2 \times 2$ transfer matrix with four transfer-function elements, provided that the active filter voltage can be represented by the other system variables. Equation manipulations would reduce the system of equations to the following form.

$$ \begin{bmatrix} {V_{ld}}^h \\ {I_s}^h \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \cdot \begin{bmatrix} {V_s}^h \\ {I_{ld}}^h \end{bmatrix} \qquad (3.93) $$

The transfer matrix elements can then be defined as follows

$$ G_{11} = \left. \frac{{V_{ld}}^h}{{V_s}^h} \right|_{{I_{ld}}^h = 0} \qquad (3.94) $$

where, $G_{11}$ represents the amount of supply voltage harmonics which is reflected to the load side at the point of common coupling, without the presence of any load current harmonics.

$$ G_{22} = \left. \frac{{I_s}^h}{{I_{ld}}^h} \right|_{{V_s}^h = 0} \qquad (3.95) $$

where, $G_{22}$ represents the amount of load current harmonics which is reflected to the supply side, without the presence of any load voltage harmonics.

$$G_{12} = \left. \frac{V_{ld}{}^{h}}{I_{ld}{}^{h}} \right|_{V_s{}^{h}=0} \tag{3.96}$$

where, $G_{12}$ represents the load equivalent impedance without any supply voltage harmonics.

$$G_{21} = \left. \frac{I_{s}{}^{h}}{V_{s}{}^{h}} \right|_{I_{ld}{}^{h}=0} \tag{3.97}$$

where, $G_{21}$ represents the system admittance seen by the supply harmonic voltage source without the presence of any nonlinear load in the system.

### 3.7.2 Case of no active filter connected

The model presented earlier can be simplified to the original state of the system where the active filter is not connected to the power system. This can be performed by substituting the value of $Z_{AF}{}^{h} = \infty$ in the two system equations (3.91) and (3.92).

The result then follows

$$G_{11} = 1 \tag{3.98}$$

$$G_{22} = 1 \tag{3.99}$$

$$G_{12} = -Z_{s}{}^{h} \tag{3.100}$$

$$G_{21} = 0 \tag{3.101}$$

This implies that the supply suffers from all load current harmonics while the load witnesses the supply voltage harmonics. These transfer functions represent the system performance, which can be used in conjunction with the known values of system inputs to predict the expected response. The equivalent impedance of the load system seen from the point of common coupling by the rest of the circuit is the negative of the supply impedance; while the input admittance of the overall system to

the supply harmonic voltage is seen to be zero. This implies that there exists no current path for the supply voltage harmonics to force harmonic currents into the system while it is unloaded.

### 3.7.3 Compensation strategies

From the above modelling, it is clear that the system operation and performance now relies upon the active filter reference determination. In other words, the system relies on the choice of the control variable $V_{AF}{}^{h}$. Several possibilities arise including the various variables of the input and output as well as the current derivatives. These are listed in the following subsections. It is noted that the variable $G_{AF}$ represents the closed loop transfer function of the active filter.

**Case of ($V_{AF}{}^{h} = G_{AF}\ I_{s}{}^{h}$)**

The modelling equations, (3.91) and (3.92), introduced earlier, reduce to the following

$$G_{11} = \frac{Z_{AF}{}^{h} + G_{AF}}{Z_{s}{}^{h} + Z_{AF}{}^{h} + G_{AF}} \tag{3.102}$$

$$G_{22} = \frac{Z_{AF}{}^{h}}{Z_{s}{}^{h} + Z_{AF}{}^{h} + G_{AF}} \tag{3.103}$$

$$G_{12} = -Z_{s}{}^{h} \cdot \left( \frac{Z_{AF}{}^{h}}{Z_{s}{}^{h} + Z_{AF}{}^{h} + G_{AF}} \right) \tag{3.104}$$

$$G_{21} = \frac{1}{Z_{s}{}^{h} + Z_{AF}{}^{h} + G_{AF}} \tag{3.105}$$

The system transfer functions in this case show a tendency to reduce the effect of the supply voltage harmonics at the point of common coupling. This is a favourable effect; however, the current transfer function can only do the same with the ratio

depicted above. In this case the total system harmonic elimination is not at all feasible. Moreover, the supply voltage harmonics have a current path in the system, which is clear from the last equation. It is to be added that the system characteristic equation in this case is dependent on the supply and filter impedances as well as the active filter transfer function.

**Case of** $(V_{AF}{}^{h} = G_{AF}\ I_{ld}{}^{h})$

The modelling equations (3.91) and (3.92), reduce to the following

$$G_{11} = \frac{Z_{AF}{}^{h}}{Z_{s}{}^{h} + Z_{AF}{}^{h}} \tag{3.106}$$

$$G_{22} = \frac{Z_{AF}{}^{h} - G_{AF}}{Z_{s}{}^{h} + Z_{AF}{}^{h}} \tag{3.107}$$

$$G_{12} = -Z_{s}{}^{h} \cdot \left( \frac{Z_{AF}{}^{h} + G_{AF}}{Z_{s}{}^{h} + Z_{AF}{}^{h}} \right) \tag{3.108}$$

$$G_{21} = \frac{1}{Z_{s}{}^{h} + Z_{AF}{}^{h}} \tag{3.109}$$

Similar to the above case, the voltage transfer function in this case shows lesser tendency to reduce the effect of the supply voltage harmonics at the point of common coupling. On the other hand, the current transfer function shows a better performance since it has the desirable effect of reducing the current transfer ratio. The main problem is that the value of the filter impedance is a complex quantity, which would not ensure a good harmonic elimination. Similar to the previous case, the supply voltage harmonics have a current path in the system, which is clear from the last equation. This impedance is reduced in this case. It is to be added that the system

characteristic equation in this case is shown to be dependent only on the supply and filter impedances.

## Case of ($V_{AF}{}^{h} = j\,\omega_h\,G_{AF}\,I_s{}^{h}$)

The presence of the complex term ($j\,\omega_h$) implies that the active filter voltage is proportional to the rate of change of the supply current, since this factor implies a differentiation process performed onto the variable of interest. The modelling equations (3.91) and (3.92), yields

$$G_{11} = \frac{Z_{AF}{}^{h} + j\,\omega_h\,G_{AF}}{Z_s{}^{h} + Z_{AF}{}^{h} + j\,\omega_h\,G_{AF}} \tag{3.110}$$

$$G_{22} = \frac{Z_{AF}{}^{h}}{Z_s{}^{h} + Z_{AF}{}^{h} + j\,\omega_h\,G_{AF}} \tag{3.111}$$

$$G_{12} = -\,Z_s{}^{h} \cdot \left( \frac{Z_{AF}{}^{h}}{Z_s{}^{h} + Z_{AF}{}^{h} + j\,\omega_h\,G_{AF}} \right) \tag{3.112}$$

$$G_{21} = \frac{1}{Z_s{}^{h} + Z_{AF}{}^{h} + j\,\omega_h\,G_{AF}} \tag{3.113}$$

Similar to the previous two cases, the transfer functions are all dependent upon the supply and filter impedances as well as the transfer function of the filter. This case is an exact replica of the first one with the only variation being the addition of the derivative term to the equations. The system in this case performs slightly better than the previous ones however no total harmonic elimination can be achieved.

## Case of ($V_{AF}{}^{h} = j\,\omega_h\,G_{AF}\,I_{ld}{}^{h}$)

The system in this case is dependent on the rate of change of the load current harmonics. The modelling equations (3.91) and (3.92), reduce to the following

$$G_{11} = \frac{{Z_{AF}}^{h}}{{Z_s}^{h} + {Z_{AF}}^{h}} \tag{3.114}$$

$$G_{22} = \frac{{Z_{AF}}^{h} - j\,\omega_h\, G_{AF}}{{Z_s}^{h} + {Z_{AF}}^{h}} \tag{3.115}$$

$$G_{12} = -{Z_s}^{h} \cdot \left( \frac{{Z_{AF}}^{h} - j\,\omega_h\, G_{AF}}{{Z_s}^{h} + {Z_{AF}}^{h}} \right) \tag{3.116}$$

$$G_{21} = \frac{1}{{Z_s}^{h} + {Z_{AF}}^{h}} \tag{3.117}$$

The above equations show that the system is the exact replica of the second case with the only performance improvement achieved by the introduction of the derivative term, which can in this case affect the numerator in the harmonic current transfer function. This may lead to total harmonic elimination (for an ideal filter inductance). The system characteristic equation still depends on the supply impedance which is uncontrollable by the active filter system.

**Case of** $({V_{AF}}^{h} = {V_{ld}}^{h} + G_{AF}\ {I_s}^{h})$

The modelling equations (3.91) and (3.92), reduce to the following

$$G_{11} = 1 \tag{3.118}$$

$$G_{22} = \frac{{Z_{AF}}^{h}}{{Z_{AF}}^{h} + G_{AF}} \tag{3.119}$$

$$G_{12} = -{Z_s}^{h} \cdot \left( \frac{{Z_{AF}}^{h}}{{Z_{AF}}^{h} + G_{AF}} \right) \tag{3.120}$$

$$G_{21} = 0 \tag{3.121}$$

The introduction of the harmonic voltage at the point of common coupling has strong effects on the system transfer functions. This fact is shown clearly by the system

transfer functions. The filter system in this case can not stop the supply harmonic voltages from reaching the point of common coupling. Nevertheless, the same supply can not force any harmonic circulating currents in the system since the system in this case has infinite impedance for supply voltage harmonics. The current transfer function shows only the system capability of reducing the load current harmonic effects on the supply current. It is however unable to completely eliminate the current harmonics. Moreover, the characteristic impedance of the system is mainly dependent upon the filter impedance and its transfer function. No supply dependency is detected in this case which shows a better performance since this impedance value ($Z_s{}^h$) is normally unknown and unpredictable.

**Case of** ($V_{AF}{}^h = V_{ld}{}^h + G_{AF}\ I_{ld}{}^h$)

The modelling equations (3.91) and (3.92) presented earlier, reduce to the following

$$G_{11} = 1 \tag{3.122}$$

$$G_{22} = 1 - \frac{G_{AF}}{Z_{AF}{}^h} \tag{3.123}$$

$$G_{12} = -Z_s{}^h \cdot \left(1 - \frac{G_{AF}}{Z_{AF}{}^h}\right) \tag{3.124}$$

$$G_{21} = 0 \tag{3.125}$$

The transfer functions of the system in this case are very similar to the previous case except for the fact that the current transfer function has the ability to better reduce the harmonic current effect on the supply side. The characteristic impedance in this case is solely the filter impedance. No supply impedance dependency exists in this case.

**Case of** ($V_{AF}{}^{h} = V_{ld}{}^{h} + j\,\omega_h\,G_{AF}\,I_s{}^{h}$)

The modelling equations (3.91) and (3.92), can be rewritten as

$$G_{11} = 1 \tag{3.126}$$

$$G_{22} = \frac{Z_{AF}{}^{h}}{Z_{AF}{}^{h} + j\,\omega_h\,G_{AF}} \tag{3.127}$$

$$G_{12} = -\,Z_s{}^{h} \cdot \left( \frac{Z_{AF}{}^{h}}{Z_{AF}{}^{h} + j\,\omega_h\,G_{AF}} \right) \tag{3.128}$$

$$G_{21} = 0 \tag{3.129}$$

The addition of the derivative term to the active filter voltage equation provides a better controllability over the system current harmonics. However, the system still remain unable to completely eliminate the current harmonics. No supply impedance dependency exists in this case.

**Case of** ($V_{AF}{}^{h} = V_{ld}{}^{h} + j\,\omega_h\,G_{AF}\,I_{ld}{}^{h}$)

From the modelling equations (3.91) and (3.92),

$$G_{11} = 1 \tag{3.130}$$

$$G_{22} = 1 - \frac{j\,\omega_h\,G_{AF}}{Z_{AF}{}^{h}} \tag{3.131}$$

$$G_{12} = -\,Z_s{}^{h} \cdot \left( 1 - \frac{j\,\omega_h\,G_{AF}}{Z_{AF}{}^{h}} \right) \tag{3.132}$$

$$G_{21} = 0 \tag{3.133}$$

In this case, the system transfer functions indicate that this control technique is unable to affect the load voltage harmonics at the point of common coupling, as it will still be affected by the value of the total supply voltage harmonics. This is the same case as

that of the previous three control strategies, which use the load harmonic voltage at the point of common coupling to calculate the system control law. The other characteristics are however improved.

The current transfer function shows that the system can reduce the effects of the load current harmonics, which are reflected into the supply side. By considering the fact that the active filter impedance is composed of an inductor, and that the transfer function of the active filter can be approximated by a gain equal to the value of the inductance, the idealised system would then yield a negligible value for the current transfer function if not zero. The system also exhibits an equivalent load impedance with the same ratio as the current transfer function multiplied by the negative of the supply impedance. The supply can only see an open circuit for the harmonic circulating currents, which implies the system capability to block the circulating currents due to the supply voltage harmonics. The active filter in this case can eliminate the effect of the supply voltage variations on the active filter performance.

This case provides an excellent performance over the cases of the other reference signals. Hence, the reference control law used here is chosen as the reference signal for the proposed active filter. The main advantage of this technique lies in the fact that the characteristic impedance of the system is represented here only by the filter impedance, which implies that it does not at all depend on any of the supply parameters. The response of the system is consequently independent from any variations in $Z_s^h$, which can be caused by possible changes in the network topology of the power system distribution. This fact is very important for retrofit applications of active filters.

## 3.8 Software simulation of the proposed circuit

To prove the operating capabilities of the proposed circuit as chosen in the previous section, the circuit is simulated on the digital computer with the employed control technique. This is presented in the following paragraphs.

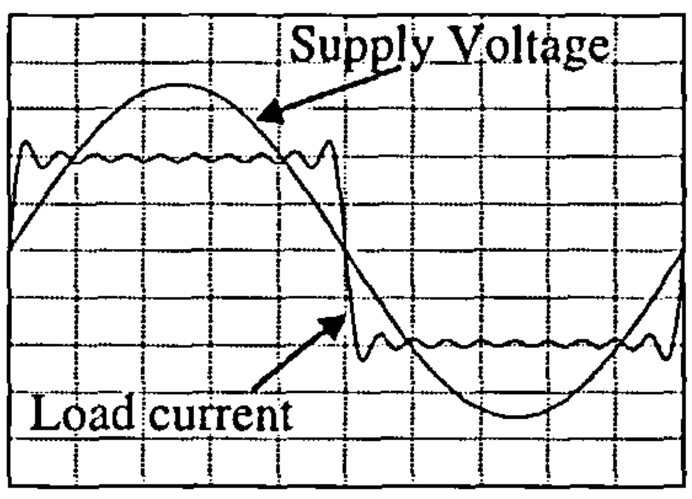
The core program, which incorporated the switching power-amplifier, produced open- and closed-loop results of the switching amplifier. The reference signal in the above cases was either a sinusoid, a triangular or a square wave respectively. From the results, the system performance was concluded in the frequency response plots of the open- and closed-loop conditions. The root locus of the modelled system was then used to determine the stable closed loop gain of the system.

The simulation of the active filter system can be tackled by modifying the above program to incorporate a nonlinear load with harmonic generation. This is performed using the respective current harmonics for each of the system loads. The simulation takes into consideration the fundamental component of the load current as well as its harmonics. It incorporates these values into a reference current calculator based on the voltage tracking principles outlined in the previous section. The calculated reference is then used in this case to generate the control effort from the closed-loop system controller. The control of the simulated circuit is minimal for this case in order to show the system capability of operation. The closed-loop simulation uses the effect of a simple proportional controller and yields rather satisfactory results. The power circuit is then simulated under the switching control of a simplified PWM

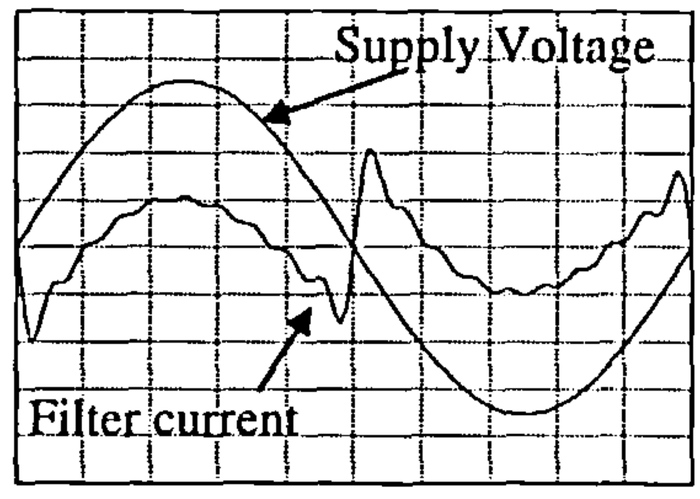
technique that consists of a clocked switching controller. The overall program was implemented in Borland Pascal.

The simulation takes into consideration two types of fixed loads. The first is a rectifier circuit feeding a highly inductive load with a known frequency spectrum. The second is a rectifier feeding a capacitive charging circuit on the dc side with a bleeding resistor across its terminals.

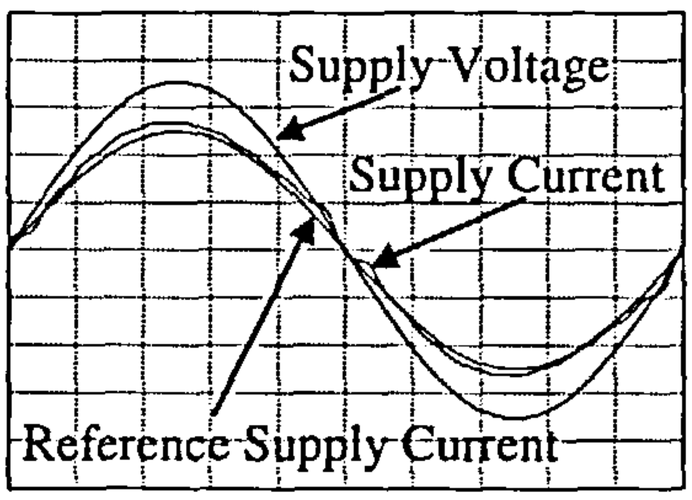
These simulation results are presented in Fig.3.38 and Fig.3.39. For the case of an inductive load on the dc side of the rectifier, Fig.3.38-a shows the supply current before filtering as well as the supply voltage waveforms, while Fig.3.38-b presents the filter current with the supply voltage. Fig.3.38-c shows the filtered supply current, which is approximately sinusoidal, in conjunction with the reference filter current and



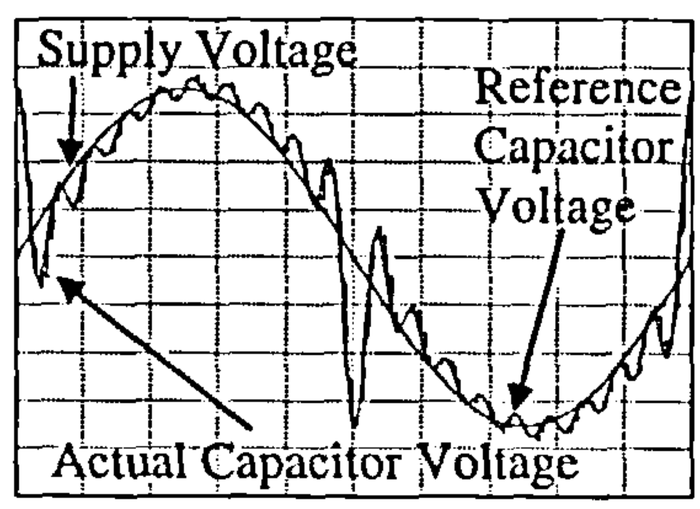

(a)




(b)




(c)




(d)

Fig.3.38 : Simulation of active filter operation with an inductive load on the dc side of a rectifier bridge

the supply voltage. It is to be noted that the filtered supply current of Fig.3.38-c is slightly larger than its reference value, as the filter draws a fundamental current component. This current is due to two main reasons: (i) the fact that the switches are not assumed ideal which implies the presence of losses in the system, (ii) the system delay in responding to the voltage reference variations. This error can be seen in Fig.3.38-d (the difference between the actual and reference capacitor voltages). The oscillations on the reference signal are mainly due to the fact that the implementation of the nonlinear load is bandlimited, since only a finite spectrum is assumed. The voltage error between the actual and reference capacitor voltage waveforms causes a considerable amount of fundamental current to flow in the filter, which eventually increases the total value of the actual filter current as pointed out earlier.

The same performance of the system simulated above is provided in Fig.3.39 for the case of a bridge rectifier charging a dc reservoir capacitor with a resistive load. This

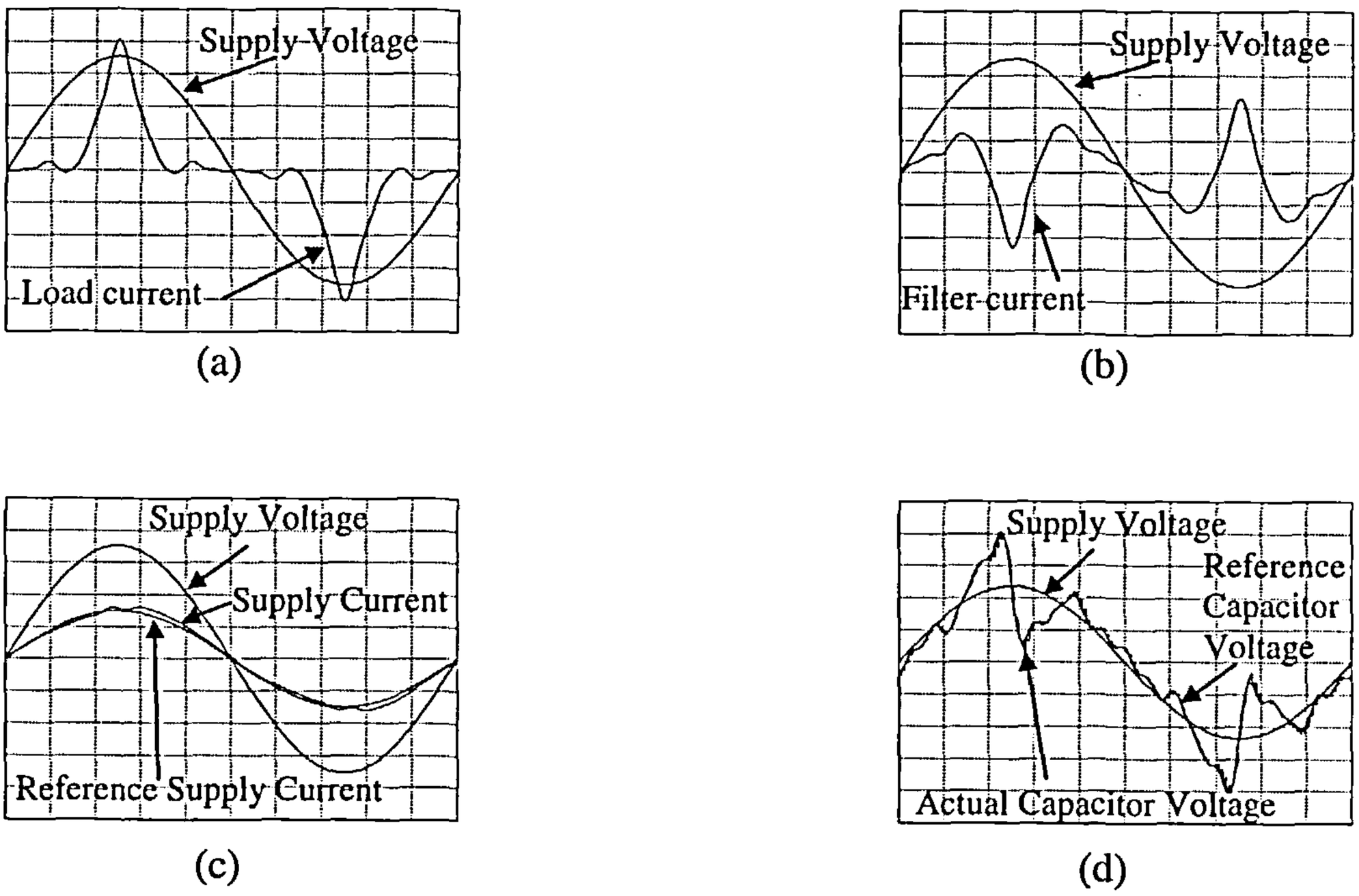



Fig.3.39 : Simulation of active filter operation with a capacitive load on the dc side of a rectifier bridge

system is presented here to demonstrate the ability of the filter to cope with high rates of voltage and current variations. The peak value of the load current in this case is much higher than that of the inductive load where the waveform is flattened. This appears clearly by visualising the severe variations of the capacitor voltage reference waveform of Fig.3.39-d. The system however copes quite well with this case and the fundamental component depicted in Fig.3.39-c is shown to be near its reference fundamental load current component.

The smooth current waveforms shown in both figures are mainly due to the filter inductance which compensate the limited switching frequency of the charging circuit by delaying the filter current deviation from its reference signal. The choice of this value is rather critical and has a strong effect on the system time response.

## 3.9 Summary

This chapter presented the main problems, involved with other active filtering techniques. These were used to develop the main requirements of the proposed system. The theoretical analysis, behind which lies the idea of the proposed system, was also presented. This is manifested in the proposed control law, which governs the operation of the filter. The time domain analysis and modelling of the proposed power circuit was also presented. This was followed by the frequency domain modelling and analysis, which provided a transfer function model of the system. The frequency domain analysis of this model is very important in proving the capabilities of the circuit to operate as designed. The proof of the proposed capacitor voltage control law was also presented in this chapter with the analysis of the frequency response of the active power filter performance in the power system under various

control laws. Finally the simulation results of the active filter performance were also presented in this chapter.

Having presented the system so far using simulation and theoretical analysis, the performance is rather satisfactory, taking into consideration the fact that the system controller and the PWM use simplified techniques. The system practical implementation now follows in the following chapter.

# Chapter 4

# Circuit Implementation and Practical Results

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# Circuit Implementation and Practical Results

## 4.1 Introduction

The active filter circuit, proposed in the last chapter, constitutes a main step towards the implementation of the system. As shown in the block diagram of Fig.2.1, the proposed power circuit realises only one block of the overall system. This is namely the power circuit block. It now remains to discuss in this chapter the implementation of each of the other blocks of the system. This includes the implementation of a fast harmonic current estimation block, which uses a modified Fourier analysis technique. This chapter also discusses the practical results obtained from the implementation of the overall active filter system.

## 4.2 Synthesis of the reference signal

It is well known that the response time of any filter is governed by three main factors.

These are namely:

(i) the synthesis of the reference signal

(ii) the overall system controller

(iii) the power circuit response time

The time response of each of these blocks is critical in considering the possible delays between the change of the load current pattern and the corresponding reaction of the filter. This implies that each of the above three factors is to have the minimum possible delay. In this section the performance of the reference current generator is discussed and thoroughly analysed.

### 4.2.1 Generation techniques of the load current harmonics

According to the techniques proposed in the surveyed literature, which are discussed in chapter two, the main current synthesis methods for single-phase applications are implemented either in analog or digital systems as in the following

**Analogue harmonic synthesis:** This technique uses analog low-pass signal filters mainly to separate the fundamental component of the nonlinear load current. This waveform is then subtracted from the total load current to yield the load current harmonic signal. The design of the active filter has to incorporate at least a $6^{th}$ order filter to ensure a reasonable roll-off frequency. The main disadvantage of this method is that the filtered fundamental has a severe magnitude and a phase errors. The phase lag error reaches at least 100°, which is a very large value. One mean of curing this phase-shift problem is to use a phase lead circuit, which shifts the signal until it obtains the original phase. However, this implies the fact that the phase shift between the true fundamental signal and the obtained corrected value is 360°. The obtained signal is thus lagging by at least one complete cycle behind the true waveform. This is considered to be a very long delay for dynamic systems that change their harmonic load pattern from cycle to cycle. The analogue system can hence not be used in this application.

**Digital FFT calculations:** The basic idea of this method, which is used in most of the literature, relies on the fact that the FFT is performed on a certain number of samples to generate the frequency spectrum of the nonlinear load waveform. The processed data belongs normally to the previous cycle or in other cases to a number of complete

sampled-cycles. Again, the system is delayed by at least one complete cycle, in addition to the time taken to compute the FFT. As an example, it was demonstrated in [74] that an 1024 (8-bit) samples FFT algorithm implemented on a the state of the art technology dedicated digital signal processor (DSP) running at 166 MHz is around 70 μsec. Other higher computational times (with a minimum factor of 40) can still be expected depending on the processor used. This is considered as an additional delay for the system. Hence, the overall delay of the reference current generator is the sum of the data acquisition cycles and the computation period. The system will then start reacting at the beginning of the following mains cycle (assuming that the decision is instantaneous). The inherent long time delay of this system is the main reason behind the fact that the three-phase compensators do not use this technique. They prefer to go to more elaborate techniques, which are sometimes inaccurate or slow in response as outlined in the survey of chapter 2.

### 4.2.2 Modified moving window Fourier analysis

To overcome the above problems, the digital system is chosen, however, several modifications remain to be added to it to increase its performance. The implementation of the reference harmonic current generator is performed using a modified Sliding-Window Fourier computation method, which is developed based upon the available hardware. The theoretical analysis of the technique is explained in the following section.

### 4.2.2.1 Basic equations

For any arbitrary band limited repetitive waveform $x(t)$ with a period $T_{period}$ and consisting only of odd harmonics ranging from the fundamental to $N_{\max}$ without any dc-component, the Fourier series equations are given by the following [75,76]

$$x(t) = \sum_{\substack{i=1 \\ i\ odd}}^{N_{\max}} A_i \cos(i\omega t) + B_i \sin(i\omega t) \tag{4.1}$$

where,

$$A_i = \frac{2}{T_{period}} \int_0^{T_{period}} x(t) \cos(i\omega t)\, dt \tag{4.2}$$

and

$$B_i = \frac{2}{T_{period}} \int_0^{T_{period}} x(t) \sin(i\omega t)\, dt \tag{4.3}$$

The above equations need to be modified in order to be used in PC calculations with digital discrete systems. Discretising the above equations at a sampling interval fixed at $\tau$ and with a total number of points of $N_{points}$, we get

$$x(k\tau) = \sum_{\substack{i=1 \\ i\ odd}}^{N_{\max}} A_i \cos(i\omega k\tau) + B_i \sin(i\omega k\tau) \tag{4.4}$$

where,

$$k = 0,1,2,\ldots,N_{points} \tag{4.5}$$

$$\tau = \frac{T_{period}}{N_{points}} \tag{4.6}$$

and similar to the above,

$$A_i = \frac{2}{N_{points}} \sum_{j=0}^{N_{points}} x(j\tau) \cos(i\omega\ j\tau) \tag{4.7}$$

and

$$B_i = \frac{2}{N_{points}} \sum_{j=0}^{N_{points}} x(j\tau) \sin(i\omega\ j\tau) \qquad (4.8)$$

The above equations are still unsuitable for the PC computation of the instantaneous current harmonics. The problem with the above equations is that they require the start of the signal from an initial fixed time.

This is, however, not the case for the sliding window Fourier analysis since the starting point is always advancing in the data array, once the new sampled point is available. The modification in this case would not speed up the computation effectively, since it is necessary to synthesise each harmonic amplitude and phase. The point to note in this case is that the fundamental component is the only one needed in active filtering applications. By calculating only the fundamental component and subtracting its value from the total nonlinear load current, it is possible to obtain the total current harmonic signal, which in this case would not need a large amount of calculations.

For this specific purpose of active filtering, the only required waveform, as outlined above, is the fundamental. Hence, equation (4.4) reduces to the following

$$x(k\tau) = A_1 \cos(\omega\ k\tau) + B_1 \sin(\omega\ k\tau) \qquad (4.9)$$

where, $k$ and $\tau$ are as given above. The factors $A_1$ and $B_1$ are given here as follows

$$A_1 = \frac{2}{N_{points}} \sum_{j=N_{current}}^{N_{points}+N_{current}} x(j\tau) \cos(\omega\ j\tau) \qquad (4.10)$$

and

$$B_1 = \frac{2}{N_{points}} \sum_{j=N_{current}}^{N_{points}+N_{current}} x(j\tau) \sin(\omega\ j\tau) \qquad (4.11)$$

To calculate the instantaneous value of the desired signal, the values of $A_1$ and $B_1$ have to be known at the same instant of time. This incorporates the necessity of evaluating the two summations depicted by equations (4.10) and (4.11) at every sampling instant, which is very time consuming.

The better alternative would be to use the software capabilities of the 80486 assembly language in handling single dimensional arrays [77-80] to implement the summations of equation (4.10) and (4.11) into two single dimensional arrays. The values stored in these two arrays correspond to the consecutive evaluations of the equations under the summation signs of equations (4.10) and (4.11). The total summation of all the elements of the two arrays is calculated once to form the initial values of $A_1$ and $B_1$, which are continuously updated. Then by using the principle of circular arrays, which introduces the new sampled and calculated value into the position of the old one, the old values are subtracted from the total sums of $A_1$ and $B_1$, respectively. The new values are then added to the resulting $A_1$ and $B_1$, respectively. This yields the new coefficients. The overall calculation process can be accomplished in the desired microprocessor time slot. The technique described in this case is summarised in the block diagram of Fig.4.1, which shows the computational steps of the system as discussed earlier.

### 4.2.2.2 Hardware and software implementation

The hardware system used incorporated a 133 MHz Pentium PC fitted with a 12-bit analog and digital interface card (PCL812-PG). The interface card incorporates the 12-bit analog to digital interface which is used for the acquisition of the load current signal. This signal is, in turn, sensed using a Hall effect current transducer. The

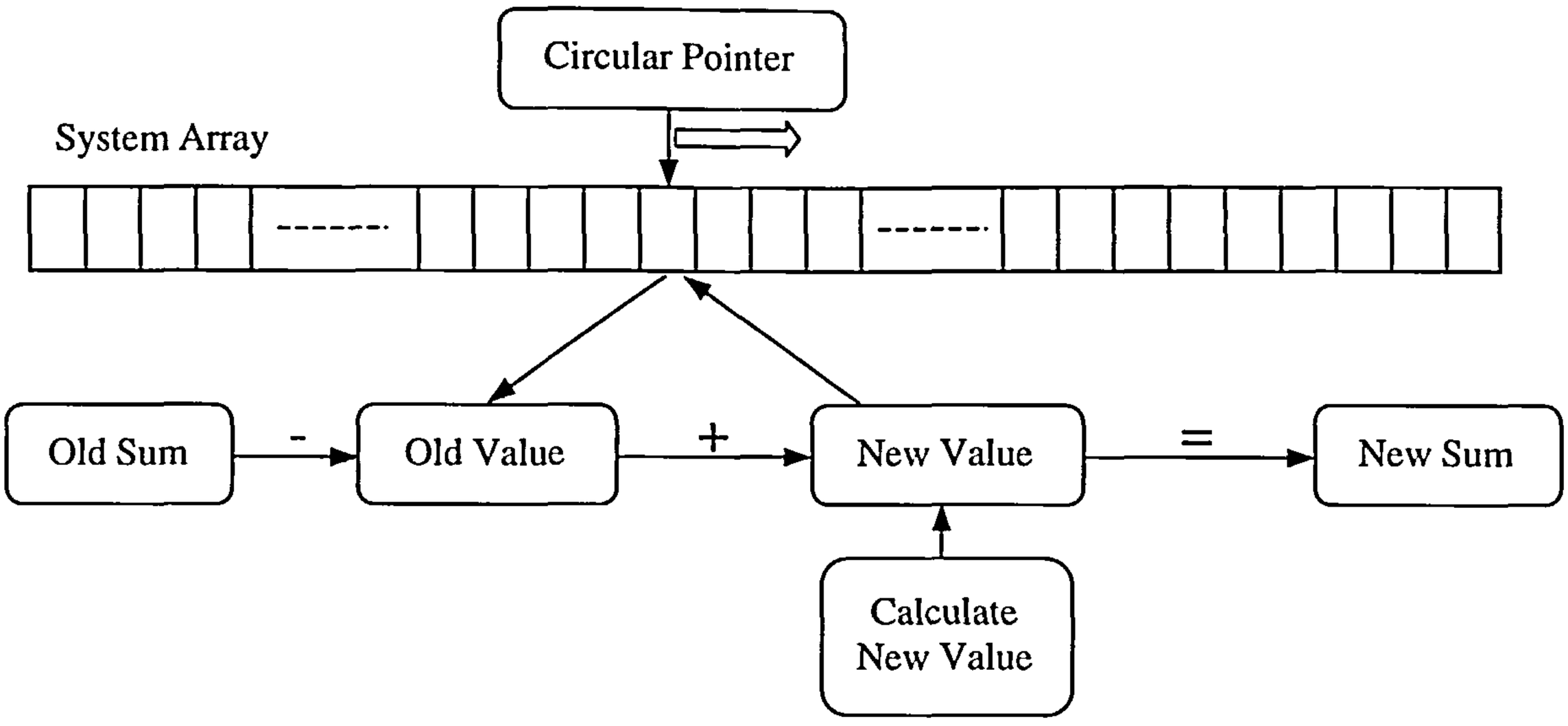



Fig.4.1 : Proposed computational system model

digital to analog interfaces on board are used to output the control signals from the PC for monitoring purposes. The card incorporates an additional 16-bit digital input and another 16-bit digital output ports. These ports are used to communicate the control signal from one PC to the other in addition to the handshaking process. The system uses some of the input signals to interface with an external custom-built board that is necessary to detect the starting edge of the supply voltage waveform for the positive and negative half cycles for synchronisation purposes. These signals are isolated from the mains using 6N137 high-speed optocouplers and are connected to the input port of the PCL812-PG card.

The software running the process uses a 32-bit resolution floating-point assembly language program dedicated for the Intel 80486 family of microprocessors, which is upward compatible with the Pentium processor. The assembly language program used is shown in Appendix B. The flow chart of this program is presented in Fig.4.2. The only role of the Personal Computer used is to compute the harmonic content of

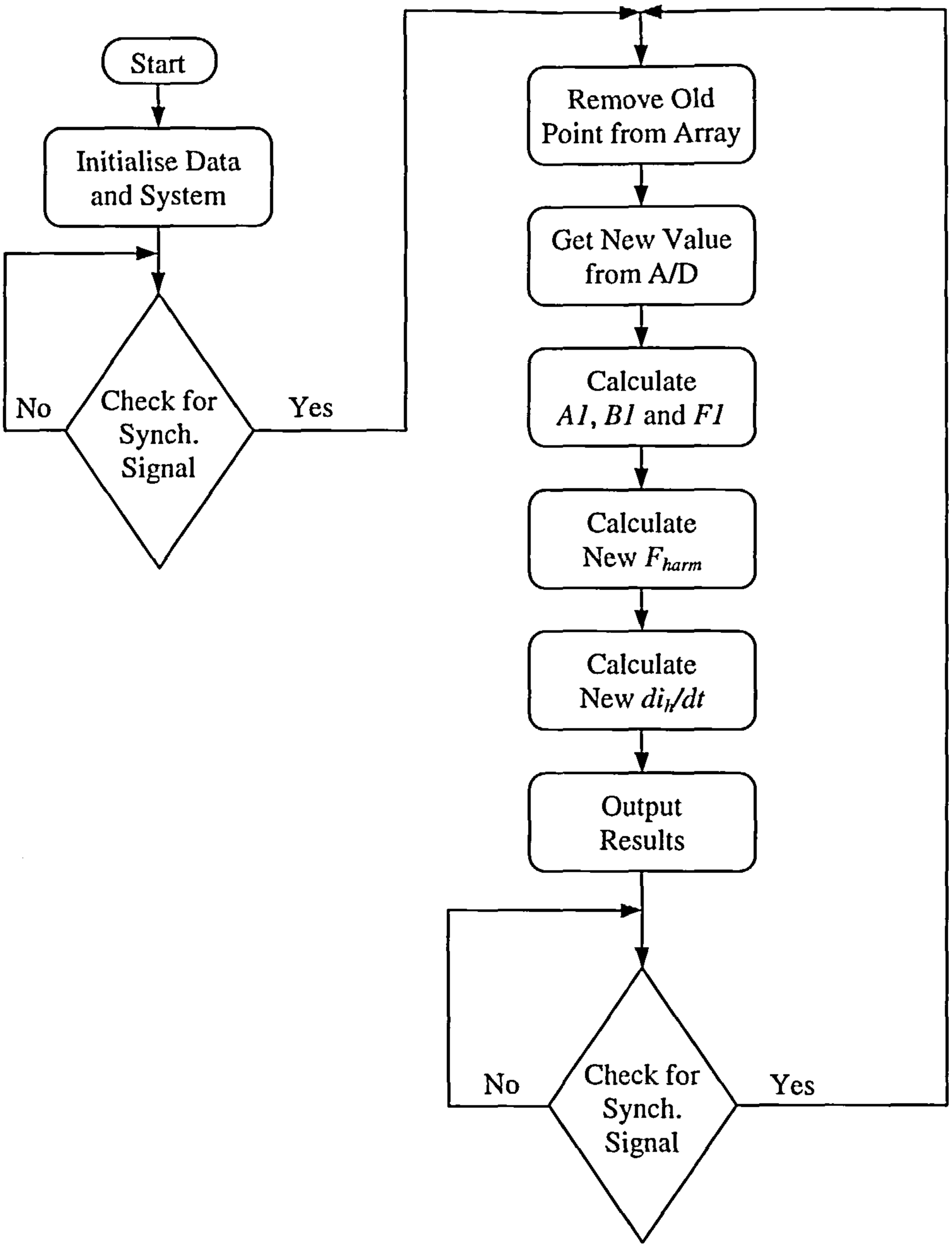



Fig.4.2 : Flow chart for Harmonic Computation Program

the load current waveform. The program then generates three waveforms, which are namely:

1. the fundamental component of the load current
2. the total harmonic content of the load current
3. the rate of change of the total harmonic content of the load current scaled by the value of the filter inductance.

These resulting waveforms are then normalised into 12-bit integer format and sent through the communication ports to the second PC, which will perform the remainder of the control task.

The floating point calculations were used in this program in order to minimise the computational time performed by the processor especially in the cases of multiplication and division without the need for any integer normalisation of the magnitudes of the sines and cosines generated by the PC and corresponding to each of the computational instants. It is to be noted that the sampling frequency of the analog to digital converter used is fixed at 25 kHz, which corresponds to a value of 40 μsec. The control sub-cycle is then limited by this value. The total amount of calculations is fitted within this slot. The above three values of interest are then calculated and dispatched to the next calculation stage within this time slot.

It is worthwhile to note that by only calculating the sine component $B_1$ instead of both $A_1$ and $B_1$, the system ends up acting as a compensator for the current harmonics as well as the fundamental reactive power, which is one of the design specifications outlined in the previous chapter.

### 4.2.2.3 Practical results of harmonic current synthesis

The above computations lead to the system implementation for which the following results show its efficiency. These results are shown in Fig.4.3 to Fig.4.8 for the various waveform cases that were applied to the system to test its sensitivity and error analysis. Six different load models were used. The results of each case is discussed

in the following subsections. The results are also compared to the readings, recorded from the power analyser for the sake of comparison.

**Case 1: Purely resistive load (Sinusoidal current waveforms)**

The simplest case of a current waveform applied to the sensing and harmonic current calculation circuit is the pure sinusoidal waveform. This case is illustrated by the waveforms in Fig.4.3. Fig.4.3-a shows the supply voltage waveform with its phase relation with the load current, which in this case is almost sinusoidal. The high frequency noise on the signal is due to the quantisation error of the measuring oscilloscope as well as the sampling noise, which accompanies the analog to digital conversion process. Other sources of noise are due to the fact that the sensing of the sampled current is performed via the Hall effect transducer which introduces an additional amount of noise. The load and supply parameters and characteristics are provided in Appendix C.

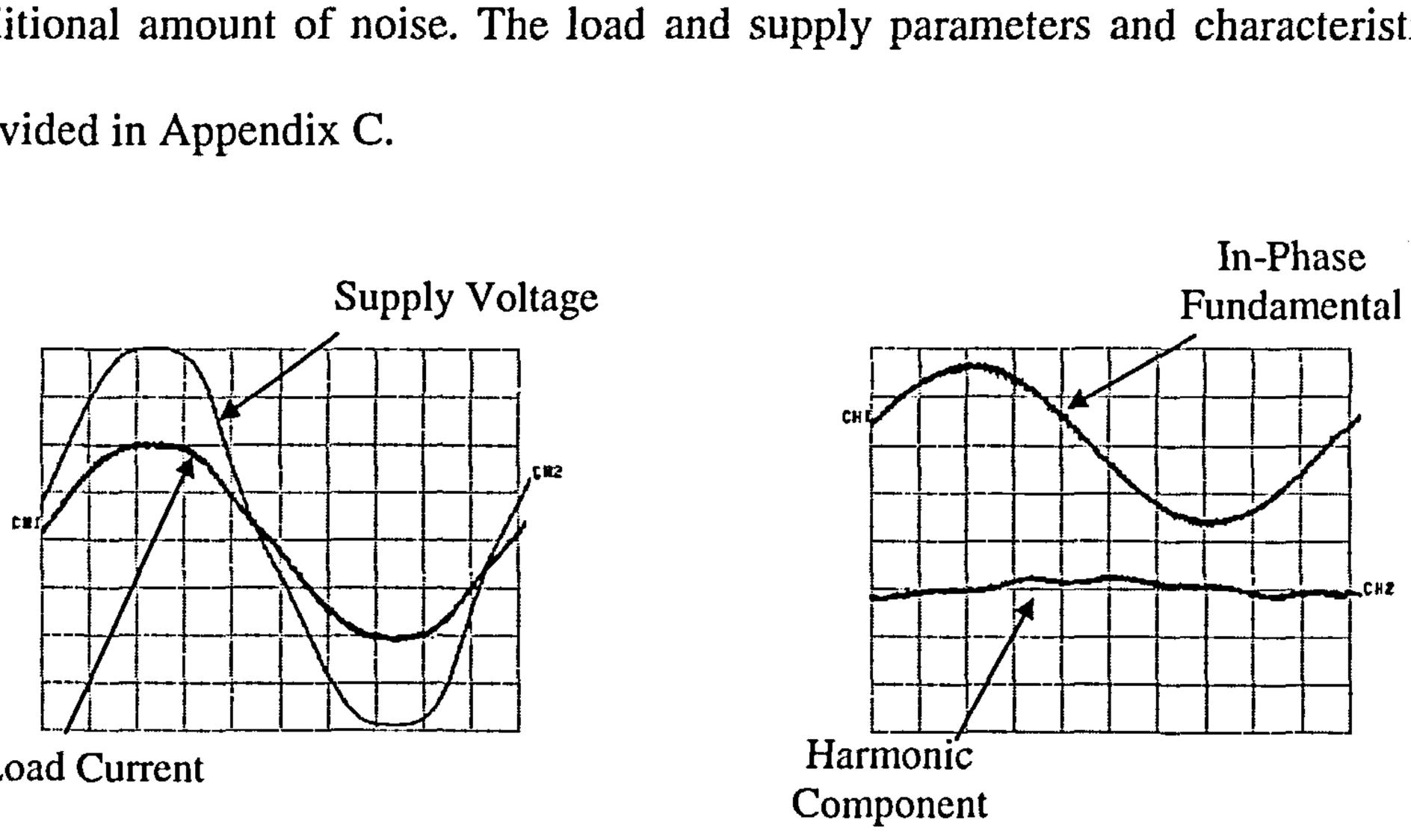



Fig.4.3 : Practical results of the reference current estimator for a purely resistive load

The figure shows a very small phase lag from the current waveform, which is confirmed by the value of 5.9° provided in Appendix C. The second waveform presented in Fig.4.3-b, provides the fundamental load current component, which is in

phase with the supply voltage waveform, The harmonics present in the signal are of course negligible, nevertheless existing, as is clear from the corresponding table in Appendix C.

**Case 2: Thyristor bridge with a resistive load**

Fig.4.4 shows the overall performance of the system under the loading condition of a thyristor bridge feeding a pure resistance. The first figure shows the supply voltage waveform with the load current, which is of course a replica of the output voltage waveform. The change of amplitude present in the voltage waveform signal is due to the voltage drop across the supply impedance. This drop is predominant in this case due to the presence of the finite value of the supply impedance (see Appendix C).

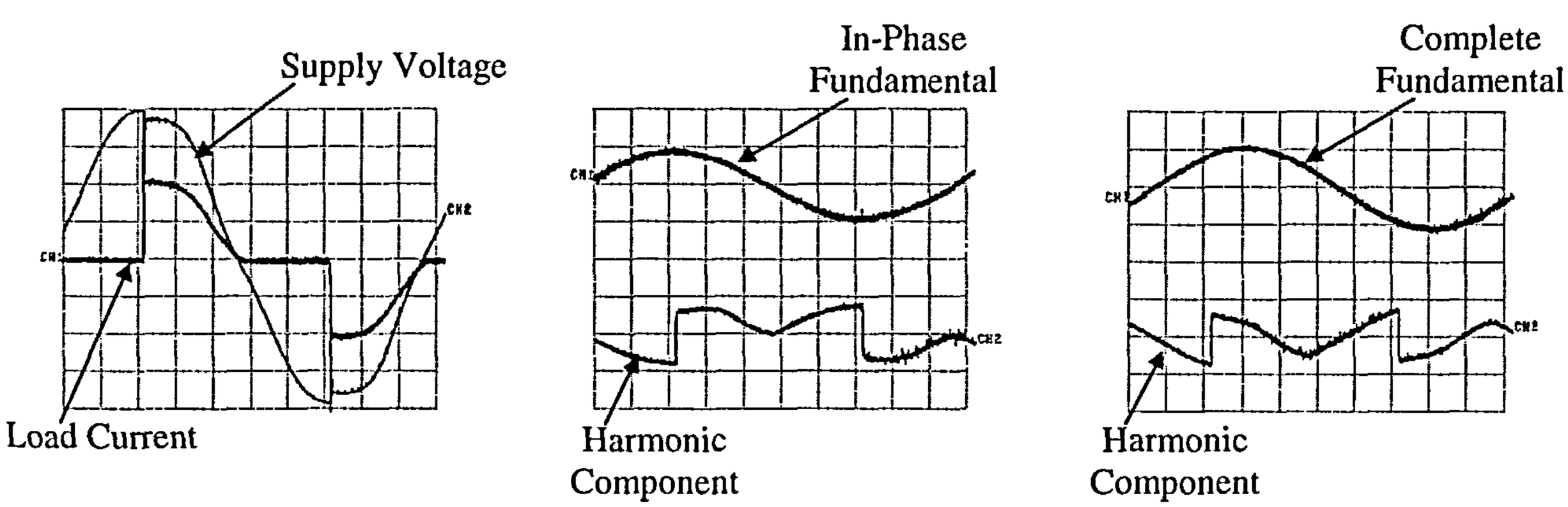



Fig.4.4 : Practical results of the reference current estimator for a thyristor bridge with a resistive load

Fig.4.4-b and Fig.4.4-c show the fundamental component of the load current as well as its total harmonic content. The difference here being the fact that the former presents the fundamental component which is in phase with the supply voltage (i.e., compensating for both harmonics and reactive power). The second waveform is the

result of the calculation of both the $A_1$ and $B_1$ in the assembly language program. The magnitudes and phase shifts presented in this case show a good correspondence with the expected results provided in Appendix C.

**Case 3: Thyristor bridge with an inductive load at minimum triggering angle**

The most common case of load harmonic spectrum is of course the inductive load, which represents most of the industrial loads and conventional dc motor drives. The inductance value used in this case is around 180 *mH*, which is reasonably high as expected in industrial cases. The corresponding current waveform, shown here in Fig.4.5-a in conjunction with the supply voltage, illustrates the smoothing effect of the highly inductive load present on the dc-side of the thyristor-bridge. It is worthwhile to note that the triggering angle in this case is not exactly zero but is a minimum value of around 13° as provided by the triggering module used in this case. The result would thus be a small phase-shift between the fundamental component representing only the harmonics and shown in Fig.4.5-c and that incorporating both the harmonics as well as the reactive power compensation which is in turn shown in Fig.4.5-b.

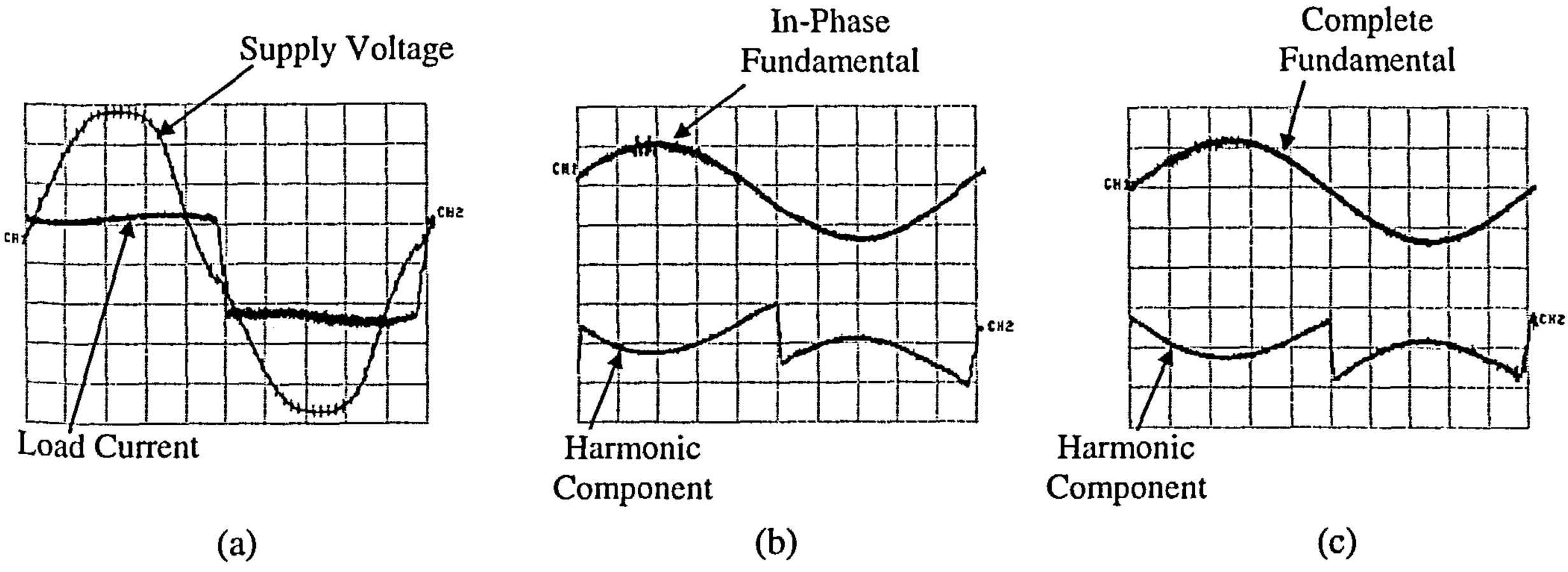



Fig.4.5 : Practical results of the reference current estimator for a thyristor bridge with an inductive load ($\alpha \approx 0$)

A phase shift of about 18° is present between the two waveforms. It constitutes a reasonable value when compared with the value of 18.3° provided in the corresponding table of appendix C for the fundamental component of current. It is also worthwhile to note that the non-perfectly flat-topped waveform results in the presence of distortions in each of the two quarter-cycles forming each of the positive and negative half cycles. The case of Fig.4.5-b, for which the fundamental current waveform is given to be in phase with the supply voltage, suffers from an unevenness of the positive and negative half cycles rising edges. This fact is perfectly correct for such type of waveforms, which confirms the accuracy of the implemented system.

**Case 4: Thyristor bridge with an inductive load at high triggering angle**

Similar to the above loading condition from the point of view of the load parameters and configuration, this case provides a different triggering angle for the load current sensed by the harmonic estimator. For the case of continuous dc side current, the waveform would simply exhibit a phase-shift with its magnitude reduced as shown in Fig.4.6-a. The spikes shown at the transition points are due to the resonance effect

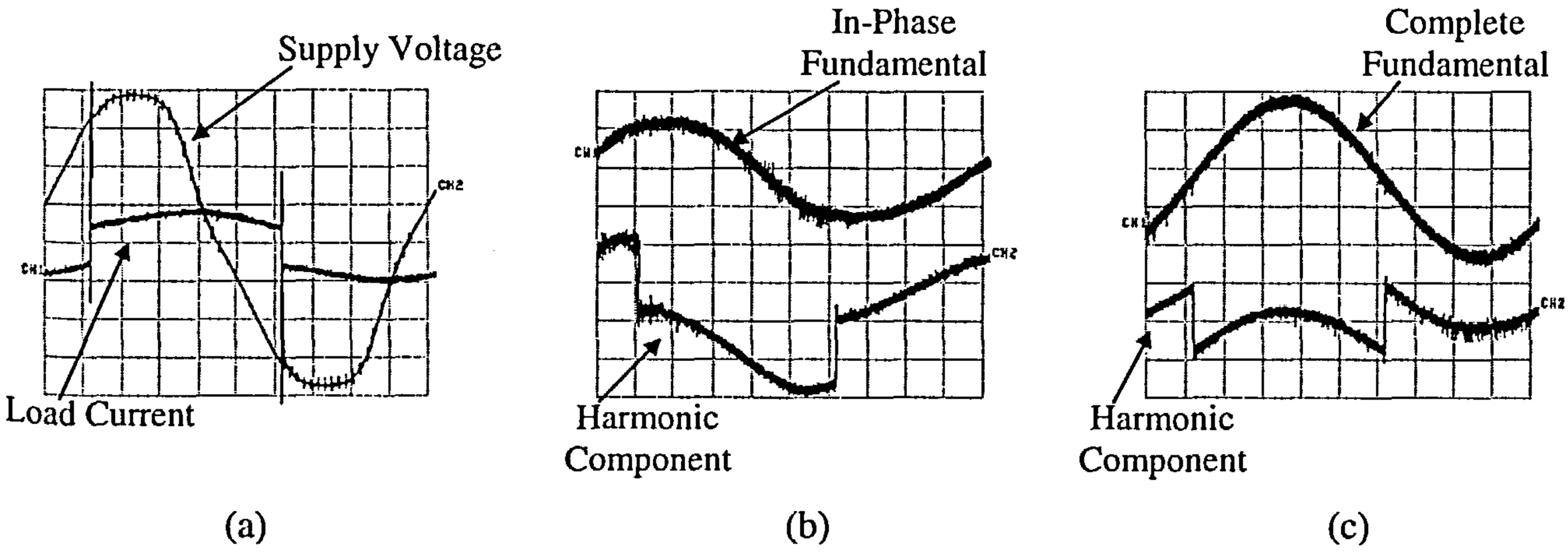



Fig.4.6 : Practical results of the reference current estimator for a thyristor bridge with an inductive load ($\alpha>0$)

between the snubber circuit capacitor connected across the thyristor and the system inductance.

The fundamental harmonic current signal, as presented in Fig.4.6-c, is shown to lag the supply voltage waveform by 59.4° as compared to the value of 58.5° which was measured on the power analyser. The thick traces in this case are due to the measurement noise as explained earlier. The fundamental component which is the result of both the compensation of the harmonics and the reactive power of the load current is shown in Fig.4.6-b. The effect of the noise amplification can also be found in this graph and is due to the same reason as above.

**Case 5: Thyristor bridge with a capacitive load at minimum triggering angle**

However uncommon in practice, this load configuration with a thyristor bridge is tested here for the only purpose of providing the ability to change the wave shape and position of the current pulse as shown in the next section. This condition of small triggering angle is similar to a certain extent to the case of a diode bridge feeding a rectifier dc link capacitor, which is very common in ac/dc/ac converter-inverter units.

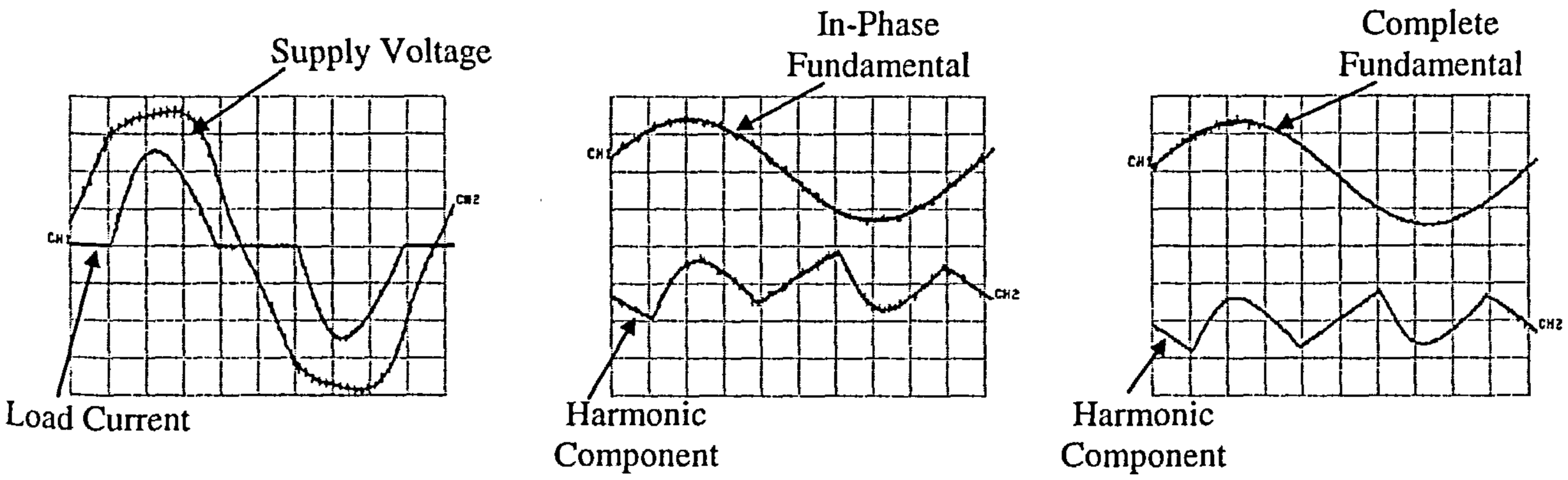



Fig.4.7 : Practical results of the reference current estimator for a thyristor bridge with a capacitive load ($\alpha \approx 0$)

The diode bridge configuration is also used for the ac interface of switched mode power supplies. It is very common in low power applications. Despite the fact that the harmonic pollution accompanying these circuits is very small, they constitute a great danger to the power quality and continuity as discussed earlier in the first and second chapters.

The high amplitude current pulse generated here is shown in Fig.4.7-a for the load current and supply voltage waveform. As is clearly seen in this case, the supply waveform is non-sinusoidal. This would not change any of the system performance except in the case of introducing further harmonics in the load current which in this case would be detected by the harmonic calculation system under investigation. The harmonic currents and the fundamental components, which are corresponding to the two different cases of harmonic and reactive current compensation as well as harmonic current compensation are presented in Fig.4.7-b and Fig.4.7-c respectively.

**Case 6: Thyristor bridge with a capacitive load at high triggering angle**

This load configuration is not at all in use by common industrial applications. However, it is presented here for the only purpose of performance demonstration. The main important characteristic this waveform possesses is its pulsed current during only a small portion of each half cycle. The high amplitude current pulse can be shifted within the mains half-cycle. The width of the pulse reduces when shifted to the right at higher triggering angles. This is the main reason why such a current waveform, shown in Fig.4.8-a, is considered difficult for the fundamental signal estimator and the active filter to compensate since this huge amount of current has to

be tackled fast enough from the part of the reference estimator before the filter can react to its change.

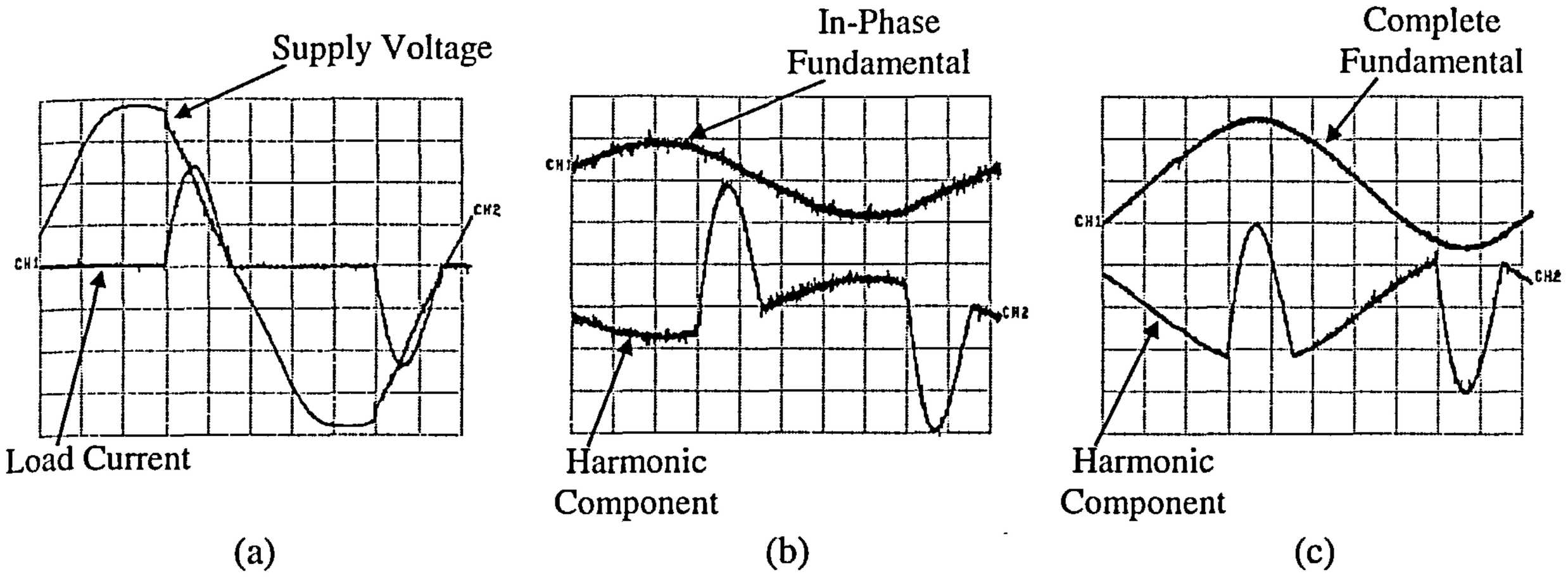



Fig.4.8 : Practical results of the reference current estimator for a thyristor bridge with a capacitive load ($\alpha$>0)

Similar to the above systems, the fundamental components in phase with the supply voltage and that corresponding to the harmonic elimination are presented in Fig.4.8-b and Fig.4.8-c, respectively. The phase shift of 54.6° for the case of the total fundamental current component, corresponds to a phase shift of about 54° in the estimated fundamental signal which is acceptable. The supply voltage in Fig.4.8-a changes magnitude abruptly at the starting point of the capacitor charging process. This large drop is due to the fact that the load current is quite high which interacts with the supply impedance to cause this voltage drop.

### 4.2.2.4 Static and dynamic performance

The proposed reference signal estimator tested above will be used in conjunction with the other system signals to generate the control effort that will drive the PWM

modulator as is discussed in the following sections. It is however important to check the static accuracy of the system for magnitude and phase errors.

The calibration of the measuring system is performed taking into account the values measured for the actual magnitude of the load fundamental and that calculated by the program. In order to compare these values, one needs first of all to calibrate the readings and refer to them directly in Amps. This is performed using the case of a purely resistive load in conjunction with a sinusoidal waveform. The measured value of the calculated fundamental generated current (generated in volts) is used with the magnitude measured with the harmonic analyser for the true value of the fundamental load current. If we divide the latter by the former, we end up with the constant transformation value of

$$I_1^{total} = 1.87\ Amps \qquad \text{and} \qquad \theta_1 = -5.9^{\circ}$$

Hence we can calculate the values of

$$I_1^{\cos} = 0.1922\ Amps \qquad \text{and} \qquad I_1^{\sin} = 1.86\ Amps$$

This implies that the constant value is

$$Constant = I_1^{\sin} / V_{peak}^{computed}$$

$$= 2.325 \quad Amps / peak\ Volts$$

This value is then used to generate Table 4.1. From this table it can be deduced that the percentage error does not at all exceed 0.92 % which is a good acceptable value for the static accuracy of the system.

| Case | Computed (peak Volts) | Computed (Amps) | True Value (Amps) | % Error |
|---|---|---|---|---|
| **1** | 0.8 | 1.68 | 1.68 | 0 |
| **2** | 0.55 | 1.278 | 1.275 | -0.235 |
| **3** | 0.65 | 1.51125 | 1.52 | 0.579 |
| **4** | 1 | 1.1625 | 1.17 | 0.645 |
| **5** | 2.5 | 2.9 | 2.88 | -0.9 |
| **6** | 1.45 | 1.685 | 1.67 | -0.925 |

Table 4.1 : Percentage errors in current magnitude measurements

The measurements of the phase angle errors are performed in Table 4.2. The error values given, show that the maximum error occurs in case 1 with a percentage error of 8.47 %, which seems to be very high. However considering that the absolute error value of 0.5° is equivalent to a time difference of 27.77µsec, it can be ignored. This is due to the fact that the computation time is around 40µsec at a 25 kHz sampling frequency. The system in this case can allow for an error of double the magnitude of the sampling interval, which is of the order of the 1.44°. It is obvious from the table that the system has a maximum value of the error of the order of 0.9° in case 4, which is well within the tolerance band.

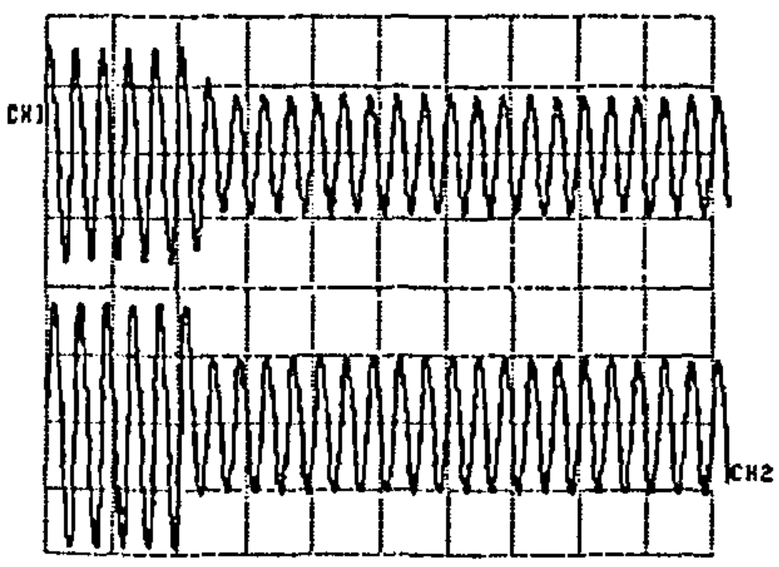
| Case | Computed | True Value | Absolute Error | % Error |
|---|---|---|---|---|
| **1** | 5.4° | 5.9° | -0.4° | -8.47 |
| **2** | 34.2° | 34° | 0.2° | 0.59 |
| **3** | 18° | 18.3° | -0.3° | -1.64 |
| **4** | 59.4° | 58.5° | 0.9° | 1.54 |
| **5** | 4.5° | 4.6° | -0.1° | -2.17 |
| **6** | 54° | 54.6° | -0.6° | -1.1 |

Table 4.2 : Percentage errors in current phase angle measurements

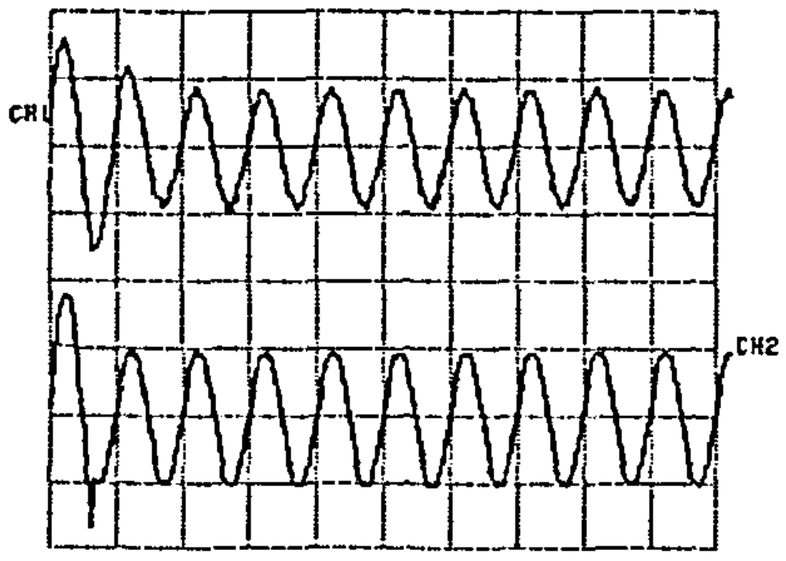
The above error analysis performed on the measured data shows good performance and accuracy characteristics of the proposed system. It now remains to analyse the

performance of the system from the point of view of dynamic performance. The system in this case while performing a one-cycle integration is expected to have a tracking error for a sudden signal change with a maximum value of one whole cycle for zero estimation error.

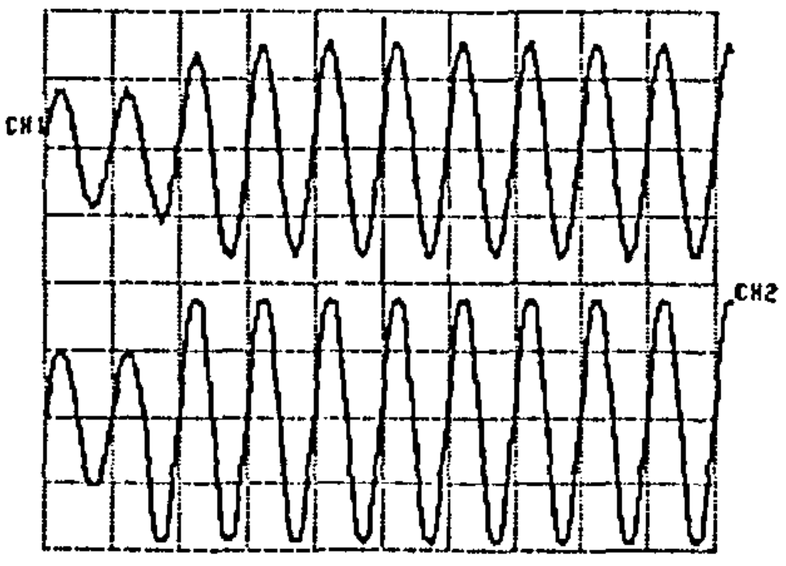
Consider the proposed system with a fast changing load as given in Fig.4.9. The various cases outlined show that the performance of the system is rather satisfactory and that the error reduces quickly with time. For cases like Fig.4.9-a, Fig.4.9-b and Fig.4.9-c, which have a step-change in the load current magnitude, either increasing or decreasing which affects the computation process. It is noted from the curves that the maximum error occurs for a graph like the one in Fig.4.9-b, in which the load current changes near the peak value of the sinusoidal waveform. In this case a reasonable error value within 10% can be obtained within one half-cycle.



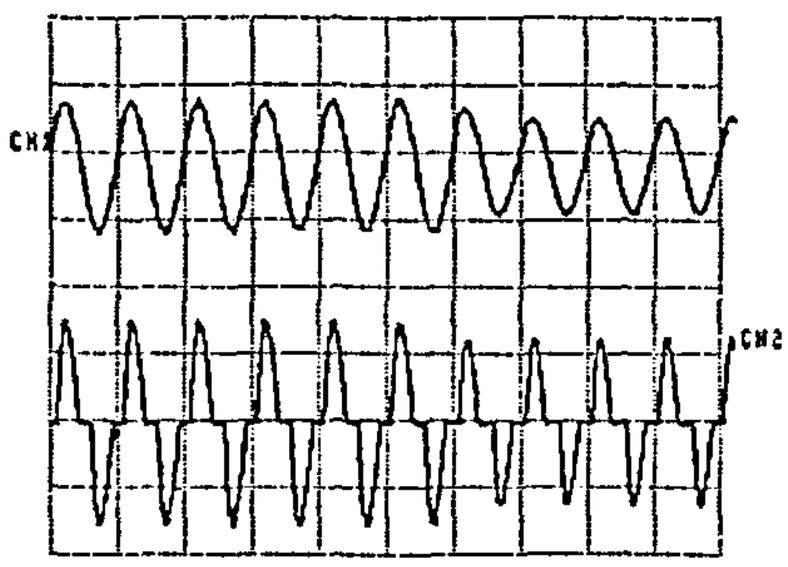

(a) Sinusoidal Load Current



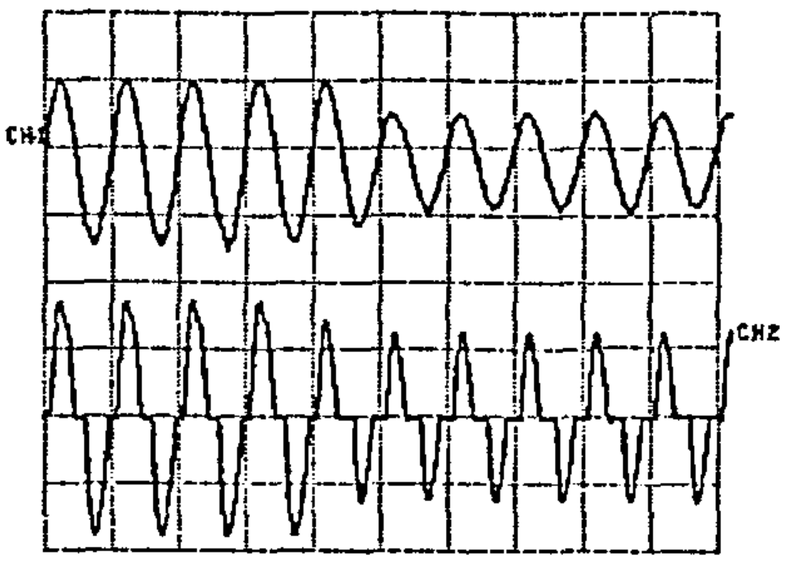

(b) Sinusoidal Load Current




(c) Sinusoidal Load Current




(d) Rectifier-Bridge with Capacitive Load Current




(e) Rectifier-Bridge with Capacitive Load Current

Fig.4.9 : Practical results of the reference current estimator with dynamic loading conditions
CH1: Calculated Fundamentals - CH2: Load Current Waveform

Fig.4.9-d and Fig.4.9-e show a slowly varying resistive load connected across a rectifying bridge with a reservoir capacitor on the dc side. Part of the resistance is being switched out of the circuit. The current decay is not instantaneous, which gives the estimator reasonable time for calculations to settle down. This mild condition is more expected in the cases of power system applications with slow changes (in the order of msec). This same computational response is the case for all other systems, which employ an integration process to calculate either the Fourier coefficients or the instantaneous average power of the load. Nevertheless, the proposed system performs satisfactorily with slowly varying loads. The time it takes to reach a reasonable amount of error would be in this case comparable to the load variations and hence a minimal error can be expected out of the system.

## 4.3 Global system controller

The reference signal generated from the PC used to calculate the total instantaneous current harmonic signal $i_h^*$ is numerically differentiated and multiplied by the value of the filter inductance. The resulting $L\,(di_h^*/dt)$ is then used as the reference for the controller. Referring to Fig.4.10, this signal is transmitted to a second PC. The second PC will serve as a controller as well as a PWM modulator as will be exploited in the next section. This PC is equipped with a general-purpose analog and digital interface board (PCL812-PG) similar to the one used in the first PC. It also includes a general purpose 48 bit digital input output lines which are programmable according to the Intel 8255 Programmable Peripheral Interface (PPI) conventions. A third custom-built general-purpose interface card is used to manage the interrupt signal generated by the Intel 8254 (triple general purpose multi-mode programmable timers), located

on the digital input/output board mentioned above. These timers manage the constant programmable switching frequency of the PWM as well as the PWM process itself.

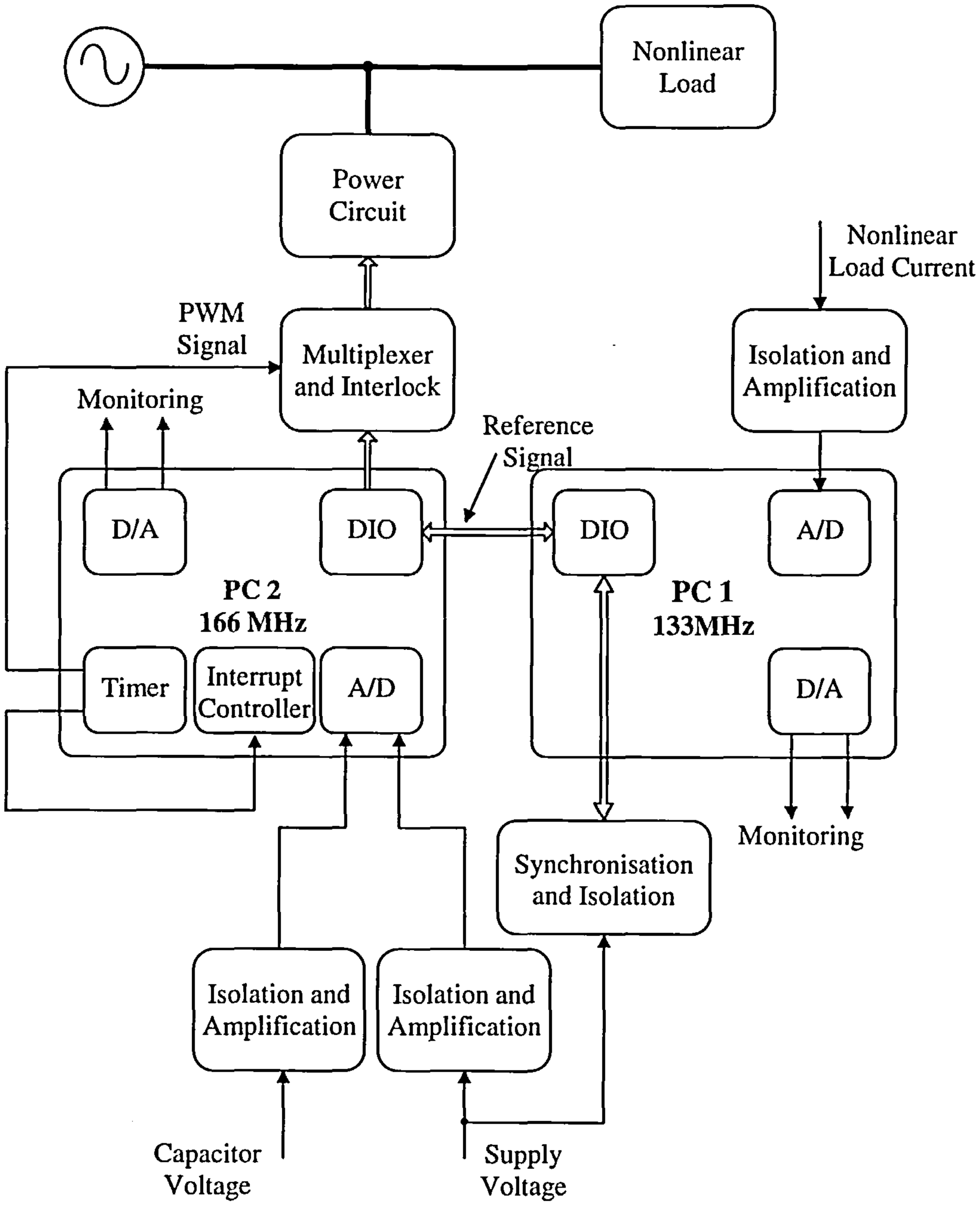



Fig.4.10 : Practical Layout of the proposed system

The reference current acquired by the second PC, through digital interface and handshaking, is then processed at the instant of the PC interrupt in conjunction with the actual signals that are obtained through the digital to analog acquisition card. These signals are the instantaneous sampled supply and filter capacitor voltages, which are sensed and isolated through custom built Hall Effect voltage transducer circuits. These are then amplified and signal conditioned to be properly interfaced to the analog to digital interface terminals.

As outlined in chapter 3, the reference signal is added to (or subtracted from) the supply voltage signal according to the acquisition polarity. This process includes the actual supply voltage waveform into the calculation process of the control effort. This will in effect cause an extra stability and adaptability of the proposed circuit control algorithm. This is due to the fact that by incorporating the supply voltage waveform which in most cases is not at all sinusoidal, will cause the tracking mechanism to be immune from the supply voltage waveform signal variation. This leads to better performance in weak power systems where the supply voltage waveform under certain operating conditions does not assume a sinusoidal waveshape. The controller will then track the required system voltage and use it as one of the references for the controller implemented.

The controller design, which is not under investigation in the course of this work, assumes the simplest possible form available which is the Proportional (P-type) controller. The control reference calculated above for the capacitor voltage is subtracted from the actual value, which was acquired by analog to digital conversion

from the external sensor and signal conditioning circuits. The resulting control effort will then drive the PWM modulator discussed in the following section.

## 4.4 PWM generation

A simplified pulse width modulation strategy was used in the system implementation in order to demonstrate the principle of operation of the circuit. The PWM block diagram, implemented in this case as a combination of both software and hardware, consists of the software calculation of the desired pulse width from the control effort as well as the PC used for the control purposes with all its three ISA interface cards.

The assembly language program used for the purpose of the PWM generation as well as performing the control of the system is presented in Appendix D, with its flow chart shown in Fig.4.11. The implemented system relies on the generation of an interrupt signal with a pre-programmed frequency through one of the channels of the general-purpose timer. This interrupt takes up one of the unused interrupt services defined for the PC motherboard. The priority of this interrupt is unimportant since the program is not performing any parallel access on any of the other devices of the computer. The interrupt service routine operating in this case starts by performing the control process as outlined in the previous section. The resulting control effort is then subjected to a linear control law, which provides the required pulse widths by the system for this particular value of control effort. The pulse widths have then to be translated into the corresponding initial values of the counter, which operates on a basis of an on-board 8 MHz clock.

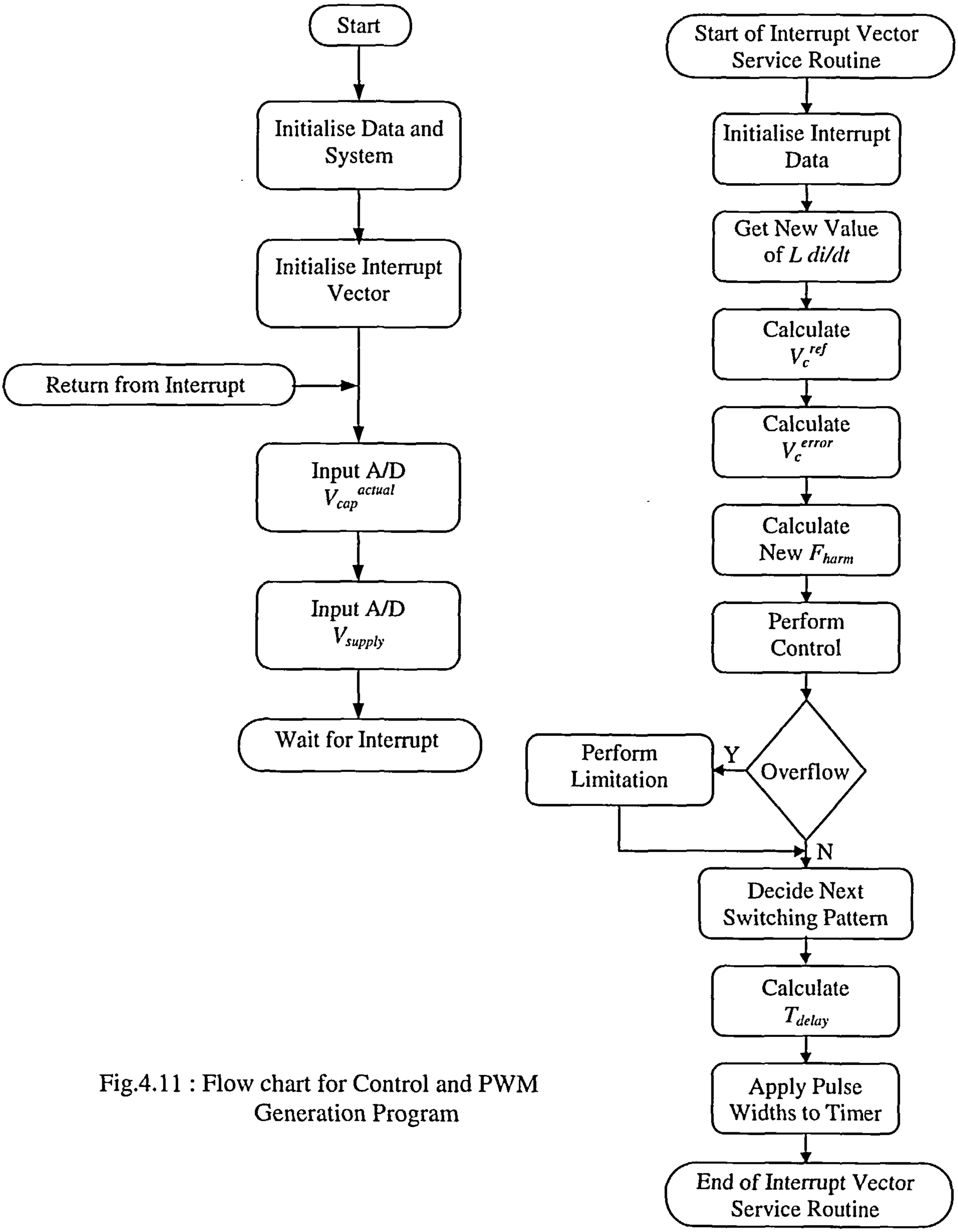
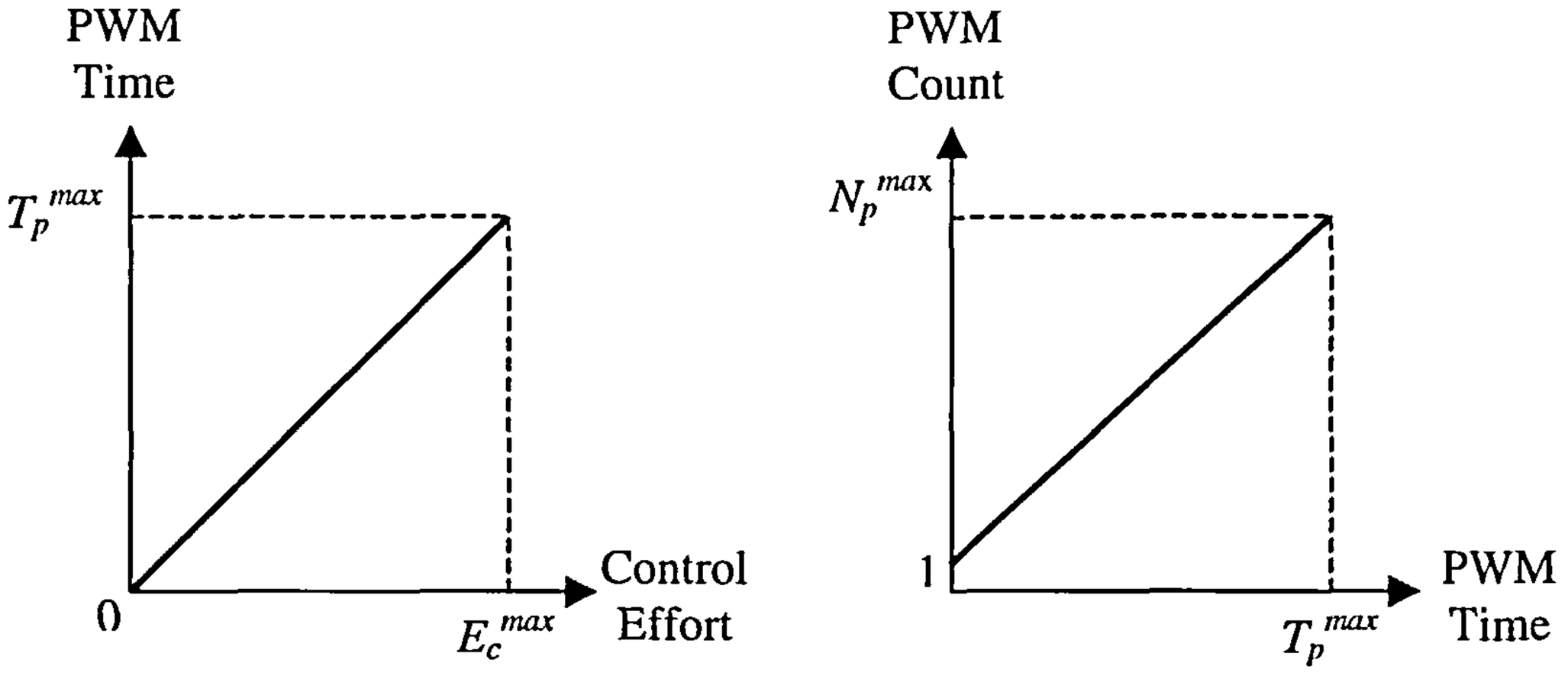



Fig.4.11 : Flow chart for Control and PWM Generation Program

In other words, the control effort is subjected to the graph of Fig.4.12-a to calculate the pulse-width, which is then applied to the graph of Fig.4.12-b to generate the count




(a) (b)

Fig.4.12 : Relation between the control effort and the PWM of the switches

number that is necessary to be downloaded into the timer initial count register and immediately start counting. The pulse generated from the timer drives an external custom-made circuit, which uses these continuous pulses to drive the modulated switch. The signal is re-routed to the particular modulated switch under question depending on the decided switching polarity provided by the software and generated on the digital output port of the PCL812-PG. These signals are then used to directly drive the semiconductor switches via opto-isolation and buffering stages

The modulation switches can then allow enough current into the charging inductance and eventually to the filter capacitor through the corresponding direction switches. The main role of these direction switches, in this case, is to prevent the charge on the capacitor from being fed back into the charging inductance. Care must, however, be taken to ensure that the polarity reversal of the auxiliary switches does not interrupt a current path through one of them. It now remains to show the results of the practical

system regarding the filter capacitor voltage and current as will be presented in the next section.

## 4.5 Overall System Implementation

The proposed active filter and its control system are implemented practically in a laboratory prototype and tested to prove the feasibility of the proposed idea. As shown in Fig.4.10, the system consists of two Pentium PCs running at 133 MHz and 166 MHz respectively and equipped with all the necessary and special interface hardware as well as the sensing, isolation, signal conditioning and PWM control circuits, in addition to the metering devices. The power circuit in this case was built as a scaled version of the full rated system.

The load considered in this case is the severest case of a capacitive-load on the dc-side of a thyristor rectifier bridge. The thyristor-bridge enables the change of the waveshape of the nonlinear load current. The active filter when able to perform its task on such a waveform should be able to perform even better on much easier waveforms with a lower frequency content. These waveforms would be easily modified into their corresponding sinusoidal fundamentals. The load current waveform, in conjunction with the supply voltage, is shown in Fig.4.7-a, presented earlier. The load current assumes the peaky shape approximately at the middle of the mains half-cycle with zeros elsewhere. The harmonic content of this waveform is given in Fig.4.13 in the frequency domain with the time domain current waveform presented in the top graph.

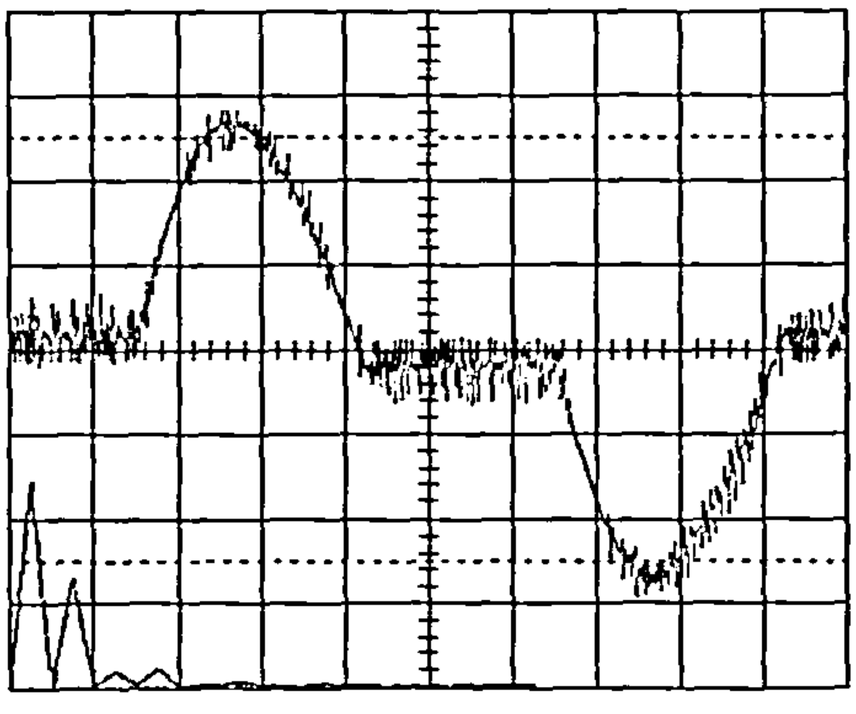


Fig.4.13 : Practical results for load current waveform

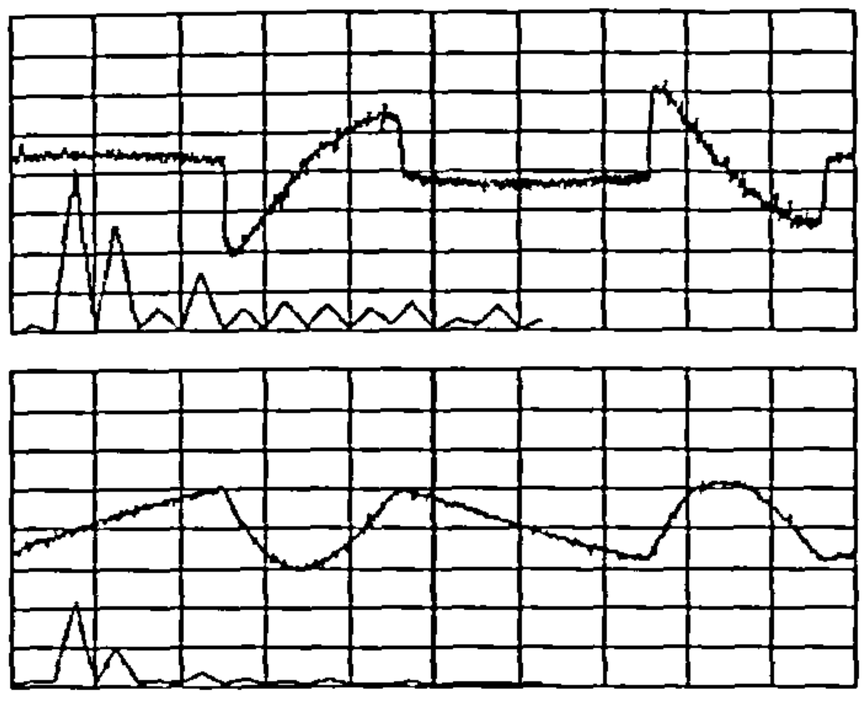


Fig.4.14 : Practical results for load current harmonic signal (bottom curve) and its derivative (top curve)

The scaled value of the rate of change of the harmonic current is given in Fig.4.14, in conjunction with its harmonic amplitudes in the top graph. The total harmonic current of the nonlinear load is presented in the lower graph with its harmonic spectrum, considering in this case only the harmonic elimination problem. It is seen that the system assumes a certain amount of noise around both signals. It is worthwhile to note that this noise superimposed on the measured signals is due to the measurement and quantisation noise by the analog to digital acquisition devices of the digital storage oscilloscope.

The effect of differentiation error can be reduced by employing a four-to-one scaling of the reference signal time domain for every four successive amplitudes. This is made possible in this case since the operating frequency of the data acquisition system is 25 kHz while the system operates around 6 kHz. With a slight modification in the harmonic compensation program used above, the compensating reference current is shown in Fig.4.15 for the combined case of power factor correction and harmonic elimination. This case will be analysed in the following paragraph due to the extra difficulties it imposes on the system controller.

Fig.4.16 demonstrates the supply voltage waveform with the actual value of the capacitor voltage. This waveform is similar to the simulated results of the capacitive loading condition presented in the last chapter (Fig.3.39-d). It is worthwhile to note that the supply voltage waveform is not sinusoidal. It however assumes a limited voltage drop in the middle part of each half cycle due to the load current flowing in the circuit and the finite value of the supply impedance. Such a non-sinusoidal waveform has a major effect on the compensated supply current as is explained later on in this section.

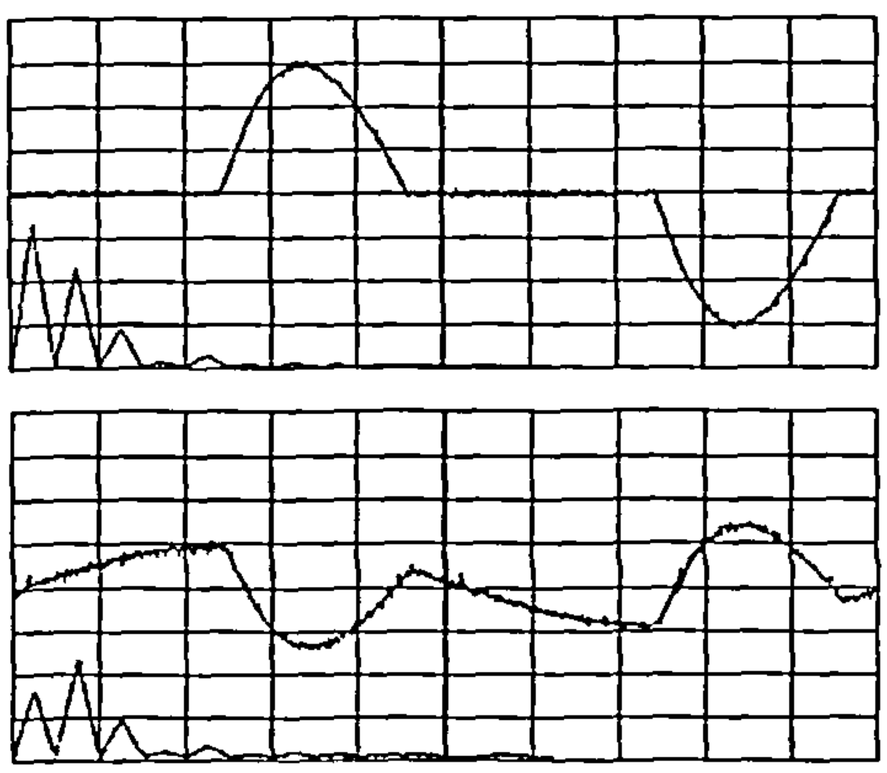


Fig.4.15 : Practical results for load current waveform (top curve) and its reactive and harmonic content (bottom curve)

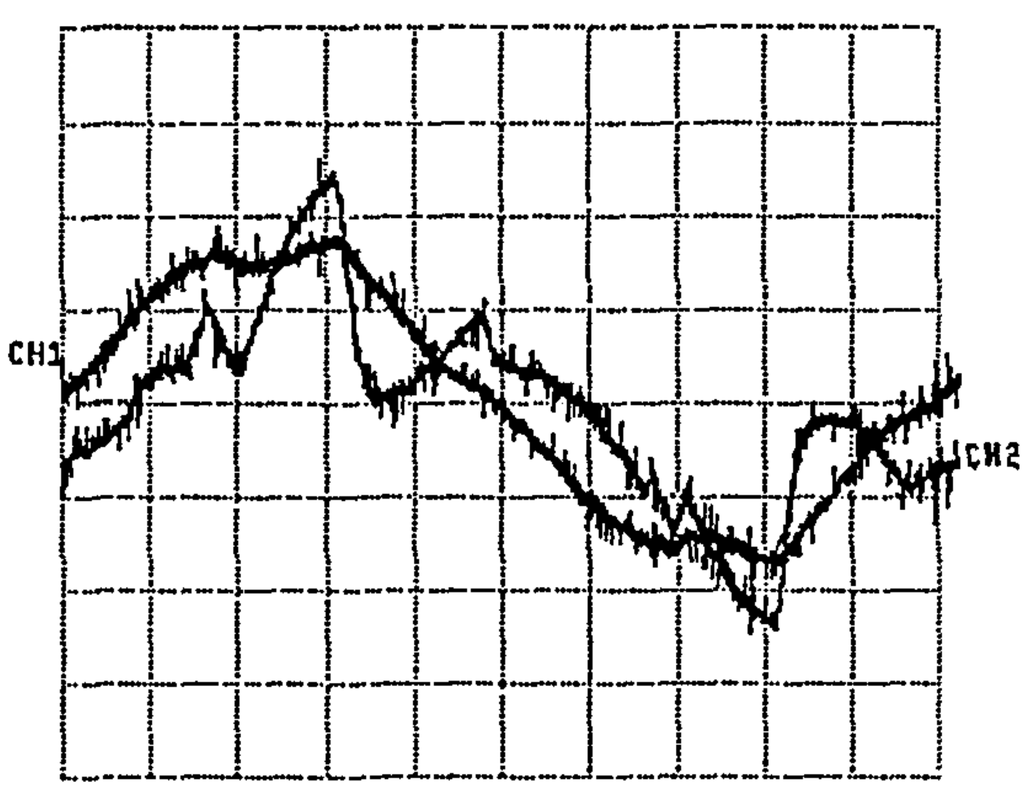



Fig.4.16 : Practical results for supply voltage waveform (CH1) and the filter capacitor voltage waveform (CH2)

It is shown (Fig.4.16) that the controlled voltage is tracking its reference value within limits imposed by the limitations of the limited gain P-type controller and the problems presented by the PC as a non dedicated controller as will be discussed in the conclusion. Consequently, the controlled filter current is shown to track, to a certain extent, its reference value of Fig.4.15 as in Fig.4.17. The filter current is shown to have a superimposed fundamental component, which is manifested by the

fundamental component of the Fourier frequency spectrum of the signal. This fundamental frequency component is due to the tracking error between the actual value of the capacitor voltage and its calculated reference. This is one major limitation imposed by P-type controllers used. A more elaborate controller can improve the case and provide better results for the system performance.

The supply current waveform after the compensation is shown in Fig.4.18. In this case, the system manifests the tracking problem discussed above with the fundamental current component affecting the resulting waveform. The large amount of noise across this signal is due to the fact that the measurement of the supply current in this case was performed on a non-earthed floating shunt resistor of 0.1 ohm. This of course introduces huge amounts of noise for this particular case, while the other measurements are performed referred to earth using isolating Hall-effect current transducers.

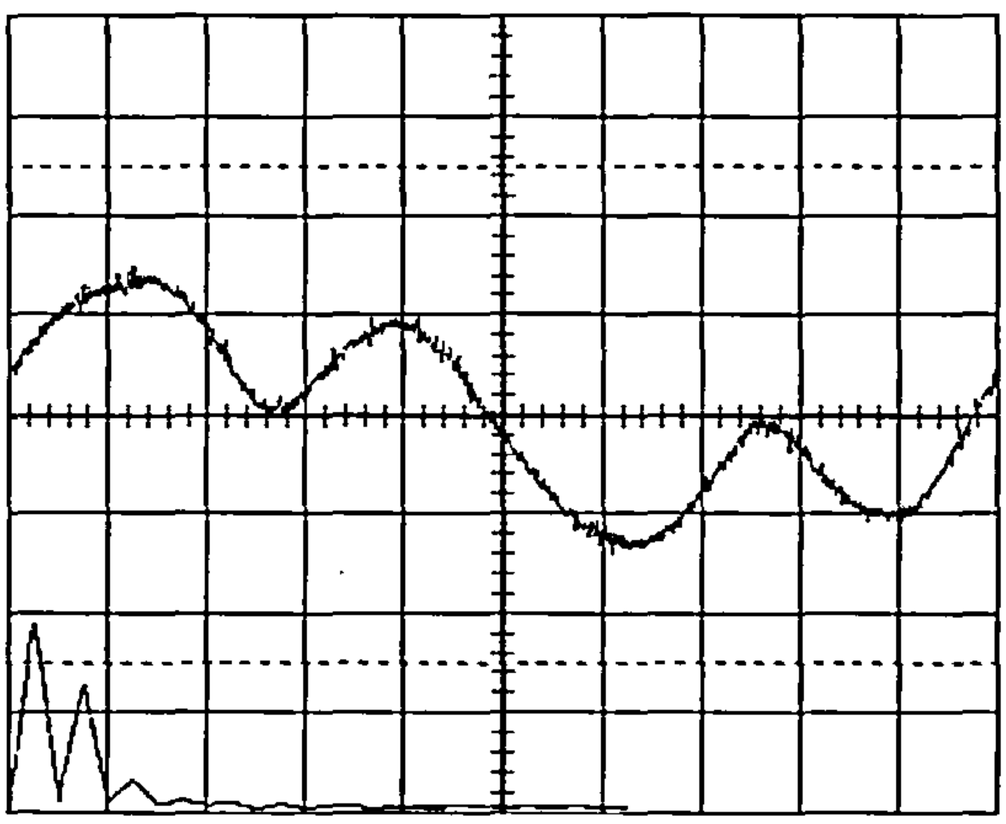


Fig.4.17 : Practical results for filter current waveform

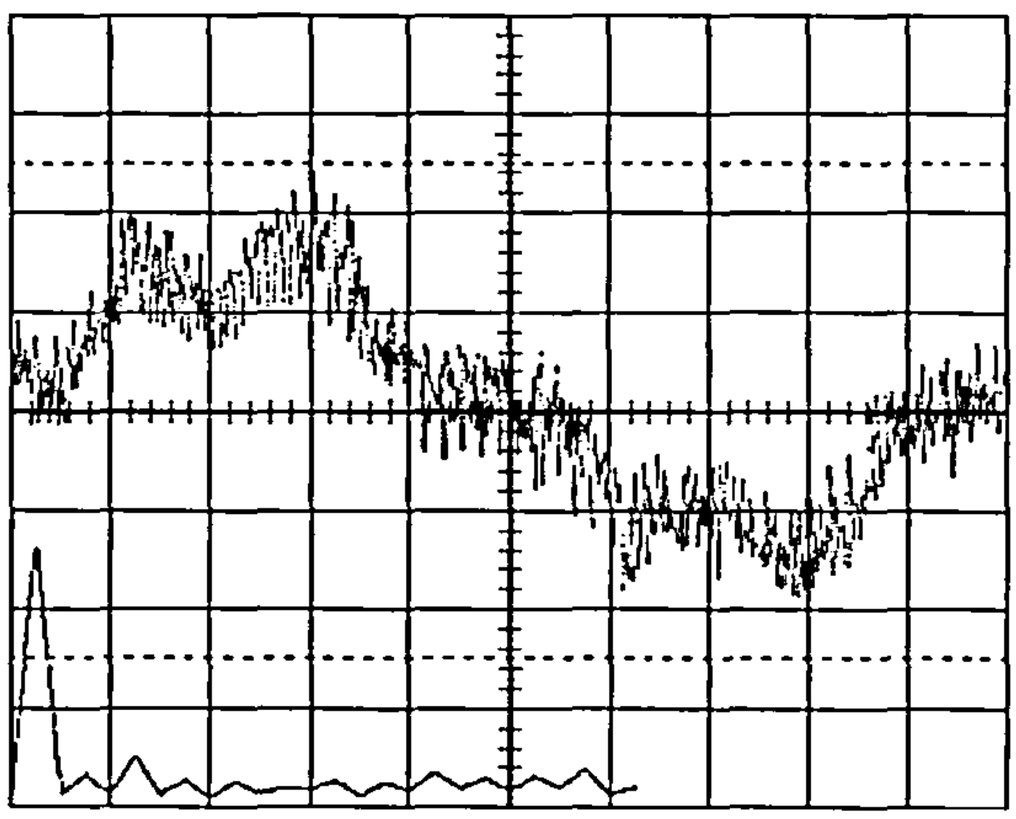


Fig.4.18 : Practical results for supply current waveform after filtration

The supply current waveform, despite its odd waveshape, shows the effort performed by the active filter to change the highly nonlinear and non-sinusoidal waveform of

Fig.4.13 into the above waveform. The dip in the supply current waveform around the middle of each of the two half-cycles, conforms with that outlined above for the supply voltage waveform. This fact confirms the frequency domain analysis of the previous chapter, which states that the filter, in conjunction with the control law adopted, can not contribute to the compensation of the effects of the supply voltage harmonics on the load current harmonics.

The above results show good correlation with the theoretical basis outlined in the previous chapter. The system despite the weak P-type controller can still track the reference signal and generate the appropriate waveforms for the capacitor voltage and the filter current. The filter operates rather satisfactorily from the point of view of eliminating the current harmonics, as tested above, under the severest nonlinear load harmonic conditions. This implies that the system performance under better loading and supply conditions would be much better than the case outlined in this text.

## 4.6 Summary

This chapter presented the hardware implementation of the proposed active filter system. Each block, from the block diagram of Fig.2.1, was realised. The current reference estimator was realised using a modified Fourier analysis technique. The implementation of the PWM control strategy and the overall system controller were also performed. These were applied to the power circuit to produce the practical results outlined above. These results match to a great extent the simulation results obtained from the simulation of the proposed system presented in the last chapter. The final conclusions of the whole thesis now follow in the fifth and final chapter.

# Chapter 5

# Conclusions and Future Work

# Chapter 5

# Conclusions and Future Work

## 5.1 Conclusions

Active filters will soon constitute a great deal of importance in our present life, as stated earlier with the presence of the huge amounts of nonlinear and time varying parameter loads. The survey of published papers presented in the second chapter of this thesis represents a broad and detailed analysis of all the available systems used for active filtering. The subdivisions, provided in that chapter, represent important and simplified guidelines to identify the present state of the art filtering techniques. They also serve to observe the points of strength and weakness of each. This was very helpful in identifying the proposed system characteristics, which were then discussed and realised in the third chapter of this thesis. These subdivisions can be followed to identify the points lacking research investigation in the present state of the art technology of active filtering.

It is important to classify the proposed circuit under the available configurations. By taking a closer look at the configurations outlined in chapter 2, we can spot immediately that the proposed circuit lies in the range of low to medium power applications with single-phase or three single-phase configurations. It also lies under the category of non-inverter circuit type of shunt active filters. The circuit may be seen similar to lattice structures. However, by taking a closer look, it can be identified that the presence of the LC circuit, which is permanently connected to the supply, brings the system into a new class of configurations involving the "dc voltage

regulator" type circuits. This type is then added in conjunction with the switched capacitor and lattice structure techniques.

The compensated variables that can be handled using this circuit, as outlined according to the analysis of chapter 2, are the current harmonics as well as the reactive power compensation of nonlinear loads. In three single-phase configurations, it can also be used for balancing three-phase supply currents.

From the control-technique point of view, the closed-loop control of the system will take a different perspective. Since the reservoir capacitor voltage control is not applicable in this case, the system will employ a voltage tracking mechanism for the reference generated by the harmonic current estimator algorithm. This technique can then be classified as a new subdivision under the title of "linear output voltage tracking control".

The detailed analysis of the system provided in the third chapter provides a good basis for the simulation of the system performance and the visualisation of the behaviour of each part of the circuit. They also provide an insight into the performance and parameter determination of the power circuit components. The approximate equations presented determine to a great extent the circuit parameters used in the system implementation. The deviations from these values are mainly due to the nonlinearities neglected during the approximate analysis of the system. These equations provide main guidelines for the design as well as for resonance considerations.

The frequency domain analysis and model of the proposed filter provides a strong backup for any further system analysis. The controller and compensator designs can only be undertaken based upon the presence of a system model. The frequency domain analysis of the active filter performance in the power system provides a strong backup for the choice of the correct control law used in the proposed active filter. It also proves the validity of the undertaken reference control law. The analysis shows that by incorporating the voltage at the point of common coupling into the control equations, the system can overcome various problems caused by the presence of harmonics in the supply and load sides. This is very important since the detailed monitoring of system power supplies, as provided in the literature, has proved that the presence of non-sinusoidal voltage waveforms can cause various amounts of damages to the performance of other power system components.

The system with this feedback is rendered immune to any supply voltage variations. Moreover, it is worthwhile to reiterate that the supply harmonics are faced in this case with infinite impedance and can not consequently force any harmonic circulating currents into the filter system. This would eventually have the main advantage of reducing the system losses and hence increasing the transmission and distribution efficiencies of the power system.

The characteristic equation of the modelled system in this case is independent of the supply impedance. This in effect shows that the proposed system is able to perform as designed without any reference to or need for supply impedance measurement, which faces system designers with great difficulties due to its continuous variation with various loading conditions. The only variables of interest, which determine the

characteristic polynomial of the system, is the filter impedance which is under the control of the system designer.

The implemented algorithm for reference harmonic signal generator, demonstrated during the course of this research, proves to be well suited for this specific application. If properly implemented on a powerful platform, it can serve as a new fast-method for the generation of the harmonic signal necessary for the filter operation. The response-time of this block is delayed by a maximum of 80 μsec which incorporates the acquisition time (analog to digital conversion delay) as well as the computation time during the following subcycle which amounts to almost the same value. The system in this case can provide an accurate generation of the overall harmonic content of the load current with a fast dynamic response limited only by the averaging process of the integration necessary for calculating the Fourier coefficients. This problem is of course the same for any other technique employing an integration process. The main advantage here is that the system implementation is quite simple and is not very time-consuming when using fast accurate processors capable of performing millions of floating-point operations per second. The numerous test results provided show that the system is robust and accurate for all the different waveforms presented during the course of the fourth chapter.

Moreover, by implementing the harmonic current estimator in this way with much faster processing and shorter calculation times, a larger number of sampling points can be used without degrading any of the system characteristics. The larger number of points can then be used to reduce the effect of noise and numerical differentiation. Comparing this case with the ordinary FFT algorithm, implemented for calculating all

the harmonics, the proposed system supersedes by its ability to incorporate a larger number of samples per cycles according to the hardware capabilities of the processor and the data acquisition system.

The simulation and practical results, presented in the third and fourth chapters, show that the proposed single-phase active filter performs satisfactorily from the point of view of generating the required current waveforms that will minimise the load current harmonics. The results obtained from simulation and practical results show a good match. The main disadvantage, as shown by the graphs and discussed earlier in the previous chapter, is the controller which would enable the system to operate at a much higher performance level if properly implemented as a robust, a sliding mode or an adaptive controller.

For the purpose of providing a proper dc-link that can be used by the dc-regulator to perform the required voltage control over the output capacitor, the proposed system uses a rectifier bridge, which feeds two dc capacitors. The harmonics, generated by this charging circuit, are negligible compared to the values normally available in the load current waveforms. The current flowing through this bridge circuit is considered as being an additional harmonic current, which can be compensated for by the filter since its effect is taken into the current reference when the load current is sampled. The reason for this, lies under the fact that the two ac terminals of the bridge are located on the load side and not on the supply side.

It is to be noted for this first prototype of the proposed system, that the implementation of the proposed active filter reference generation and controller in

which the PC was used as a system controller, does not prove much success. This is related to the fact that the PC, which is not a fully dedicated processor, is normally busy doing other tasks, ranging from the dynamic memory refresh as well as serving the Microsoft Windows 95 operating system (running in the background). The main obvious proof for this case is the fact that the external interrupt used in the circuit implementation of the PWM technique is responded to only after the privileged system software (of level 0, 1 and 2 in Pentium multitasking shared memory management system) have checked any of their need for it. The result is a delay of over 20μsec in the initiation of interrupt service routine. This case is dominant when operating the system with Microsoft Windows 95 in the background while the system control program is running in the foreground. The initiation of a full DOS-session in Microsoft Windows 95 systems is not at all discarding this problem since the windows kernel program is still running in the background and monitoring all the processes being performed to the system.

Due to the above problems, the continuous operation of the system is not practical under PC control. The continuous interruption of the operating system running in the background as well as the computer BIOS initiating system IRQ0 interrupt for dynamic memory refresh, leaves the transistor switching system without any control, for a few hundreds of microseconds, at the last switching state. This case may be tolerable with the presence of one single PC using a DOS based machine, which does not run Microsoft Windows 95. However, the fact that the system uses two PCs in cascade worsens the problem, which eventually becomes dominant. This problem will incur a system loss of control over the capacitor voltage for short periods of times every refresh cycle of the PC. The resulting filter current drawn from the supply is

then deviating away from its reference. When the program regains control of the PC, the tracking tunes back as quick as possible into the new value of the output filter capacitor reference.

The above problem is persistent and dominant on the system implementation. However, the main reason behind using the PCs for this phase is to prove the basic idea of the power circuit operation and control algorithms, which can then be implemented in a next stage as is discussed in the following section, involving the proposed future work.

## 5.2 Suggestion for Future Work

The analysis outlined in this thesis for the synthesis, design and implementation of the new power circuit configuration in conjunction with the reference generation mechanism provides a basis for further improvements to the system. Following the implementation of the first prototype of the proposed system, the following can be pursued in the same field to improve the system usability and applicability:

- The implementation of the above system using PCs as controller is not a proper solution for an industrial project. This fact was demonstrated earlier by the problems accompanying the system in addition to the fact that such a system is bulky and expensive. The better solution would then be to implement this system using a dedicated processor board that is designed to handle the computational and control tasks required by the system. The system can use one of the modern Digital Signal Processors (DSPs) provided in the market by several manufacturers. Two excellent examples of such systems are the 1600 MIPS TMS320-C6200 DSP and the 1000 MFLOPS

TMS320-C6700 DSP, both introduced recently by Texas Instruments. The main disadvantage of such a system would of course be the initial cost, which normally amounts to several thousands of pounds for the development boards and the necessary accompanying software and hardware.

- The applied PWM technique for the prototype built was set to be as simple as possible since it was implemented in a linear process. The investigation of better techniques using nonlinear switching characteristics can follow the above analysis. This would eventually show better system performance.
- The suggested PWM technique in the previous point uses feedforward algorithms, which have their own disadvantages for the tracking of the reference voltages and currents. An investigation of the implementation of modified hysteresis voltage control, suitable for the proposed circuit, can now follow.
- The circuit presented in this thesis serves as a single-phase configuration, which is designed to perform the active filtering task in only one single-phase. The generation of a three-phase version of this circuit would then necessitate the presence of 12 power switches, which is double the number used by conventional inverter configurations. This is not a major problem, since the presence of a triple version of this circuit has the advantage of the system capability of compensating for the phase unbalance and dissymmetry.
- The connection of the proposed circuit in parallel to the load was investigated during the course of this research. Another alternative can also be sought if the proposed circuit is connected in series with the supply. The control of the voltage applied across the terminals of the capacitor would then ensure the compensation of voltage harmonics present in the supply at the PCC. This

case may be as important as eliminating the current harmonics. This system, used in a three-phase configuration, can also be used to balance the supply voltage which may be uneven or out of sequence due to abnormal system conditions.

- The idea of combining the above series compensator in conjunction with the available shunt configuration can yield a series/shunt configuration which can be exploited in harmonic elimination and balancing of supply voltages and currents. The resulting system would then be seen as another configuration for FACTS, which is a case of extreme importance in the present power system control.
- The proposed single-phase circuit, as shown in chapter 3, can be used in other applications not involving active filters. Such applications may include power amplifiers, as already presented, as well as supply interfaces for non conventional energy resources (wind and solar energy), without the need for the presence of additional active filtering means.
- Other configurations can also be investigated for the above circuit to perform the same task, which may include a lesser number of power switches used. This would encourage an immediate implementation of an industry practical prototype for single and three phase compensator systems.
- The proposed circuit was mainly presented here in this thesis from the point of view of power electronic and system implementation. The analysis of the circuit from the control and modelling point of view can then follow the above which can lead to generating a theoretical continuous or discrete time mathematical model serving as a main building block for further analysis and improvements to the controller.

- As an alternative to the bridge rectifier, an additional switch, diode and inductor can be added to the system. This switch in conjunction with the inductor when connected on the dc-side of the rectifier-bridge can be controlled to operate as a unity power factor sinusoidal input rectifier, which does not generate any low order harmonics. The determination of the reference current magnitude, which is controlled via the capacitor voltage, can be processed individually from the filter control process using a small processing unit responsible only for this function. The rating of the switch used would not be high, due to the fact that the voltage drop of the two capacitors is only due to the switching and circuit copper losses.
- Finally, the use of neural networks, fuzzy logic, robust, sliding-mode and/or adaptive controls to implement and improve the performance of several parts of the filter controller, can also be investigated for the proposed circuit as well as the other blocks of the filter system.

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# Appendix A

## PSPICE Analysis Circuit Diagrams

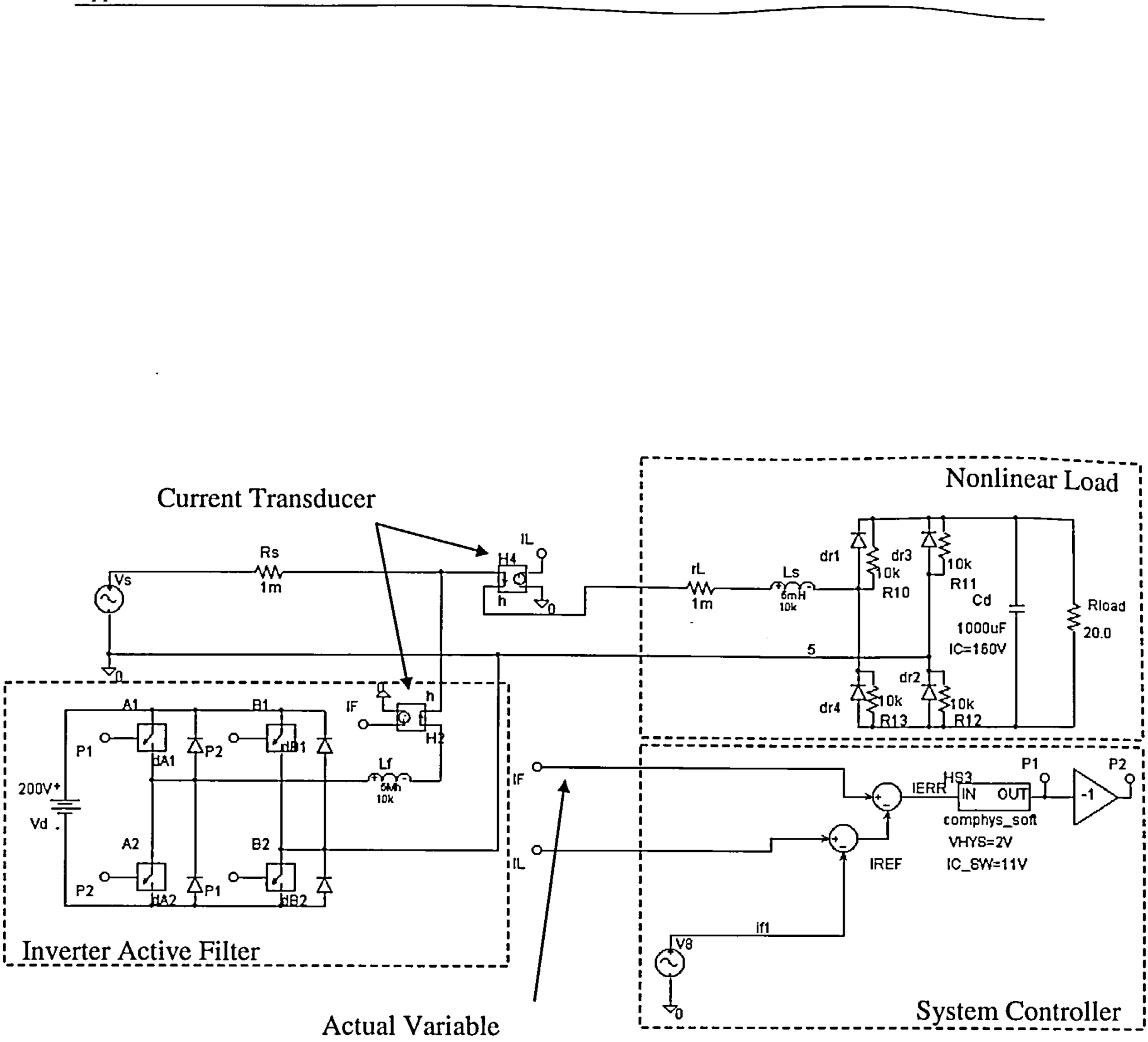


Fig.A.1 : PSPICE representation of inverter filters with a secondary dc supply

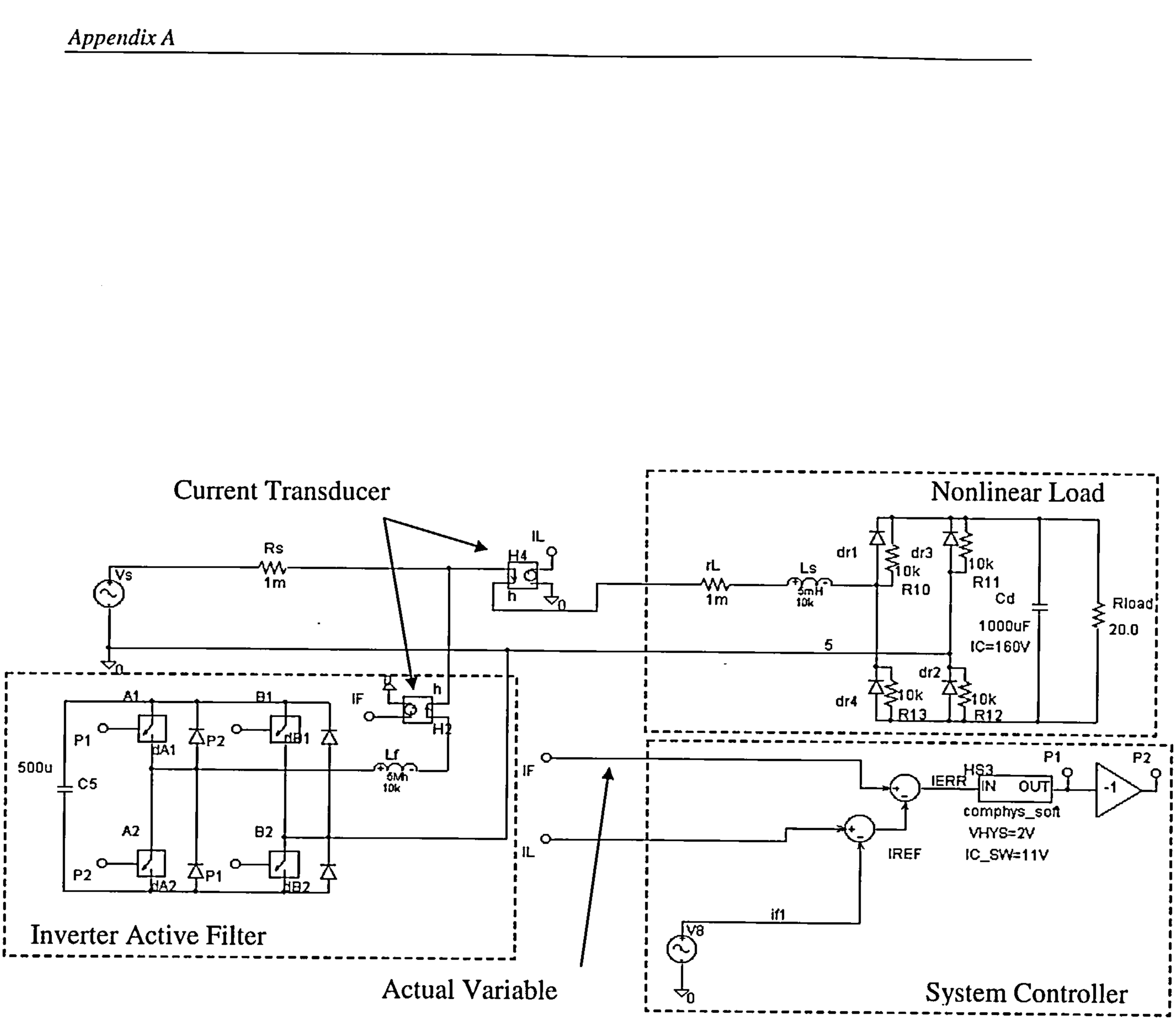


Fig.A.2 : PSPICE representation of inverter filters with a secondary capacitor

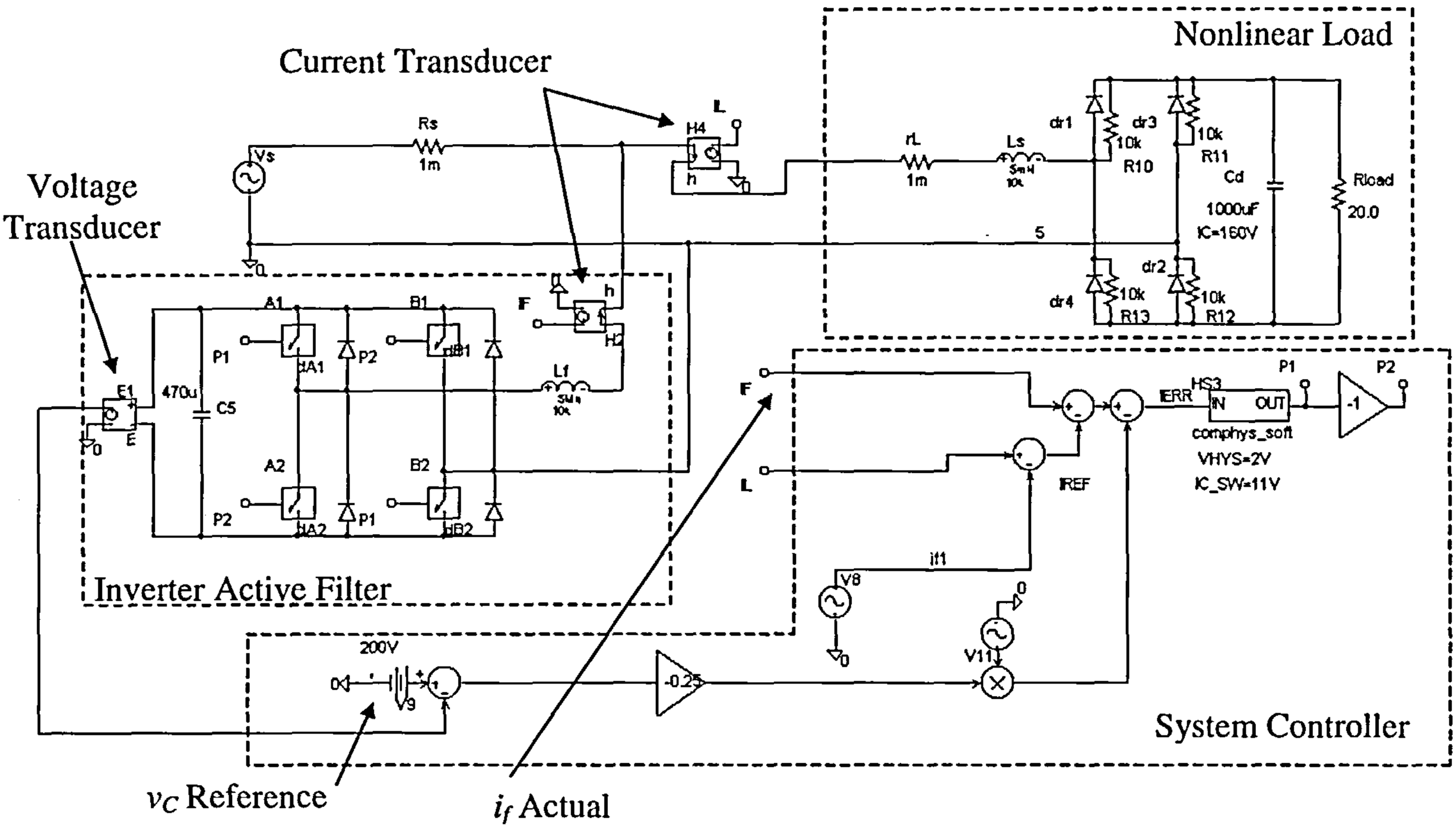


Fig.A.3 : PSPICE representation of inverter filters with a secondary capacitor and a capacitor voltage control loop

# Appendix B

# Assembly Language Program for Reference Synthesis

# Assembly Language Program for Reference Synthesis

```
        DOSSEG
        .MODEL      SMALL
        .Stack      1000h
        .486
        .Code
        JMP    @@ProgramStart
Alpha               EQU    1
Alpha1              EQU    250
Alpha2              EQU    250-Alpha
DC_out              EQU    100h
N_samples           EQU    512
Power_factor        EQU    0FFh
Mid_Range           EQU    0800h
NEG_SHIFT           EQU    0h
POS_SHIFT           EQU    0h
N_points            DW     N_samples
last_state          DW     00
angle               DW     0
XXX                 DW     0
C_12_bit            DW     2047
F_t_i               DW     0
F_XXX               DW     0
Ldih_by_dt          DW     0
A1_new              DD     0.0
B1_new              DD     0.0
F1_new              DD     0.0
Constant            DD     0.004
C_2pi               DD     (6.28318)
F_h_i               DD     0.0
F_sampling          DD     25000.0
F_h_i_old           DD     0.0
L_f                 DD     0.001
F_t                 DW     1024   DUP(0)
F_h                 DD     1024   DUP(0.)
SinArray            DD     1024   DUP(0.)
CosArray            DD     1024   DUP(0.)
temp_Sin_Array      DD     1024   DUP(0.)
temp_Cos_Array      DD     1024   DUP(0.)
@@ProgramStart:
        XOR    ECX,ECX
        FINIT
@@loop1:
        MOV    angle,CX
        FILD   angle
        FLD    C_2pi
        FMUL
        FILD   N_points
        FDIV
        FSINCOS
        FSTP   CosArray[ECX*4]
        FSTP   SinArray[ECX*4]
        INC    ECX
        CMP    ECX,N_samples
        JNZ    @@loop1
        CALL   Set_up_A2D_pacer
        MOV    AX,8
```

```
        MOV    BX,10
        CALL   Set_Timer_Pacer
        MOV    last_state,+1
@@Wait_for_start:
        CALL   Check_for_synch
        CMP    AL,+1
        JNE    @@Wait_for_start
@@Loop_all:
        XOR    ECX,ECX
@@calculate:
        FLD    B1_new
        FSUB   Temp_Cos_Array[ECX*4]
        FSTP   B1_new
        FLD    A1_new
        FSUB   Temp_Sin_Array[ECX*4]
        FSTP   A1_new
        CALL   Wait_for_EOC
        MOV    F_t_i,AX
        SUB    F_t_i,Mid_Range
        FLD    CosArray[ECX*4]
        FMUL   Constant
        FIMUL  F_t_i
        FST    Temp_Cos_Array[ECX*4]
        FADD   B1_new
        FSTP   B1_new
        FLD    SinArray[ECX*4]
        FMUL   Constant
        FIMUL  F_t_i
        FST    Temp_Sin_Array[ECX*4]
        FADD   A1_new
        FSTP   A1_new
        FLD    SinArray[ECX*4]
        FMUL   A1_new
        MOV    AL,Power_factor
        CMP    AL,0FFh
        JZ     @@pf_only
        FLD    CosArray[ECX*4]
        FMUL   B1_new
        FADD
@@pf_only:
        FST    F1_new
        FIST   F_XXX
        MOV    EAX,F_h_i
        MOV    F_h_i_old,EAX
        FISUB  F_t_i
        FST    F_h_i
        MOV    EAX,F_h_i
        MOV    F_h[ECX*4],EAX
        FISTP  F_XXX
        MOV    AX,F_XXX
        BT     AX,15
        JC     @@NEG
        ADD    AX,POS_SHIFT
        JMP    @@NEXT
@@NEG:
        SUB    AX,NEG_SHIFT
@@NEXT:
        CALL   out_D2A_1
        FLD    F_h_i
        FSUB   F_h_i_old
        FMUL   F_sampling
```

```
        FMUL    L_f
        FISTP   Ldih_by_dt
        MOV     AX,Ldih_by_dt
        CALL    out_D2A_2
        CALL    Digital_Out
        INC     ECX
        CALL    Check_for_synch
        CMP     AL,00
        JG      @@NoMore
        CMP     ECX,N_samples
        JG      @@NoMore
        JMP     @@calculate
@@NoMore:
        JMP     @@loop_all
end_prog:
        MOV     AH,4Ch
        INT     21h

INCLUDE         hbrk_008.asm

END
```

# Appendix C

# Load/Supply Parameters and Characteristics for the Harmonic Current Calculation Technique

# Load/Supply parameters and characteristics for the harmonic current calculation technique

## Supply characteristics

The supply parameters are given by the open and short circuit test at reduced voltage as follows

$V_{oc} = 6.25$ Volts

$I_{sc} = 6.647$ Amp

$W_{sc} = 25.73$ Watts

Hence, we can calculate the following parameters

$R_{source} = 0.58\ \Omega$

$Z_{source} = 0.94\ \Omega$

$X_{source} = 0.545\ \Omega$

$L_{source} = 1.735$ mH

## Load characteristics:

For the six different cases outlined in chapter 4 the following different loading conditions apply to each case respectively.

### 1. Pure resistive load (Sinusoidal current waveforms)

$I_{rms} = 1.8801$ Amp

$I_{pk} = 2.5$ Amp

THD = 6.6 %

| | Fund | 3rd | 5th | 7th | 9th | 11th | 13th | 15th | 17th | 19th |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_h$ | 1.87 | 5.6% | 3.3% | 0.82% | 0.4% | 0.29% | 0.07% | 0.07% | 0.08% | 0.01% |
| $\Theta_h$ | -5.9° | -66.7° | -124° | -83.3° | -222° | -217° | -99° | -19.5° | -18.4° | 0° |

## 2. Thyristor bridge with a resistive load

$I_{rms}$ = 1.434 Amp

$I_{pk}$ = 2.5 Amp

THD = 50.8 %

| | Fund | 3rd | 5th | 7th | 9th | 11th | 13th | 15th | 17th | 19th |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_h$ | 1.275 | 41.9% | 17% | 12.6% | 8.9% | 8.75% | 6.26% | 5.95% | 4.9% | 4.63% |
| $\Theta_h$ | -34° | -262° | -75.6° | -238° | -45.7° | -222° | -28° | -202° | -9.3° | -184° |

## 3. Thyristor bridge with a resistive/inductive load at minimum triggering angle

$I_{rms}$ = 1.66 Amp

$I_{pk}$ = 2.18 Amp

THD = 44.73 %

| | Fund | 3rd | 5th | 7th | 9th | 11th | 13th | 15th | 17th | 19th |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_h$ | 1.52 | 35.5% | 19.5% | 11% | 7.8% | 6.77% | 5.6% | 4.43% | 3.64% | 3.1% |
| $\Theta_h$ | -18.3° | -25.3° | -29° | -36.7° | -51.9° | -65° | -73° | -85° | -97.7° | -113° |

## 4. Thyristor bridge with a resistive/inductive load at a higher triggering angle

$I_{rms}$ = 1.203 Amp

$I_{pk}$ = 1.745 Amp

THD = 26 %

| | Fund | 3rd | 5th | 7th | 9th | 11th | 13th | 15th | 17th | 19th |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_h$ | 1.17 | 21.7% | 6.45% | 6.23% | 4.95% | 4.18% | 3.77% | 3.2% | 2.8% | 2.34% |
| $\Theta_h$ | -58.5° | -106° | -273° | -346° | -111° | -197° | -308° | -42° | -149° | -247° |

## 5. Thyristor bridge with a resistive/capacitive load at minimum triggering angle

$I_{rms}$ = 3.4 Amp

$I_{pk}$ = 6 Amp

THD = 48.42 %

| | Fund | 3rd | 5th | 7th | 9th | 11th | 13th | 15th | 17th | 19th |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_h$ | 2.88 | 47.1% | 5.8% | 8.4% | 1.36% | 2.65% | 1.4% | 0.79% | 1.15% | 0.11% |
| $\Theta_h$ | -4.6° | -180° | -311° | 44° | -76.8° | -234° | -256° | -70° | -86.5° | -212° |

## 6. Thyristor bridge with a resistive/capacitive load at a higher triggering angle

$I_{rms}$ = 2.5 Amp

$I_{pk}$ = 5.631 Amp

THD = 92.58 %

| | Fund | 3rd | 5th | 7th | 9th | 11th | 13th | 15th | 17th | 19th |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_h$ | 1.67 | 74.3% | 47.8% | 24.4% | 6% | 6.46% | 6.5% | 2.95% | 1.95% | 2.96% |
| $\Theta_h$ | -54.6° | -340° | -259° | -176° | -68.4° | -248° | -155° | -53.4° | -232° | -125° |

# Appendix D

## Assembly Language Program for PWM Generation

# Assembly Language Program for PWM Generation

```
        DOSSEG
        .MODEL      SMALL
        .Stack      2000h
        .486
        .Code
        JMP    @@ProgramStart
DIObase             EQU    1B0h
A2Dbase             EQU    230h
EOI_code            EQU    20h
PIC1_1              EQU    020h
PIC1_2              EQU    0A0h
Speaker             EQU    061h
Timer               EQU    040h
Int1                EQU    0Ah
Tim1                EQU    00h
Tim2                EQU    05h
pw1                 EQU    00h
pw2                 EQU    01h
T_delay             EQU    0Fh
T_delay1            EQU    0Fh
frequency           EQU    0FFh
off                 EQU    00h
D_pos               EQU    01h
D_neg               EQU    02h
S_pos               EQU    05h
S_neg               EQU    0Ah
Ready_bit           EQU    15
Np_max              DW     0460h
Old_Int1_off        DW 1   DUP(0)
Old_Int1_seg        DW 1   DUP(0)
Mid_Range           DW     800h
Max_range           DW     7FFh
Min_range           DW     010h
New_A2D             DB     0h
A2D_data_0          DW     0h
A2D_data_1          DW     0h
Dig_in              DW     0h
V_cap               DW     0h
V_s_Shift           DW     20h
V_c_Shift           DW     0h
Error_Gain          DW     3
A2D_Gain            DW     1
@@ProgramStart:
      MOV AL,80h
      MOV DX,DIObase+3
      OUT DX,AL
      MOV AL,9Bh
      MOV DX,DIObase+7
      OUT DX,AL
      MOV AL,off
      MOV DX,DIObase+0
      OUT DX,AL
      MOV AL,00h
      MOV DX,A2Dbase+9
      OUT DX,AL
      MOV AL,01h
```

```
        MOV DX,A2Dbase+11
        OUT DX,AL
        MOV AX,Mid_range
        MOV A2D_data_0,AX
        MOV A2D_data_1,AX
        MOV New_A2D,00h
        MOV AL,36h
        MOV DX,DIObase+11
        OUT DX,AL
        MOV DX,DIObase+8
        MOV AL,Tim1
        OUT DX,AL
        MOV AL,Tim2
        OUT DX,AL
        MOV AH,35h
        MOV AL,Int1
        INT 21h
        MOV Old_Int1_off,BX
        MOV Old_Int1_seg,ES
        MOV AH,25h
        MOV AL,Int1
        LEA DX,PROG_Int1
        PUSH CS
        POP DS
        INT 21h
        MOV AL,off
        MOV DX,DIObase+1
        OUT DX,AL
main_loop:
        CMP New_A2D,00h
        JNE main_loop
        MOV AL,02h
        MOV DX,DIObase+1
        OUT DX,AL
        MOV AL,00h
        MOV DX,A2Dbase+10
        OUT DX,AL
        MOV DX,A2Dbase+12
        MOV AL,00h
        OUT DX,AL
@@get_A2D_data_0:
        MOV DX,A2Dbase+5
        IN AL,DX
        MOV AH,AL
        BT AX,12
        JC @@get_A2D_data_0
        AND AH,0Fh
        DEC DX
        IN AL,DX
        ADD AX,V_c_Shift
        SUB AX,Mid_range
        MOV A2D_data_0,AX
        MOV AL,00h
        MOV DX,DIObase+1
        OUT DX,AL
        MOV AL,04h
        MOV DX,DIObase+1
        OUT DX,AL
        MOV AL,01h
        MOV DX,A2Dbase+10
        OUT DX,AL
```

```
        MOV DX,A2Dbase+12
        MOV AL,00h
        OUT DX,AL
@@get_A2D_data_1:
        MOV DX,A2Dbase+5
        IN AL,DX
        MOV AH,AL
        BT AX,12
        JC @@get_A2D_data_1
        AND AH,0Fh
        DEC DX
        IN AL,DX
        ADD AX,V_s_Shift
        SUB AX,Mid_range
        MOV A2D_data_1,AX
        MOV AL,00h
        MOV DX,DIObase+1
        OUT DX,AL
        MOV New_A2D,0FFh
        JMP main_loop
        PUSH DS
        MOV AH,25h
        MOV AL,Int1
        MOV DX,Old_Int1_off
        MOV DS,Old_Int1_seg
        INT 21h
        POP DS
        MOV   AH,4Ch
        INT   21h
PROG_Int1   PROC
        JMP @@start
@@start:
        PUSHA
        MOV AL,01h
        MOV DX,DIObase+1
        OUT DX,AL
        MOV New_A2D,00h
@@continue:
        MOV DX,DIObase+5
@@Data_Rdy:
        IN AL,DX
        MOV AH,AL
        BT AX,Ready_bit
        JC @@Data_Rdy
        BT AX,12
        JC @@one
        BTR AX,8
        JMP @@rest
@@one:
        BTS AX,8
@@rest:
        AND AH,0Fh
        MOV DX,DIObase+4
        IN AL,DX
        SUB AX,Mid_range
        MOV Dig_in,AX
        MOV AX,A2D_data_1
        MOV BX,Dig_in
        SUB AX,BX
        PUSH AX
        ADD AX,Mid_range
```

```
        MOV DX,A2Dbase+6
        OUT DX,AL
        MOV AL,AH
        INC DX
        OUT DX,AL
        POP AX
        MOV V_cap,AX
        MOV BX,A2D_data_0
        SUB AX,BX
        CMP AX,00h
        JS Negative_Number
Positive_Number:
        MUL Error_Gain
        CMP DX,00h
        JZ P_No_overflow
P_overflow:
        MOV AX,0FFFFh
P_No_overflow:
        MOV BX,AX
        CMP AX,Max_range
        JG P_over_range
        CMP AX,Min_range
        JL P_under_range
        MOV DX,DIObase+0
        MOV AL,S_pos
        OUT DX,AL
        JMP pw1_pw2
P_over_range:
        MOV DX,DIObase+0
        MOV AL,S_pos
        OUT DX,AL
        JMP pw1_pw2
P_under_range:
        MOV DX,DIObase+0
        MOV AL,D_pos
        OUT DX,AL
        JMP pw1_pw2
Negative_Number:
        NEG AX
        MUL Error_Gain
        CMP DX,00h
        JZ N_No_overflow
N_overflow:
        MOV AX,0FFFFh
N_No_overflow:
        MOV BX,AX
        CMP AX,Max_range
        JG N_over_range
        CMP AX,Min_range
        JL N_under_range
        MOV DX,DIObase+0
        MOV AL,S_neg
        OUT DX,AL
        JMP pw1_pw2
N_over_range:
        MOV DX,DIObase+0
        MOV AL,S_neg
        OUT DX,AL
        JMP pw1_pw2
N_under_range:
        MOV DX,DIObase+0
```

```
        MOV AL,D_neg
        OUT DX,AL
        JMP pw1_pw2
pw1_pw2:
        MOVZX EAX,BX
        PUSH AX
        ADD AX,Mid_range
        MOV DX,A2Dbase+4
        OUT DX,AL
        MOV AL,AH
        INC DX
        OUT DX,AL
        POP AX
        MOVZX EBX,Np_max
        MUL EBX
        MOVZX EBX,Max_range
        DIV EBX
        INC AX
        CMP AX,Np_max
        JB @@Continue1
        MOV AX,Np_max
@@Continue1:
        MOV BX,AX
        MOV AL,70h
        MOV DX,DIObase+11
        OUT DX,AL
        MOV DX,DIObase+9
        MOV AL,BL
        OUT DX,AL
        MOV AL,BH
        OUT DX,AL;
        MOV AL,00h
        MOV DX,DIObase+1
        OUT DX,AL
        MOV AL,EOI_code
        MOV DX,PIC1_2
        OUT DX,AL
        MOV DX,PIC1_1
        OUT DX,AL
        POPA
        IRET
PROG_Int1    ENDP
END
```

# Appendix E

# List of Publications

# List of Publications

1. El-Habrouk M., Darwish M. K., Mehta P., "How to choose the appropriate active power filter for a specific application – Part I: Power circuits and configurations", MEPCON'97, January 1997, Alexandria, Egypt.

2. El-Habrouk M., Darwish M. K., Mehta P., "How to choose the appropriate active filter for a specific application – Part II: Compensated Variables, Control and Reference estimation", MEPCON'97, January 1997, Alexandria, Egypt.

3. El-Habrouk M., Darwish M. K., Mehta P., "A new configuration for shunt active filter", EPE'97, September 1997, Trondheim, Norway.

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***Notes:***

- The fourth paper won the best presented-paper award in the UPEC'97.
- The author was awarded the "1998 Young Power Engineer Award" for the fifth paper.