Long and Short Term Effects of X-Rays on Charge Coupled Devices

A thesis submitted for the degree of Doctor of Philosophy

by

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This thesis is dedicated to my parents, Joan and Ian Tudge

Abstract

EEV buried channel charge coupled devices (BCCDs) with technological variations have been studied with respect to their response to 70kVp X-rays. Process variations considered are the conventional BCCD, scintillator coated BCCDs ((Gadox(Eu) and CsI(Tl)) and the inversion mode device. The work was made necessary by the use of these CCDs for dental X-ray imaging.

Effects investigated include changes in device operating voltages and dark current. The dark current buildup has been characterised in terms of a prompt component seen immediately following irradiation, and a time dependent component which occurs gradually. A major part of this work was the determination of the location and concentration of the energy states responsible for this dark current buildup. Also a novel aspect of the work was the derivation of an expression describing the time dependent component as a function of time and temperature.

Effects associated with the bias dependence of the BCCD have also been considered, with particular regard to the effect of a negative substrate bias, and the theoretical explanation has been developed.

The findings of this work have demonstrated the suitability of these devices for the commercial application of imaging x-rays for dentistry.

Contents

Abbreviations and Acronyms

BCCD	Buried Channel Charge Coupled Device
CCD	Charge Coupled Device
CTE	Charge Transfer Efficiency
FET	Field Effect Transistor
Gadox	Gd_2O_2S
MIS	Metal Insulator Silicon
MNOS	Metal Nitride Oxide Silicon
MOS	Metal Oxide Silicon
PKA	Primary Knock-on Atom
SCCD	Surface Channel Charge Coupled Device
V_{rd}	Voltage applied to CCD Reset Drain
V_{SS}	Voltage applied to CCD Substrate

Device Notation

The devices used in this investigation are shown with both the identification numbers used by EEV, and the identification numbers used in this report.

Identification used in this report	Identification code used by EEV	Type of Device
CCD02-1	A1036/37	Conventional CCD02
CCD02-2	A1036/15	Conventional CCD02
CCD02-3	A0783-32	Conventional CCD02
CCD02-4	A0700-31	Conventional CCD02
CCD02-5	A0816/58	Conventional CCD02
CCD02IM-1	A2220-10-1	Inversion Mode CCD02
CCD02IM-2	A2381-4	Inversion Mode CCD02
CCD05-1	A2178-14-6	Conventional CCD05
CCD05-2	A2120-12-9	Conventional CCD05
CCD05-3	A1099-11-8	Conventional CCD05
CCD05-4	A2179-15-10	Conventional CCD05
CCD05-5	A3094-16-5	Conventional CCD05
CCD05-6	A3094-16-8	Conventional CCD05
CCD05-7	A2178-14-4	Conventional CCD05
CCD05-8	A3067-10-10	Conventional CCD05
CCD05GC-1	A3098-5-4	Gadox(Eu) coated CCD05
CCD05GC-2	A3098-5-5	Gadox(Eu) coated CCD05
CCD05CsI	A2705-17-17	CsI(Tl) coated CCD05

Terms and Units Relating to Dose and Exposure

The gray (Gy)	This is the SI unit of dose and corresponds to an energy deposition of 1 joule per kilogram of absorber.
The krad	The unit of dose employed in this report, is equal to 10Gy
The roentgen	The unit of exposure required to generate 2.58×10^{-4} ions per kg in air.
(Electronic) equilibrium	An absorber, or region of an absorber, is said to be in electronic equilibrium if the energy lost by transport of energetic electrons out of the absorber is equal to the energy gained by the transport of energetic electrons into the absorber.
kerma	This relates to energy deposited by a photon beam directly into an absorber, in the form of energetic electrons. No account is taken of electron transport into or out of the material. If the absorber is in electronic equilibrium then the kerma is equivalent to the dose.
Flux	The number of particles passing through a defined zone per unit time ($cm^{-2}s^{-1}$).
Fluence	The time integrated flux (cm^{-2})
Erg	A traditional unit of energy, equivalent to 10^{-7} joules.
Dose Equivalent	The biological damage caused by irradiation is not only depndent upon dose deposited, but also upon the type of radiation absorbed. Each type of radiation is assigned a quality factor ,Q, which represents the relative danger it poses to living tissue and bone etc. The dose equivalent of any given radiation exposure is then equal to the product of the dose, and the quality factor. e.g. betas and gammas have a quality factor of unity, whereas the more damaging alphas have a quality factor of approx 20.
sievert (Sv)	This is the SI unit of dose equivalent = Q x Dose(Gy)
rem	This is the tradiational unit of dose equivalent = Q x Dose(rad)

Acknowledgements

I would like to thank my supervisor at Brunel, Dr Steve Watts, along with Prof Andrew Holmes-Siedle, for their help and guidance throughout this work. Also, for their help and co-operation during the time of our collaboration, my thanks go to Dr Brian Allen, Tim Eaton, Ian Airs, and Peter Poole from EEV.

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Introduction

1.1. Operation of CCDs

1.1.1. Introduction to the CCD

In principle, the CCD is a 2-dimensional array of MIS capacitors. These are formed by coating a semiconductor substrate with a continuous layer of dielectric then defining an array of electrodes over the dielectric. Charge, which is the signal, can be generated by energetic particles or photons interacting in the semiconductor. The capacitors are able to store charge generated locally, so recording the spatial distribution of the charge generation, and thus defining pixels in the image. In order that the charge in each pixel can be isolated from the charge in neighbouring pixels it necessary for each pixel to comprise at least two capacitors (2-phase), although more typically it would comprise three capacitors (3-phase). By appropriate pulse clocking of the electrodes, it is then possible to "read out" the latent image from the device whilst retaining the signal information in each pixel.

1.1.2 The MOS Capacitor as a Potential Well

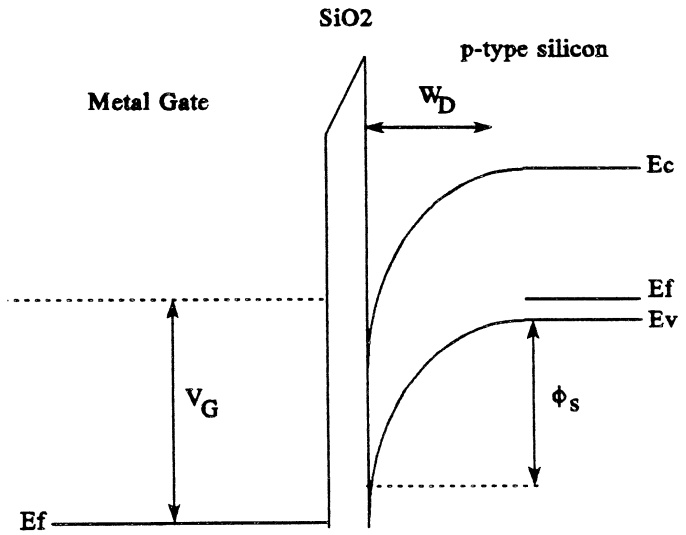


Fig 1.1.a. The MOS capacitor in deep depletion.

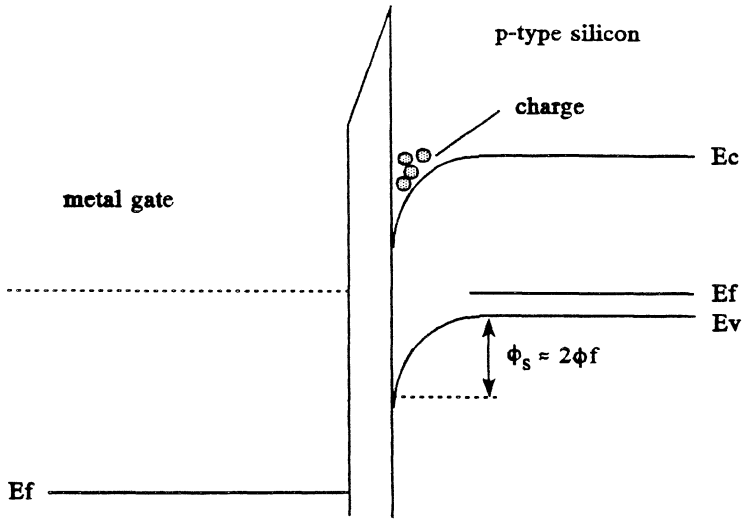


Fig 1.1.b. The MOS capacitor in thermal equilibrium.

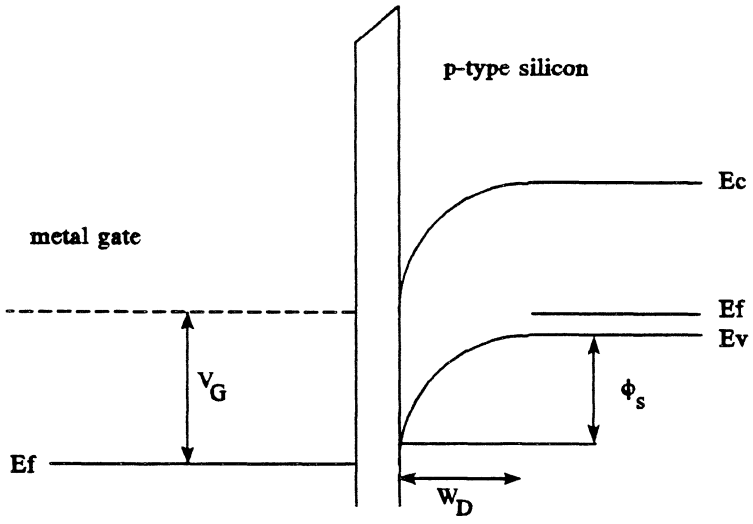


Fig 1.1.c The MOS capacitor in deep depletion, as fig 1.1.a., but with a smaller gate voltage.

Fig 1.1 The potential profile through an MOS capacitor, and its dependence upon applied gate bias. Fig 1.1.a shows the capacitor in deep depletion immediately after application of a gate votage, fig 1.1.b shows the charge layer after the device has reached equilibrium and fig 1.1.c shows the deep depletion condition for a smaller applied gate bias. W_D is the depletion depth, ϕ_S is the surface potential, and V_G is the gate bias.

As shown in Fig 1.1., the MOS capacitor provides a simple potential well structure. Electrons generated thermally within the depletion region, along with electrons arriving via other mechanisms will be prevented from escaping into the bulk silicon by the potential gradient. Comparison between Fig 1.1.a, and Fig 1.1.c illustrates the way in which the potential profile through the structure may be modulated by control of the gate bias. It can be seen that the potential well under the gate held at high potential, is deeper than than that under the gate held at lower potential.

The actual depth of the potential well ϕ_s, and the width of the depletion region, W_D are determined by solution of Poissons equation [1] and are given by;

$$\phi_s = V_G + V_0 + \frac{Q_{INV}}{C_{OX}} - \sqrt{2(V_G + \frac{Q_{INV}}{C_{OX}})V_0 + V_0^2}$$

where $V_0 = qN_A\xi_0\xi_{si}/C_{OX}^2$, Q_{INV} is the charge density per unit area in the inversion layer (Ccm^{-2}), N_A is the acceptor concentration (cm^{-3}), C_{OX} is the oxide capacitance per unit area (Fcm^{-2}), and V_G is the voltage applied to the gate (volts).

and;

$$W_D = \sqrt{\frac{2\xi_0\xi_{Si}\phi_s}{qN_A}}$$

where ξ_0 is the dielectric permittivity of free space ($C^2N^{-1}cm^{-2}$), and ξ_{Si} is the dielectric constant for silicon.

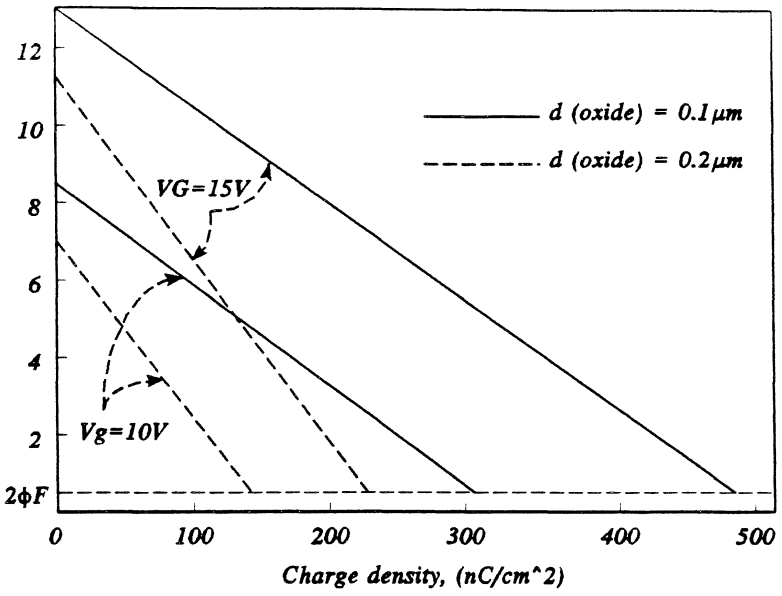


Fig 1.2. The reduction in potential well depth as a function of inversion charge density. This shows the relationship between surface potential, and inversion layer charge, for two different thicknesses of oxide on a p-type substrate of dopant density 1 x 10^{15} cm^{-3} [1 fig 1.4]

The relationship between ϕ_s and Q_{INV} determines the charge capacity of the potential well. Fig 1.2 shows how the well depth reduces with increasing inversion layer charge for two different thicknesses of oxide on a p-type substrate of dopant density 1 x 10^{15} cm^{-3} [1 fig 1.4]. The potential well capacity is effectively the charge density at which the surface potential reaches its equilibrium level of about $2\phi_F$,.

1.1.3. The Basic Structure of the Surface Channel CCD (SCCD)

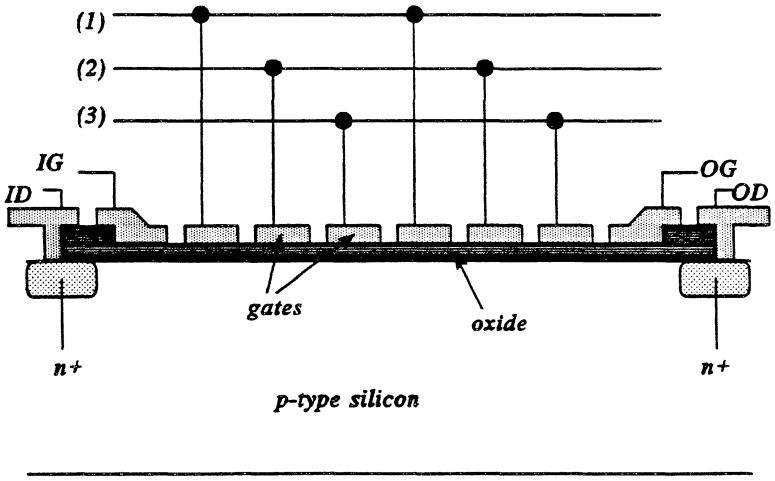


Fig 1.3 The layer structure of the surface channel CCD

The surface channel CCD as shown in fig 1.3 is the simplest of the two basic types of CCD, and is based upon the MOS capacitor described in section 1.1.2. The potential profile in the silicon ensures that any charge collected is confined to the locality of the Si/SiO_2 interface. During operation of the device the capacitors are biased so as to be in deep depletion (Fig 1.1a) therefore generation of electron-hole pairs exceeds recombination. The holes so generated pass down the potential gradient into the substrate, whilst the electrons are confined in the potential well, adjacent to the oxide. If the device was held in open circuit mode these electrons would accumulate until equilibrium was reached, (fig 1.1b) so taking the capacitor out of deep depletion. However in the case of an operational device the charge is constantly clocked out from the device so preventing equilibrium from being reached. As a result of this a constant generation of charge is seen in the absence of signal.. This generation of charge is referred to as the dark current, and provides a background from which signal charge has to be distinguished. The magnitude of this dark current will be dependent upon many factors, but will rise exponentially with temperature.

The most serious limitation of the SCCD is that the charge is stored and transferred adjacent to the oxide surface, and so is able to undergo interaction with traps and defects found here. This causes a reduction in the charge transfer efficiency, (CTE) which is the fraction of signal charge remaining after transferral from one electrode to the next. As the signal has to undergo many hundreds of

transfers during the clocking of a CCD, it is imperative that this CTE is very high (>0.99999) if the signal information is not to be lost.

1.1.4. The Basic Structure of the Buried Channel CCD (BCCD)

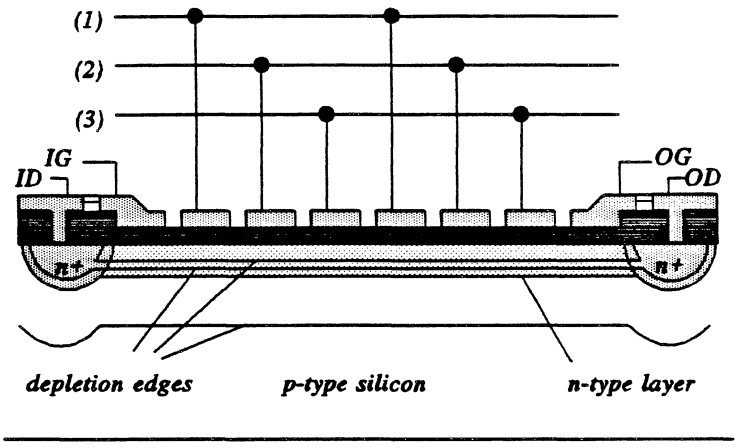


Fig 1.4 The layer structure of a BCCD, before pinch-off.

The idea that CTE could be improved by transfering signal charge in a channel remote from the oxide interface was first suggested by Boyle and Smith [2]. BCCD devices typically have the structure shown in fig 1.4. A shallow n-type layer is implanted on top of the p-type substrate as shown. If the voltage applied at the drain is sufficiently high then the depletion layer resulting from the Si/SiO_2 surface meets the depletion layer resulting from the p-n junction. When this "punch-through" condition is satisfied the n-type layer is fully depleted.

With the device in this condition the potential profile under the electrodes is no longer dependent upon the bias applied at the drain, and can be controlled by the electrode bias. A typical potential profile through the device for two applied gate biases is shown in Fig 1.5 The potential minimum for electrons now lies in the n-layer, and is well away from the oxide interface.

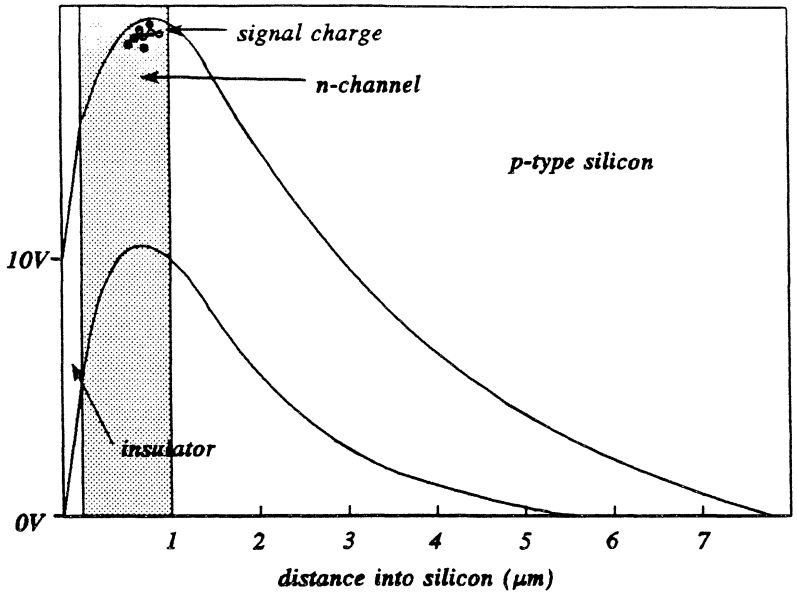


Fig 1.5. The potential profile through a BCCD, assuming the same parameters as fig 1.6.

The signal charge is no longer able to interact with the states at the Si/SiO_2, so the potential CTE is much greater.

The BCCD has significantly improved charge transfer efficiency compared with the SCCD. However the disadvantage of using the buried channel structure is the loss of potential well capacity incurred. Fig 1.6 shows the way in which the channel potential of a structure such as that of the CCD02 device decreases as charge is collected in the channel. For the limiting case where the gate voltage is low, the channel potential approaches the substrate potential for a channel charge density of about 65 $nCcm^{-2}$. This is significantly lower than the charge concentration required to fill the potential well of a typical SCCD, (see fig 1.2) and corresponds to approximately 4.5×10^5 electrons per pixel.

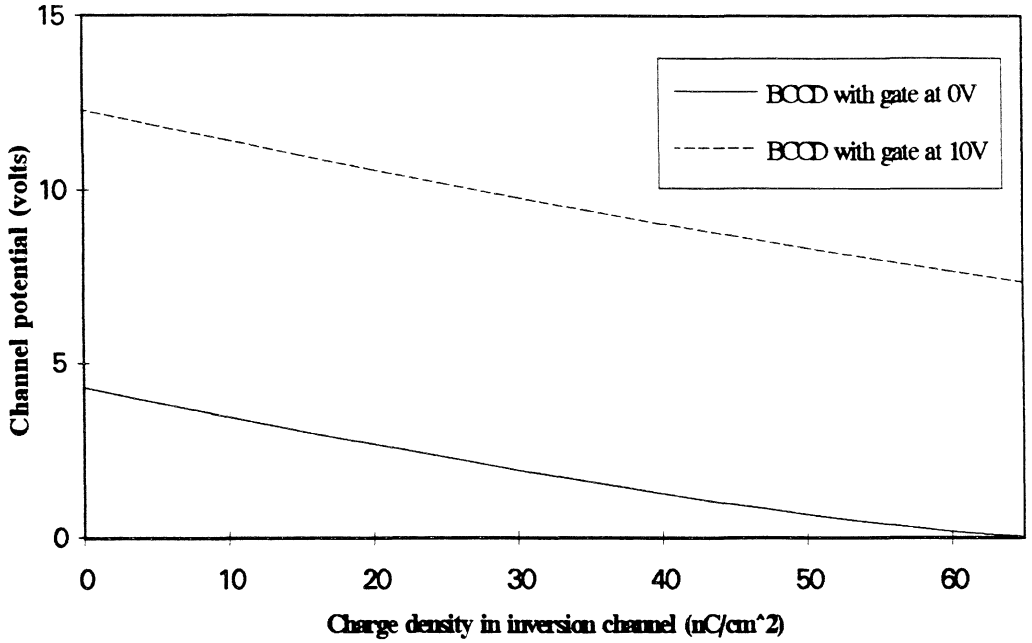


Fig 1.6. This plot shows the reduction in channel potential caused by charge accumulation in the potential well of the CCD02 structure, and was obtained numerically for the abrupt junction approximation [1 p28]. Vss was taken to be 6V, whilst the channel potential refers to the potential with respect to Vss. The n-channel donor density was taken as 1×10^{16} cm^{-3}, with the acceptor concentration of the p-type epitaxial layer taken as 5×10^{14} cm^{-3}.

1.1.5. The CCD Pixel Array

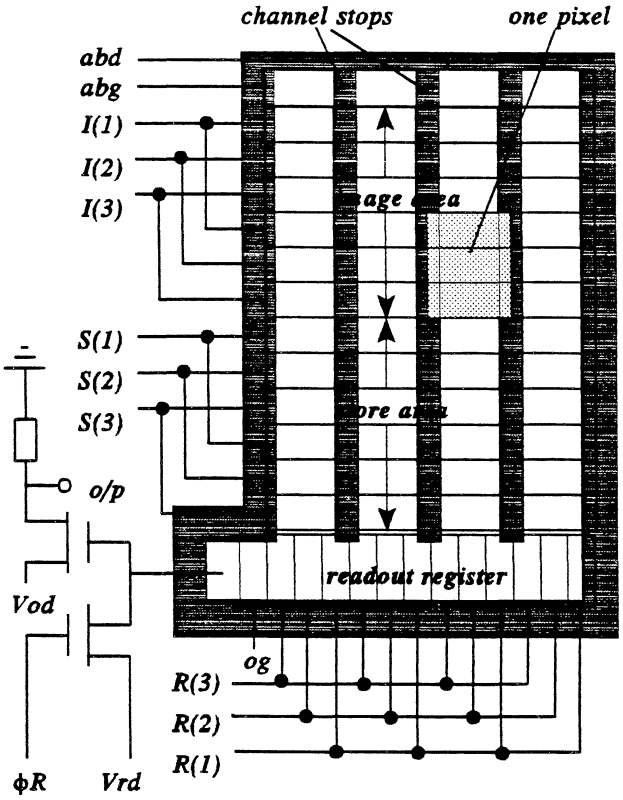


Fig 1.7 A typical CCD pixel array (with features as for EEV's CCD02 device). Charge is clocked along the columns, and then scanned out of the output register one row at a time. Vrd is the reset drain bias, Vod is the output drain bias, φR is the reset transistor gate pulse, abd is the antiblooming drain connection and abg is the antiblooming gate (see section 1.2).

In order for the signal information to be retained, it is necessary for the signal charge to be confined to the appropriate pixel, until charge transfer to the next pixel is desired. As described previously the potential profile through the device prevents charge from escaping into the substrate. P-type channel stops running parallel with the n-channel (Fig 1.9) prevent charge from spreading laterally into neighbouring columns. These stops ensure that the charge is able to migrate only along the direction of the n-channel. This movement of charge is controlled by modulation of the gate biases. The use of gate bias modulation to confine charge in a three phase CCD pixel is shown in fig 1.8. Therefore we have a 2-dimensional CCD array in which charge is localised where it is generated To access this information we now need to manipulate the gate biases to enable the pixel data to be read sequentially from the device.

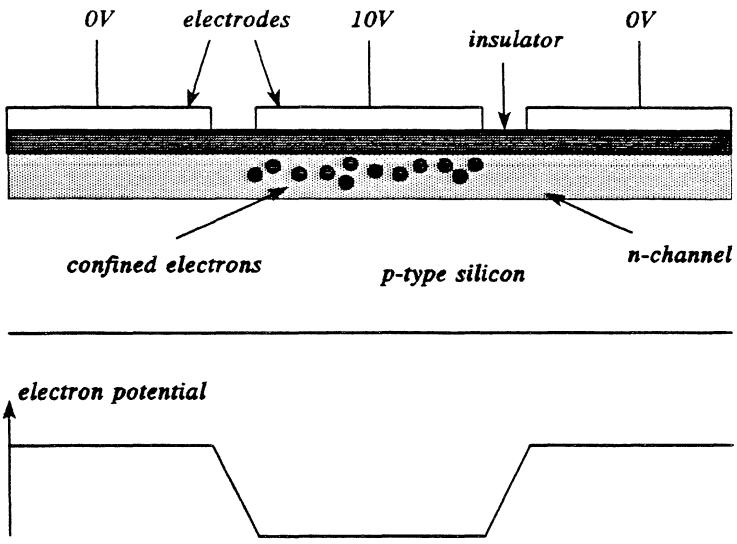


Fig 1.8. The use of gate bias modulation to confine charge.

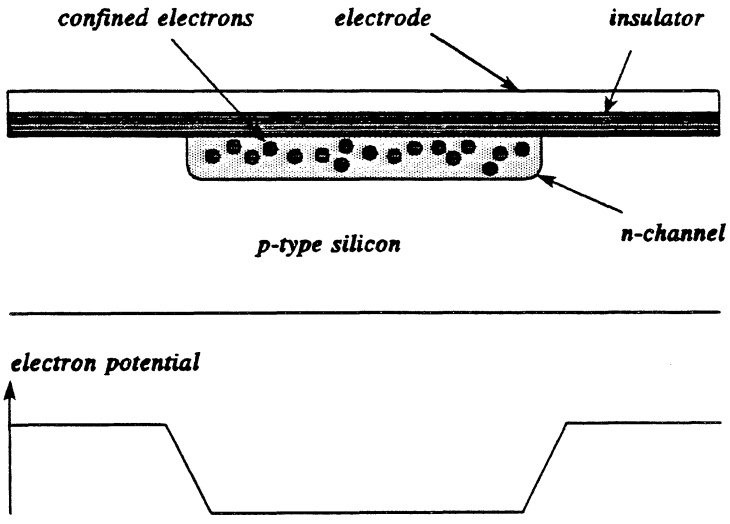


Fig 1.9 The use of p-type channel stops for an n-channel BCCD

1.1.6. Image Formation and Charge Transfer within the CCD

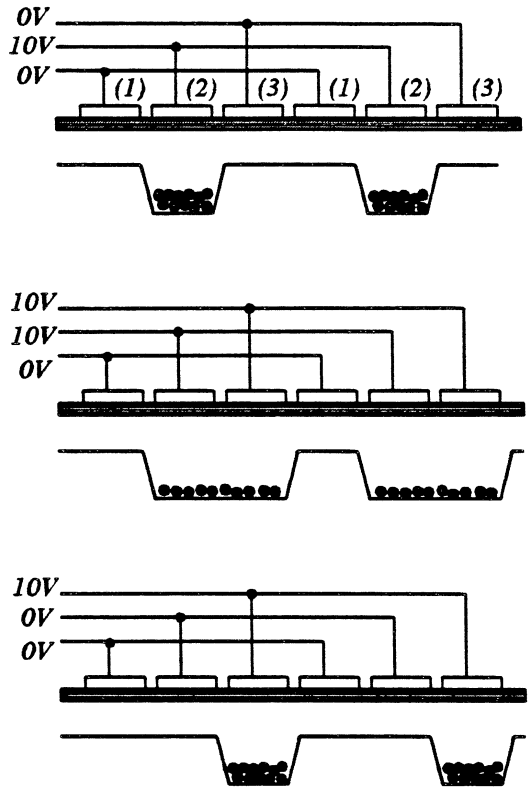


Fig 1.10 charge transfer in a three phase CCD, such as the CCD02 and CCD05.

Charge transfer for a three-phase CCD is shown in fig 1.10. During imaging the charge in each pixel is confined under IΦ2 electrode. For the case shown in fig 1.7 the device array is made up of two regions each with separate electrode connections. The image area is the region of the device which is exposed to the signal and where the image is formed. The store area is the region of the device where the image is stored pending transfer to the output circuitry. For video applications this area is shielded with an opaque layer. After a finite integration period, which for television applications would be around 20ms, the charge transfer process will begin. The IΦ3 electrode is switched to high potential then the IΦ2 electrode is switched to low potential, such that any charge held under IΦ2 passes to the IΦ3. The charge is then transferred from the IΦ3 electrode to the IΦ1 , and then again to the next IΦ2 electrode by the same means. Thus after one cycle, the charge

packets have all been shifted by one whole pixel. This process is then repeated once for every pixel row in the image area, so that the image is located in the store region of the device.

Once the signal charge from one image as reached the store region of the device it is then ready to be dumped row by row into the output register. Each row will be clocked sequentially out from the output register to the sampling electronics. As this is carried out a new image will be generated in the image region of the device.

1.1.7. Output Circuitry

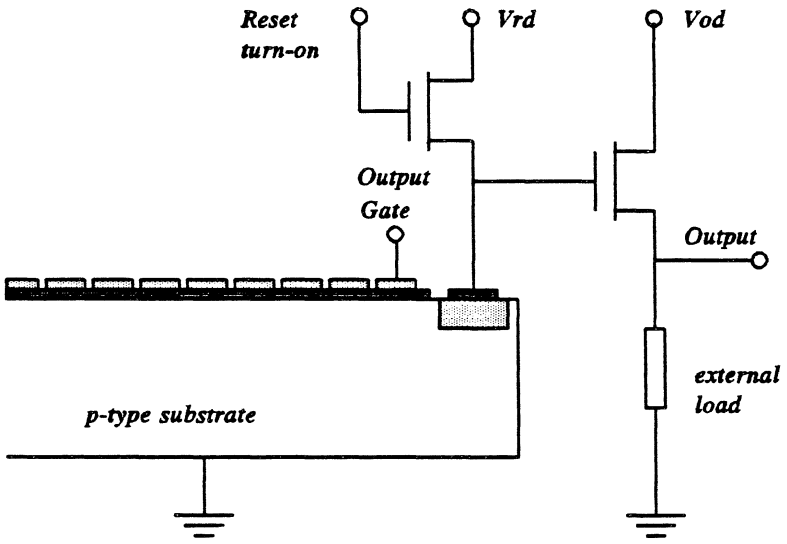


Fig 1.11 A typical CCD "floating diffusion" output circuit

Fig 1.11 shows a typical CCD output circuit, known as the floating diffusion circuit. Charge from the output register is dumped onto the output node as shown. This causes a change in voltage of the node, which is dependent upon the quantity of charge and the capacitance of reverse biased output diode plus any other stray capacitances on the output circuit. After each charge packet is sampled, the output node is reset to the reset drain voltage, by pulsing of the reset FET gate. The output node is then ready to receive the next charge packet. The output gate shown helps to keep the output node electrically remote from the RΦ3 electrode and so minimises feedthrough of the RΦ3 pulse. Sometimes a dummy circuit identical to the one shown is fabricated, but not connected to the output

diode. In this way the output from the dummy circuit will represent the feedthrough pulses but not the signal, enabling the outputs from the two circuits to be compared and the feedthrough to be effectively eliminated.

1.2. The EEV CCD02 and CCD05

These two EEV device structures were studied extensively in this work. Although EEV produce technology variations of both structures, including inversion mode operation, and scintillator coated devices, (described in 1.2.3.) the basic layout of each structure remains the same.

1.2.1. The EEV CCD02 Device

This device can be equipped either with a low noise, slow scan output circuit for low temperature scientific work, or with a high speed output circuit for television applications. The image region consists of 288 rows by 385 columns, whilst the store region has 290 rows by 385 columns. Each gate is approximately 7μm by 22μm, giving a pixel area of 22μm by 22μm. The total active area of the device is 8.5mm by 12.7mm.

The devices were provided without shielding over the store area as this gave greater flexibility for experimental purposes. The CCD02 is designed with an antiblooming drain, the purpose of which is to allow a path of low resistance out of the device for excess charge in any individual column. If this were not the case the charge would eventually flood across the p-stop barriers and into neighbouring columns causing a "blooming" in the image.

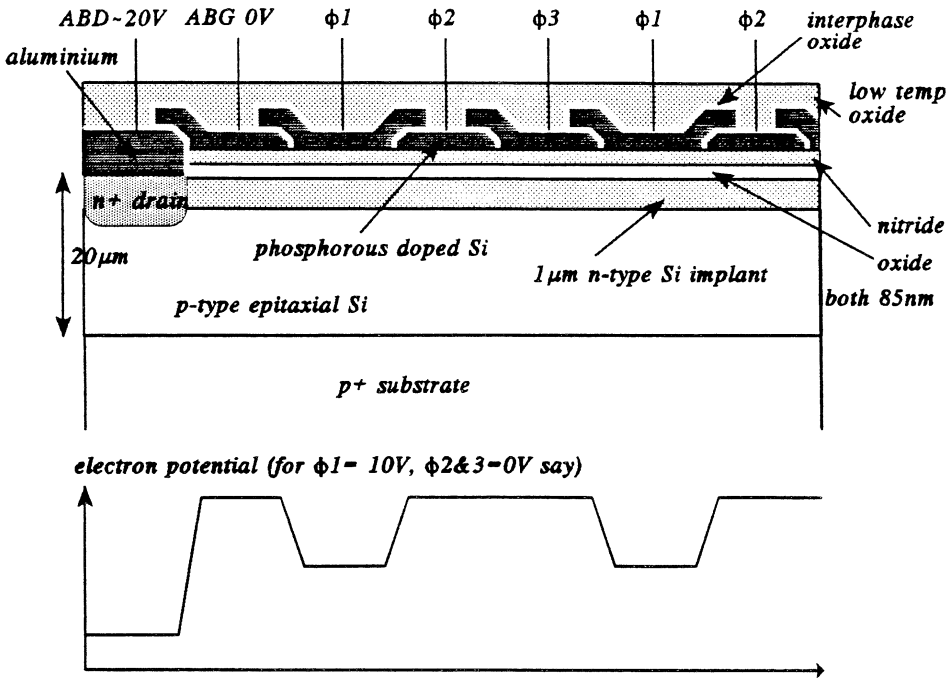


Fig 1.12. A schematic cross-section of the CCD02 BCCD. ABD is the anti-blooming drain, and ABG the anti blooming gate.

A cross section through the device is shown in fig 1.12. The substrate is a Czochralski grown p-type silicon with a doping concentration of around 5 x 10^{18} cm^{-3}. A 20μm epitaxial layer is then grown onto the substrate with a doping concentration of around 5 x 10^{14} cm^{-3}. The buried channels are created by masking the surface to define the p-stop strips, and then implanting phosphorous to a concentration of 1 x 10^{16} cm^{-3}.

The gate insulator is a double layer of SiO_2 and Si_3N_4. This double layer is chosen because it combines the virtues of both layers whilst minimising the weaknesses. The SiO_2 matches well to silicon so enabling a low interface trap density to be achieved , but it is a poor passivating layer being porous to water vapour and metallic ions. SiO_2 is also vulnerable to radiation, being susceptible to buildup of trapped charges. The Si_3N_4 does not match well with silicon and so a direct interaface between the two is likely to yield a high density of defects. In addition to this it is found that tunneling and trapping of charge carriers around the interface causes the band condition of the structure to be indeterminate for any applied voltage [4]. However the Si_3N_4 gives a very good

passivation layer, and is relatively invulnerable to radiation (see section 2.2.2). Both layers are easily prepared by single processing steps so the double layer is an ideal compromise. The flat-band condition for the MNOS system is shown in fig 1.13 [5].

The gates are fabricated from semi-transparent poly crystalline silicon. This is necessary in order that light of optical wavelengths can be imaged. The polysilicon is doped with phosphorous to reduce resistivity. Overlapping gate technology is employed, as this is found to enable optimum charge transfer.

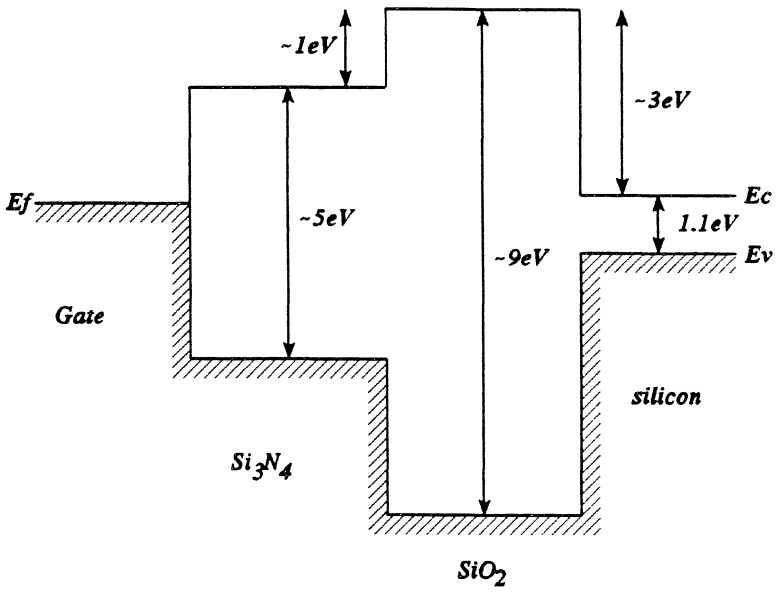


Fig 1.13 Energy band structure of MNOS system in flat-band condition (see also [6+7]).

1.2.2. The EEV CCD05 Device

The CCD05 device is a large area version of the CCD02. It has 770 columns by 576 rows in both the image area and in the store area. The active area is 17.3mm by 25.9mm. In addition to its extra size the CCD05 device has output registers at both ends of the chip. Each output register in turn has two output circuits, a high speed output circuit at one end and a slow scan output at the other end. Reversal of the $\Phi 1$ and $\Phi 2$ phases allows the charge to be clocked in either direction both within the active area of the device and within each output register. These options allow the user to choose the appropriate output at the time of use, and also provide some redundancy in the event of damage to one of the output circuits. Unlike the CCD02 therefore, one chip is suitable for either scientific,

or video use.

1.3. Technological Variants of the CCD02 and CCD05

1.3.1. The Inversion Mode Device

As described in 1.1.3. an operational device shows a background "dark" current in the absence of signal. This dark current can limit the performance of the device as described in section 1.4.1. The inversion mode device has been designed in order to suppress dark current generation from Si/SiO_2, surfaces, which are a souce of much of the dark current in CCDs, both irradiated and unirradiated. These devices are therefore capable of withstanding much larger radiation doses before the dark current levels prevent normal operation. This is particularly useful in hostile regimes, such as space, where the devices may receive doses in excess of 1Mrad in a few years.

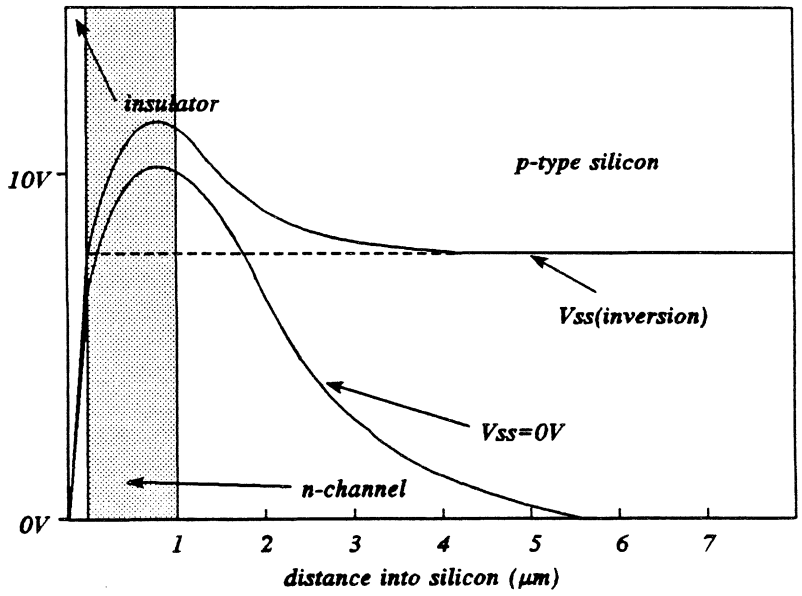


Fig 1.14. The potential through the device with V_G=Vss=0V, and with Vss equal to the potential at the silicon/oxide interface. If Vss is increased beyond the potential at the interface, then holes are injected from the p-stops into the n-channel. These holes then accumulate at the interface, so suppressing surface current generation.

The operation of the inversion mode is understood by referring to fig 1.14. It can be seen that if the substrate bias is increased to a critical point, then the potential in the substrate will equal the potential at the surface of the n-channel. Any further increase in the substrate bias causes the injection of holes into the n-channel at the oxide surface, so forming an inversion layer, which inhibits charge generation here.(see section 2.3.2.2.) As charge generation at the oxide interface is by far the greatest component of the dark current in these structures, this leads to a dramatic reduction in dark current, typically from nanoamps to picoamps.

This effect can be seen with conventional mode devices, but the full benefit cannot be realised because when the gate is pulsed to high voltage the n-channel surface is raised to a higher potential than the substrate, and so is depleted once more. As one of the gate phases has to be held at high potential permanently in order to maintain charge confinement, (Fig 1.8) the dark current is only inhibited in two thirds of the device. One solution to this problem is shown in fig 1.15

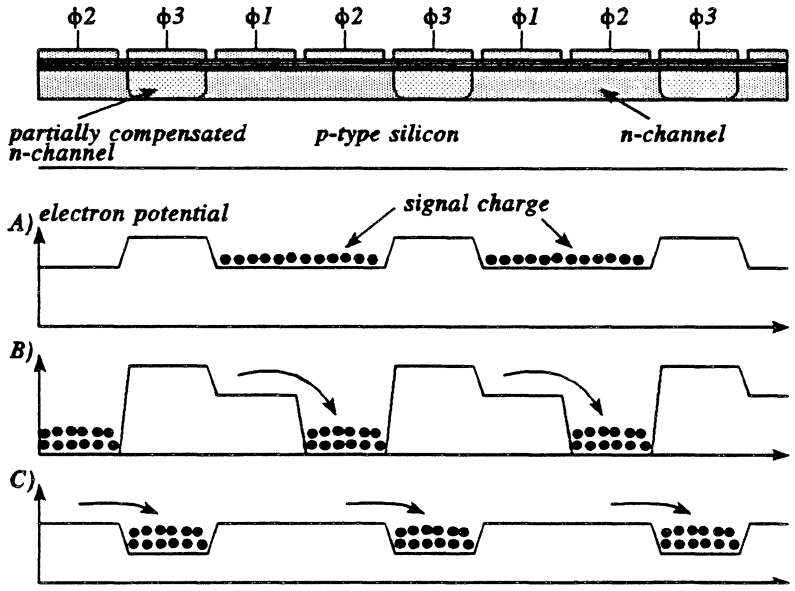


Fig 1.15 The modified structure of an inversion mode device, with the channel under one phase partially compensated by p-type dopant. The electron potential under each phase is shown for; A) all gates held at zero bias, B) ϕ2 biased at 10V with ϕ1 and ϕ3 at 0V, and C) ϕ3 biased at 10V with ϕ1 and ϕ2 at 0V.

The structure of the device is modified slightly by doping the channel under one of the phases with

acceptor atoms. In the structure shown the Φ3 phase has been selected for this dopant. The dopant concentration has to be chosen very carefully in order that the integrity of the potential well under phases Φ1 and Φ2 be maintained, whilst also allowing the potential well under Φ3 to be restored by pulsing of the gate during charge transfer. In this way the whole device is operating in inversion mode during the image integration time, and the n-channel surfaces are only re-depleted during charge transfer. Charge transfer is rapid and typically will account for less than 0.1% of the duty cycle. As would be expected the inversion mode device has a reduced potential well capacity, about half that of the conventional mode devices for EEV's CCD02.

1.3.2. Scintillator Coatings

The relatively thin epitaxial silicon layer (20μm) in the CCD is not an efficient collector of x-ray photons. Unlike visible light photons, most will pass through the layer without interacting, and so will not contribute to the signal (see fig 1.16). Positioning of a thicker, more dense (so able to stop more x-ray photons) scintillator layer, in front of the device therefore offers the prospect of an enhanced signal in the device, the signal being made up partly from scintillated light, and partly from secondary electrons. The obvious potential benefits to result from this are, reduced patient dose in devices used for medical imaging, and increased device longevity, as the devices are not damaged by scintillated light. In addition there is the possibility that the coatings could be used as intensifying screens to allow higher energy X-rays to be imaged. Possible drawbacks to this technology could include enhancement of dose seen by the vulnerable oxide layer, and loss of robustness in routine operation.

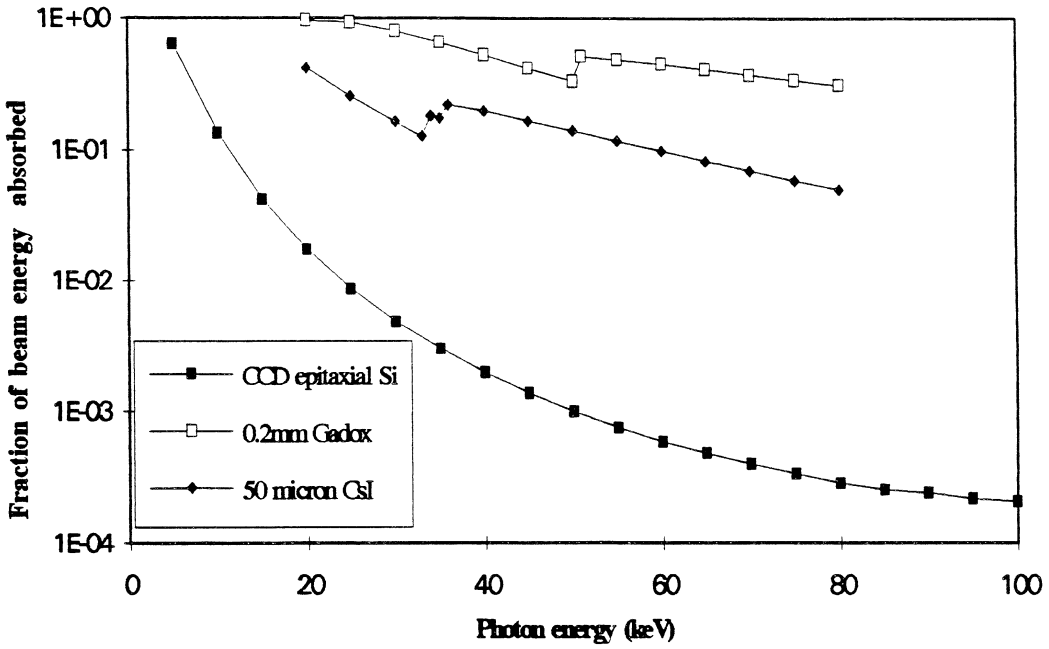


Fig 1.16. The fraction of beam energy absorbed by the 20μm CCD epitaxial layer, as a function of photon energy. Also shown is the corresponding data for the two scintillator layers considered in this work. These values were calculated using the PHOTCOEF package (see section 3.3.4. and [8]).

1.3.2.1.The Principle of Scintillation

Scintillators fall loosely into two categories, organic and inorganic. Whereas with organic scintillators the mechanism for scintillation is based upon transitions in the energy level structure of individual molecules, and is therefore independent of the physical state of the material, scintillation from inorganic materials is a function of the energy states in the crystal lattice, and is understood in terms of its band structure. This work is concerned only with the inorganic scintillators CsI(Tl), and $Gd_2O_2S(Eu)$ or Gadox.

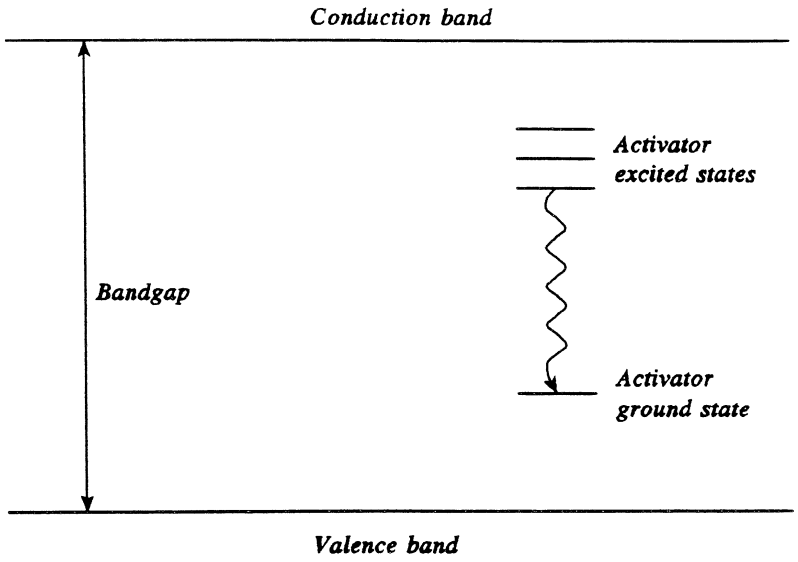


Fig 1.17 Energy band structure of activated scintillator [9, fig 8.6]

Fig 1.17 shows the band structure of a typical insulator. Absorption of radiation energy can cause an electron to be raised to the conduction band, from its original position in the valence band. On its return to the valence band, energy will be released in the form of a photon. In order that this photon should fall in the visible spectrum it is necessary that the energy released should be in the range 2-3eV. There are few pure crystals with bandgaps of this size, [10] and the use of such a semiconductor would cause considerable loss of signal due to self absorption, as the energy carried by an emitted photon would be similar to that required to excite an electron-hole pair. The preferred solution is to use insulating materials (having bandgaps in excess of 4eV) and dope them with activator impurities.The insulator materials can then be selected on the basis of their suitability in terms of other criteria such as transparency to emitted light, luminescence decay times, and ease of manfuacture into blocks of appropriate size and optical quality.

The purpose of the activator impurity is to introduce, into the scintillator material, possible energy transitions of the desired magnitude. When electron-hole pairs are formed by absorption of radiation energy there is a strong liklihood that the holes will be annhilated by ionisation of the activator states. With little chance of recombining with holes in the insulator, the electrons are then free to migrate through the material until they encounter one of the ionised activator states. When an electron drops into such a state, the result is a neutral state with its own set of energy states as shown in fig 1.17. If the electron combines with the activator in such a way as to form an excited

configuration with an allowed transition to the ground state, then de-excitation will follow with the probable emission of a photon. If an appropriate scintillator host and activator impurity are chosen then this photon will fall in the visible spectrum. In practice the scintillator will emit photons over a spectrum of energies, corresponding to all the allowed energy transitions within the absorber energy states. Also in addition to the process described above, it is possible for some of the electrons to interact with the activator states in such a way as to form an excited configuration from which transition to the ground state is not allowed directly. In this case additional energy is required to raise the state to a higher energy state from which transition to the ground state is possible. This extra energy is likely to be in the form of thermal energy. The photon which is subsequently emitted will represent a slow component of the scintillated light, this is referred to as phosphorescence.

1.3.2.2. The light output from a scintillator

The light output from a scintillator is a function of the dose absorbed and the efficiency with which this is converted to visible light. If a dose, D, is absorbed by the scintillator then the number of electron-hole pairs created, N, is given approximately by [9 p229 and 11];

$$N \approx 6.24 \times 10^{16} \times \frac{DM}{3E_{BG}} \qquad (1.1)$$

where E_{BG} is the bandgap (eV), M is the mass of the scintillator (g), and D is the dose (krad). The constant takes account of the use of the krad ($=1x10^{-2}$ Jg^{-1}) as the unit of dose.

In a good inorganic scintillator the efficiency of transfer from an electron-hole pair to scintillated photon is typically greater than 80%, [9] so the number of photons produced will approach that of electron-hole pairs. The light output of the scintillator is normally described in terms of photons produced per MeV of absorbed radiation energy.

The absolute efficiency of the scintillator is defined as the fraction of absorbed energy, subsequently emitted as light and is typically of the order of 0.1. A value of 0.12 is quoted for CsI(Tl) [9,12], which has a peak wavelength emission at 550nm, or 2.3eV. The absolute efficiency however does not take into account the "stopping power" of the material. For a given fluence of radiation, higher density material will absorb a greater dose, and may therefore, be able to emit more light even if the

absolute efficiency is lower.

An important parameter of the light output is the principal decay constant, τ, which is the half life of de-excitation of the excited states for the principal process of light production (see section 1.3.2.1). This imposes a limitation upon the temporal resolution of the scintillator, as in order that two pulses of radiation can be resolved, it is necessary that the time interval separating them, is greater than the decay constant of the scintillated light. For CsI(Tl) the principal decay constant is approximately $1x10^{-6}$s [9,13].

1.3.2.3. CCD Signal Contribution from the Scintillator layer.

Adding a layer of scintillator to the CCD, can significantly change the responsivity of the device to radiation. This is partly due to the scintillated light passed from the scintillator to the CCD epitaxial layer, and partly due to the change in dose deposition profile caused by the scintillator. In order that the net signal enhancment can be predicted, it is necessary to use PHOTCOEF (see section 3.4 [8]) simulations to determine the dose deposition profile through the device, and then to estimate the scintillated light contribution from the scintillator dose.

As mentioned in 1.3.2.1, the two scintillators used to coat EEV CCDs for this work are CsI(Tl) at a thickness of 50μm, and Gd_2O_2S(Eu), at a thickness of 200μm. PHOTCOEF predicted the dose depositions shown in fig 1.18, for different device structures exposed to a fluence of 70kVp x-rays, f, sufficient to deposit a dose of unity in the epitaxial layer of an uncoated device.

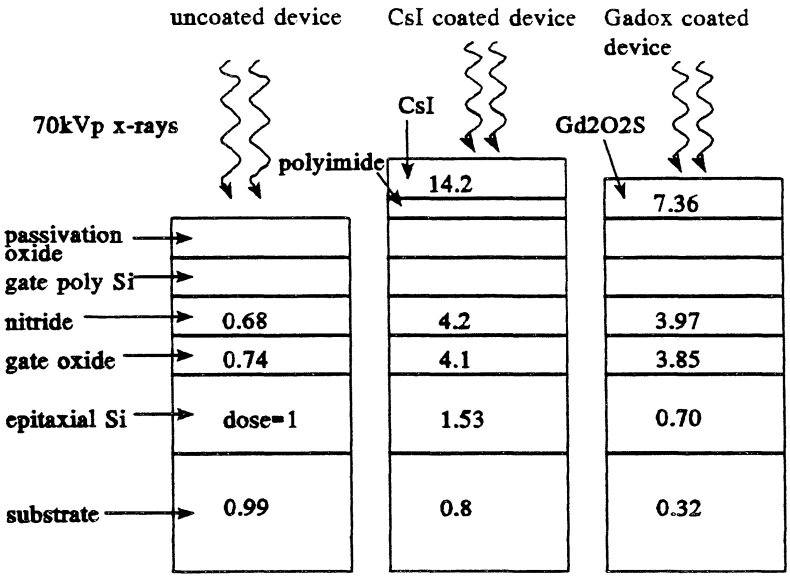


Fig 1.18 Relative dose deposition values for uncoated, and scintillator coated devices.

For the uncoated device, the signal size is determined by the dose deposited in the epitaxial silicon. In terms of the number of signal electrons per cm^2 of device area, this is given by;

$$N_{uncoated}=1.74\times10^{16}\times D_{Si}t_{Si}\rho_{Si} \qquad (1.2)$$

where D_{Si} is the dose in krad, t_{Si} is the thickness of the epitaxial silicon layer in cm, and ρ_{Si} is the density of silicon in gcm^{-3}. The constant takes account of the electron-hole yield in silicon, of $(3.6eV)^{-1}$, and the use of the krad ($=1x10^{-2}\ Jg^{-1}$) as unit of dose.

In the case of the scintillator coated devices it is necessary to first calculate the number of scintillation light photons which will be produced by the radiation, and then estimate the number of electron-hole pairs which will be created in the silicon by this light. From equation 1.1, it can be seen that the number of scintillation photons emitted by the scintillator per cm^2, is given by;

$$N_{ph}=6.24\times10^{10}\times Dt_{sci}\rho_{sci}y_{ph}$$

where t_{sci} is the scintillator thickness in cm, ρ_{sci} is the density of the scintillator in gcm^{-3}, and y_{ph} is

the photon yield of the scintillator in MeV^{-1}. The constant is included to allow dose in krad. to be used with photon yield in MeV^{-1}, as these are the preferred units of use.

The number of signal electrons subsequently generated in the CCD then approximates to;

$$N_e(sci) \approx 6.24 \times 10^{10} \times D_{sci} t_{sci} \rho_{sci} y_{ph} y_Q F_{CCD}$$

where y_Q is the representative quantum efficiency of the CCD across the scintillator emission spectrum. F_{CCD} is the fraction of scintillated light escaping from the scintillator in the direction of the CCD, and is a function of the refractive indices of the scintillator and the CCD surface oxide.

The total signal in the scintillator coated device is the sum of the the direct radiation component and the scintillated light component, and is therefore given by;

$$N_{tot} \approx 1.74 \times 10^{16} \times D_{si}(sci) t_{Si} \rho_{Si} + 6.24 \times 10^{10} \times D_{sci} t_{sci} \rho_{sci} y_{ph} y_Q F_{CCD} \qquad (1.3)$$

where D_{Si}(sci) is the dose seen in the silicon epitaxial layer of a scintillator coated device.

The signal enhancement caused by the scintillator coating is then determined by dividing equation 1.3 for the signal in a scintillator coated device, by equation 1.2 for the signal in a conventional device. This requires an estimation of the quantum efficiency, y_Q, of the CCD in detecting the scintillated light.

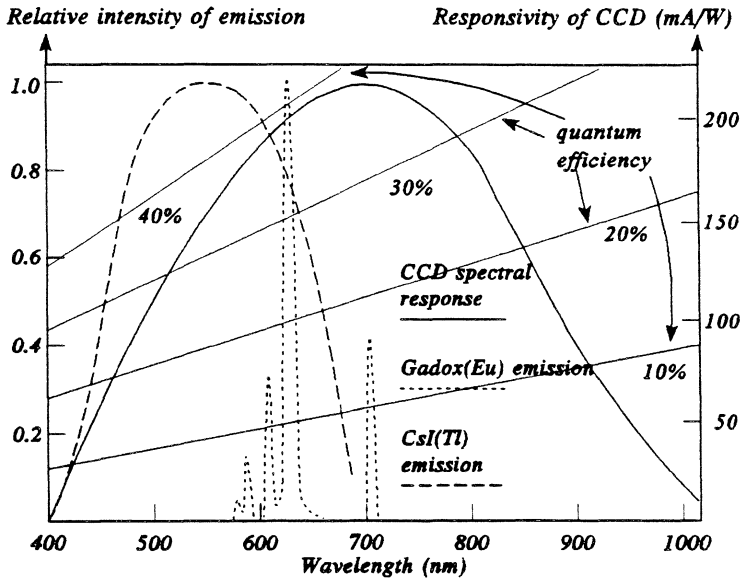


Fig 1.19. This shows the emission spectra of the two scintillators along with the specral responsivity of the CCD to visible light.

Fig 1.19 shows the spectral responsivity of the CCD, compared with the normalised emission spectrum of the scintillators. At the wavelength of peak emission from the CsI(Tl) scintillator (~550nm), the quantum efficiency of detection of the CCD is between 30% and 40%, although towards the short wavelength tail of the CsI(Tl) emission spectrum, it falls below that level. For the emission spectrum of $Gd_2O_2S(Eu)$ the quantum efficiency of the CCD is slightly higher, approaching 40% at the wavelength of peak emission of around 620nm.

Thus for the CsI(Tl) coated device, taking 0.3 as being representative of y_Q across the CsI(Tl) emission spectrum, y_{ph} for CsI(Tl) as 52000 MeV^{-1} (estimate, see [9,12,13 and 14,]), the density of CsI as 4.54 gcm^{-3}, the density of silicon as 2.32 gcm^{-3}, and using the dose deposition values in fig 1.18 to substitute D_{Si} for D_{sci} and $D_{Si}(sci)$, then the total signal size is given by;

$$N_{tot} \approx 1.24\times10^{14}\times D_{Si}\ [direct\ component] + 3.16\times10^{14}\times D_{Si}F_{CCD}\ [scintillator\ comp]$$

compared with the signal in the uncoated device given by equation 1.2, which reduces to

$$N_{uncoated} = 8.1\times10^{13}\times D_{Si}$$

As the refractive index of the CCD polyimide (~ 1.8) is significantly greater than that of air, F_{CCD} will be somewhere between 0.5 and 1.This suggests a signal enhancement in the range 3.5 - 5.5. Quoted estimates of y_{ph} for CsI(Tl) vary between 45000 MeV^{-1} [13] and 56000 MeV^{-1}[12] with Knoll [9] settling for an intermediate figure of 52000 MeV^{-1}. This uncertainty combined with inevitable inaccuracies in the dose deposition profiling, due to uncertainty of absorption cross-sections and approximations used to determine electron transport between layers, (see chapter 3) means that this enhancement factor only serves as a loose approximation. More specific work has been carried out by Hylton [15], which indicates that approximately 19000 photons are detected by CCDs of this type for every MeV absorbed by the CsI(Tl) layer. This value, $y_{ph(CCD)}$, is the product of the photon yield, y_{ph}, the fraction of scintillated light escaping the scintillator in the direction of the CCD, F_{CCD}, and the representative quantum efficiency of the CCD across the scintillator emission spectrum, y_Q.

The Gadox is of higher density than the CsI, at 7.5 gcm^{-3}, and this, combined with the greater thickness of the layer enables it to stop many more of the x-ray photons (as shown in fig 1.16). Although Blasse [16] discusses the properties of sister scintillators Gadox(Pr) and Gadox(Ce), quoting a light output 75% of that from the CsI(Tl)(approx 40,000MeV^{-1}), and a decay constant of 3μs, there is little information available as regards Gadox(Eu). Hylton suggested that the number of scintillated photons detected by a CCD coated with 200μm of Gadox(Eu), $y_{ph(CCD)}$, is around 6000 MeV^{-1}. Taking this value for $y_{ph(CCD)}$, the density of Gadox as 7.48 gcm^{-3}, the density of silicon as 2.32 gcm^{-3}, and using the dose deposition values in fig 1.18 to substitute D_{Si} for D_{sci} and $D_{Si}(sci)$, then the total expected signal size for the Gadox(Eu) coated device is given by;

$$N_{tot} \approx 5.65\times10^{13}\times D_{Si}\ [direct\ component] + 4.1\times10^{14}\times D_{Si}\ [scintillator\ comp]$$

Dividing this expression by equation 1.2, for the uncoated device, indicates a signal enhancement factor, due to the Gadox(Eu) layer, of between 5 and 6.

1.3.2.4. Radiation Damage to Scintillators

Coating a CCD with a scintillator has obvious implications for the radiation hardness of the device, as the dose seen in the oxide layer is a function of the scintillator (as shown in fig 1.18, and

described more fully in chapter 3). However it is expected that any extra device degradation caused by the scintillator will be more than offset by the signal enhancement. What is of greater concern is the possibility that the scintillator itself could degrade following irradiation. Previous work with Co^{60} gammas [17] has shown that the transmission spectrum of CsI(Tl) in the visible spectrum, deteriorates after only a few krad. This was seen for blocks of a few cubic cm in size however, and whilst the physics of the degradation may apply to thin films of scintillator, it is unlikely for the loss of transmission to prove a problem. The light output of Csi(Tl) was also seen to degrade after irradiation although measurements were only made after a dose of 2Mrad. Reductions in light output of between 14% and 48% are quoted for different manufacturer's samples. At smaller doses [13], a 34% reduction in light output has been observed after 0.5krad, although it is stressed that this figure is exaggerated by the spectral mismatch between the CsI(Tl) emission and the photomultiplier tube used to measure the output. Long lived phosphorescence, or afterglow, itself has been found to vary greatly from sample to sample, sometimes lasting for many minutes after high dose rate irradiations. Grassman et al [13] suggest that good crystals should have an afterglow which is less than 5% of the total light yield.

1.4. X-ray Imaging with the CCD.

CCDs have a variety of applications, including digital signal processing in which the devices can be used to construct high density shift registers and serial memories [18]. The devices considered here though, are detector devices which can be used as detectors of particles for high energy physics, or as a record of images received by the device in the form of visible light, or x-rays, in much the same way as photographic film. This work is concerned with the use of these devices as x-ray imagers in dentistry

CCDs have been used for medical imaging in recent years, specifically in dentistry. Here the CCD is used as an alternative to radiographic film. The device, whilst in communication with its driving electronics via a flexible connector lead, is positioned inside the mouth as the film would be. For the sake of hygiene the device itself is covered by a protective rubber sleeve. The image stored by the device is normally displayed on a monitor, although the user has the option of a hard copy if desired. The obvious benefits to be gained from using the CCD rather than radiographic film, are that the CCD is reusable, and that the patient dose necessary to achieve a satisfactory image is about ten

times lower than that required for the film. (0.05rad (tissue), compared to (0.5rad) for radiographic film). Reduced dose also has the side benefit of allowing faster exposures, therefore minimising the effect of patient movement.

1.4.1. Dark Current in the CCD

The background signal or dark current is an important factor for consideration with these devices. The problem caused by dark current is related to the size of the dark current charge packet carried by each pixel. For devices used in high energy physics, for particle detection, is possible to cool the device to very low temperatures to suppress dark current levels (see section 2.3 for quantitative description of dark current), whilst for relatively high speed scanning applications, such as video cameras, the short integration times ($\leq$40ms) help to minimise the size of dark current charge packets. For dental imaging purposes however it is necessary that the device be operated in the mouth, and so be at blood temperature. Integration time is pre-determined by the consumer imaging equipment to be in the range 100-900ms, with a default of 500ms.

The typical dark current level in an unirradiated device operated with standard settings at 300K is around 1.5nAcm^{-2}. For an integration time of 500ms this corresponds to a dark current charge packet of around 22,000 electrons per pixel. Increasing the temperature of the device to 310K (blood temperature) increases this to around 50,000 electrons per pixel. This compares to the potential well capacity of around 500,000 electrons for the buried channel structure used in these devices (see section 1.1.4).

If the dark current level is increased as a result of device irradiation this will affect device performance in two ways. The signal carrying capacity of the pixels will be reduced by an amount corresponding to the increase in size of the dark current charge packet, and also the dark current noise will increase. In general there are two components of dark current noise to be considered, that arising from non-uniformity of dark current generation across the device, and that arising from the randomness of thermal generation of carriers [1]. Noise resulting from device non-uniformity may not be affected by irradiation if the dark current increase itself is uniform across the device. However, as far as the the random thermal generation of charge carriers is concerned, the noise is effectively the standard deviation of the dark current charge packet size. As the size of the thermally generated charge packets will follow a Poisson distribution, the standard deviation is equal to the

square root of the mean of these charge packets. Therefore the noise associated with the dark current increases as the square root of the dark current.

References for Chapter 1

[1] J.D. Beynon and D.R. Lamb, "Charge Coupled Devices and their Applications", Published by McGraw Hill, 1980.

[2] W.S. Boyle and G.E. Smith, "Charge Coupled Semiconductor Devices", B.S.T.J. 49, 587-593, 1970.

[3] M.S. Robbins, "Radiation damage Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1992.

[4] T. Roy, "Ionising Radiation Induced surface effects in Charge Coupled Devices", PhD Thesis. Dept of Physics , Brunel University, UK, 1993.

[5] N.S. Saks, "Response of MNOS Capacitors to Ionizing Radiation at 80K", IEEE Trans. Nucl. Sci., NS-25, 6 1226-1232, 1978.

[6] J. Robertson, "Electronic Structure of Silicon Nitride", Phil. Mag. B, 63 (1) 47-77 1991.

[7] S. Manzini, and F. Volante, "Charge Transport and Trapping in Silicon Nitride- Silicon Dioxide Dielectric Double Layers", J. Appl. Phys., 58 (11) 4300-4306, 1985.

[8] PHOTCOEF, AIC Software, PO Bx 544, Grafton, Mass 01519, USA.

[9] G. F. Knoll, "Radiation Detection and Measurement", Published by John Wiley & Sons, 1989.

[10] M. Goodge, "Semiconductor Device Technology", Published by Macmillan, 1985.

[11] R.B. Murray, "Energy Transfer in Alkali Halide Scintillators by Electron-Hole Diffusion and Capture", IEEE Trans. Nucl. Sci., NS-22, 54-57, 1975.

[12] E. Sakai, "Recent Measurements on Scintillator-Photodetector Systems", IEEE Trans. Nucl. Sci., NS-34 418-422, 1987.

[13] H. Grassman, E. Lorenz, and H. G. Moser, "Properties of CsI(Tl)- Renaissance of an old Scintillator Material", Nucl. Instr. and Meth., A228, 323-326, 1985.

[14] I. Holl, E. Lorenz, and G. Mageras, "A Measurement of the Light Yield of Common Inorganic Scintillators", IEEE. Trans. Nucl. sci., Vol 35, 1, 105-109, 1988.

[15] J.D.Hylton, "Performance and Suitability of CCD Imaging Systems for Industrial Radiography", MSc Thesis, Dept of Physics, Brunel University, 1994.

[16] G. Blasse, and B.C. Grabmaier, "Luminescent Materials", Published by Springer-Verlag, 1994.

[17] C.L. Woody, J. A. Kierstead, P.W. Levy, and S. Stoll, "Radiation Damage in Undoped CsI and Csi(Tl)", IEEE. Trans. Nucl. Sci., Vol 39, 4, 524-531, 1992.

[18] J. Millman, and A. Grabel, "Microelectronics", Published by McGraw-Hill, 1987.

CCDs and Radiation

2.1 Radiation Effects in CCDs

Semiconductor devices are vulnerable to radiation damage by several mechanisms, the relative significance of each being dependent upon the nature of the radiation and the structure of the device. There are three regions of the CCD which are susceptible to long term radiation induced effects. These are the gate dielectric, the silicon epitaxial layer, and the interface between the two. In the case of scintillator coated devices there is also the possibility that the performance of the scintillator will be degraded.

2.1.1 Irradiation by Charged Particles

2.1.1.1. Charge Generation by Heavy Charged Particles

As heavy charged particles such as alphas, and protons, pass through a material, they interact with many of the orbital electrons of the absorber [1]. This is as a result of the coulomb forces between the charged particles and the negatively charged electrons. The electrons gain energy at the expense of the decelerating incident particle and are either raised to a higher energy level (excitation) or freed from the host atom (ionisation). The energy imparted to an individual electron depends upon its proximity to the path of the particle, those closest may have sufficient kinetic energy to ionise further atoms. These energetic electrons or "delta rays" provide a means for indirect transfer of energy to the absorber, and typically account for most of the energy absorption. However their range is very small so they do not significantly influence the distribution of generated charge.

The energy loss, and hence charge generation of the particle as it passes through the material, is described as the "linear stopping power", and is given by the expression of Bethe, as;

$$-\frac{dE}{dX}=\frac{4\pi e^4 z^2}{m_0 v^2}NB \qquad (2.1)$$

where

$$B=Z[\ln(\frac{2m_0v^2}{I})-\ln(1-\frac{v^2}{c^2})-\frac{v^2}{c^2}]$$

v is the velocity and ze the charge of the incident particle, N the number density and Z the atomic number of the the absorber, and m_0 and e the rest mass and charge of the electron. I is the average excitation and ionisation potential of the absorber and normally has to be determined experimentally. In the case of a multiply-charged positive projectile, if the absorber is thick enough, the particle will lose sufficient energy that charge exchange with the absorber becomes significant. Electrons are then picked up, so neutralising the charge of the particle, which is brought to rest in a neutral state. As the Bethe formula takes no account of this charge exchange it is not valid towards the end of the particle's path

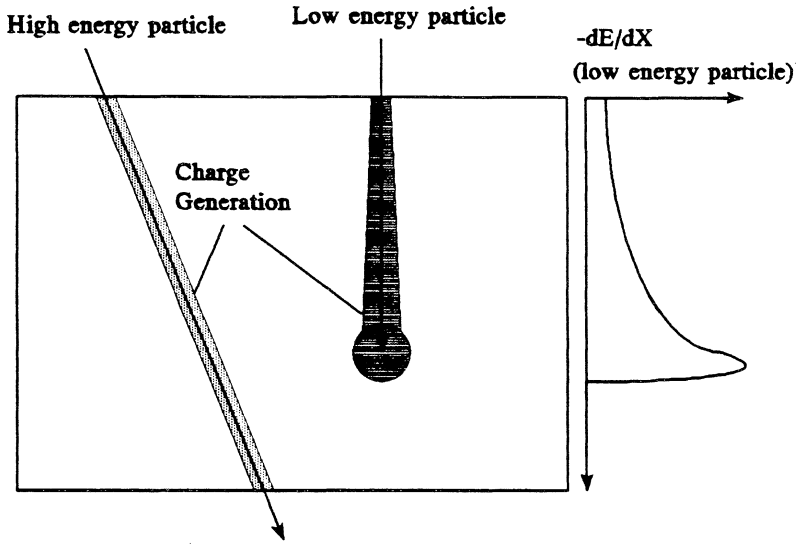


Fig 2.1 charge generation by alpha and proton

Heavy charged particles incident upon a CCD will leave a trail of charge in the form of electron-hole pairs, as shown, the range being dependent upon the energy of the particle and the target material. Particles of energy below a threshold value will be absorbed entirely within the 20μm epitaxial silicon layer, whereas those of higher energy will pass through the layer and into the substrate. For

the alphas this threshold energy is about 5MeV, compared to just above 1MeV for the proton [2].

The charge generated in the silicon constitutes signal if the CCD is in use for the purpose of particle detection, or noise if another purpose is intended, but in either case there will be no long term consequences. Charge generated in the dielectric layer however is likely to lead to build up of both fixed charge, and interface states. As described in section 2.2.2. this has implications for the operation of the device.

2.1.1.2. Charge Generation by High Energy Electrons

High energy electrons passing through a material undergo interaction with the orbital electrons of the material, as do heavy charged particles. The nature of the interactions differ however in that the incident particle is now of similar mass to the orbital electrons, and of similar charge. The incident electrons suffer much greater deviations in path, and can surrender far more of their energy in individual encounters. Also the electrons lose energy in the form of radiation, or bremsstrahlung, as they are accelerated during these deviations. For high energy electrons it is necessary to amend the Bethe expression for linear energy transfer of a heavy charged particle (Eq 2.1) in order to take account of the negative charge of the electron. Also an extra term is added to allow for energy loss by radiation. The specific energy loss due to collisions is given by;

$$-\frac{dE}{dX_c}=\frac{2\pi e^4 NZ}{m_0 v^2}\left[\ln\left(\frac{m_0 v^2 E}{2I^2(1-\beta^2)}\right)-(\ln 2)(2\sqrt{1-\beta^2}-1+\beta^2)+(1-\beta^2)+\frac{1}{8}(1-\sqrt{1-\beta^2})^2\right]$$

where $\beta = v/c$

and the specific energy loss due to radiative processes is given by;

$$-\frac{dE}{dX_r}=\frac{NEZ(Z+1)e^4}{137 m_{0_2} c^4}\left[4\ln\left(\frac{2E}{m_0 c^2}\right)-\frac{4}{3}\right]$$

The ratio of the two types of energy loss approximates as:

$$\frac{dE}{dX_r} / \frac{dE}{dX_c} \cong \frac{EZ}{700}$$

with E in MeV. Therefore it can be seen that radiative losses are only important for high electron energies, and absorbers of high atomic number.

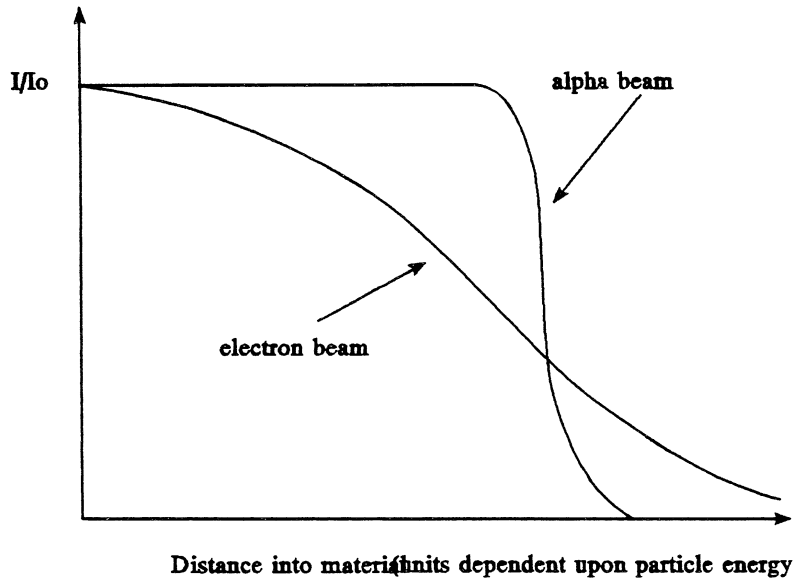


Fig 2.2. Attenuation of electron and alpha beams passing through a material.

Although an electron beam will be gradually attenuated as it passes through silicon as opposed to the abrupt attenuation of a beam of heavy ions (Fig 2.2), the individual electrons will leave trails of charge in a similar way to the heavy charged particles. The energy required for an electron to have a high probability of passing right through the CCD epitaxial layer is approximately 70keV [1], electrons of lower energy are likely to deposit all of their energy within the 20μm epitaxial layer.

2.1.1.3 Atomic Defects caused by Charged Particles

Whilst the predominant interaction between a charged particle and its absorber is that between the particle and orbital electrons in the absorber, it is also possible for encounters between the particle and host atomic nuclei to take place. If the energy transfer from particle to host atom is great enough

then the atom can be displaced from its site in the lattice. This PKA (primary knock-on atom) will come to rest by losing energy as it passes through the absorber, possibly causing further bulk defects if it carries sufficient energy. Interstitial atoms, and vacancies resulting from this process are able to react with impurity atoms and other defects, so creating defects which are electrically active.

The outcome of a collision between a charged particle and an atomic nucleus can be characterised by determination of two parameters, the maximum possible recoil energy of a PKA following such a collision, and the mean recoil energy expected from all such collisions. For the case of heavy charged particles, with energies less than around 100MeV, these values can be calculated using classical mechanics, and are given respectively, by [3];

$$E_{MAX}=\frac{4E_P mM}{(m+M)^2} \qquad (2.2)$$

and,

$$E_{MEAN}=\frac{E_D \ln(E_{MAX}/E_D)}{(1-E_D/AE_{MAX})} \qquad (2.3)$$

where;

$$A=\frac{4mM}{(m+M)^2}$$

E_D is the displacement energy of the nucleus, E_P is the original particle energy, m is the particle mass and M is the mass of the nucleus.

Solution of equation 2.3 shows that the mean recoil energy is only a few times greater than the displacement energy E_D, and is much smaller than the maximum possible energy E_{MAX}.

For electrons the maximum energy transfer assumes greater significance as it implies an electron threshold energy, below which atomic displacement is not possible. As a result of the high velocities of energetic electrons, prediction of the outcome of collisions with atomic nuclei is complicated by the need for relativistic effects to be considered. The maximum energy transfer being given by [3];

$$E_{MAX}=\frac{2E_e(E_e+2m_ec^2)}{(Mc^2)}$$

where E_e is the electron energy and m_e is the electron rest mass.

The minimum displacement energy for silicon has been quoted at 12.9eV and 21eV, although the higher energy fits much of the experimental data more closely (see Summers [4]). If a minimum displacement energy of 13eV is assumed, the calculated threshold electron energy is about 140 keV, whilst if a minimum displacement energy of 21eV is assumed, this increases to 220keV.

2.1.2. Irradiation by Gammas and X-rays

2.1.2.1 Charge Generation

There are a number of different interactions between an incident photon and an absorber material which can lead to charge generation, the likelihood of each mechanism being a function both of the the absorber material and the energy of the photon.

Low energy photons, of less than about 80keV in silicon, tend to interact via the photoelectric effect, in which all of the photons energy is absorbed in a single collision with a host atom, resulting in the emission of a photoelectron. Higher energy photons tend to interact with orbital electrons in the absorber via Compton scattering. In this encounter the photon may lose more or less of its energy, depending how great the angle through which it is scattered. (These processes are considered in more detail in chapter 3.)

If the photon energy is greater than 1.02 MeV (twice the rest mass energy of an electron) then pair production is possible. As the photon passes through the coulomb field of an atomic nucleus it disappears and is replaced by an electron-positron pair. The positron and electron then share the excess energy originally carried by the photon (above 1.02MeV). The positron will subsequently itself be annhilated, the resulting two annhilation photons being secondary products of the

interaction. Both the electron and positron generate charge as they decelerate in the absorber, and further charge may be generated by Compton scattering of the annhilation photons. Pair production is the dominant process of absorption for photons of several MeV and greater.

2.1.2.2. Atomic Defects caused by Gammas

Gammas and x-rays cannot interact directly with atomic nuclei of an absorber. Indirect interaction is possible via the electrons produced during Compton scattering or photoelectric absorption of a photon. If the atomic displacement energy in silicon is taken to be 13eV (which is to the lower end of quoted estimates [4]), then in order that an atom in the absorber can be displaced it is necessary for electrons of above 140keV to be generated. Consequently x-rays of lower energy than this threshold are unable to cause bulk damage in silicon.

2.2. Degradation of CCD Performance by Irradiation

2.2.1. Charge Generation within the Device

As mentioned in section 2.1.1.1, charge generation within the silicon dioxide dielectric is the principal concern as far as long term effects are concerned. Any unwanted charge generation within the epitaxial silicon will form background noise, but will not cause a permanent degradation of device performance.

Silicon dioxide has a forbidden band gap of about 9eV, which implies that any photon of energy greater than this threshold can induce ionisation, and create an electron-hole pair. Because of loss of thermal energy to the oxide lattice during irradiation, it is found that the mean energy absorption required to form an electron-hole pair is around 17eV [5 p91]. This parameter, sometimes referred to as the "ionisation energy" determines the quantity of charge generated for a given deposition of radiation energy. The capacity of the charge cloud to interfere with device operation however is a function of several other parameters, including the nature of the absorbed radiation.

There are several mechanisms by which charged particles generated in the oxide layer of a device

can cause a permanent change in the device characteristics. However, in order that they can migrate from their site of creation to a position where they are either trapped to form a fixed charge, or can react with another agent in the oxide, they must avoid recombination with any particles of the opposite charge in the vicinity. The fraction of charge escaping recombination is referred to as the charge yield. This charge yield itself is a function of both the nature of the absorbed radiation and also the electric field strength in the oxide. The probability that an individual charge carrier will undergo recombination at any position in the oxide, is dependent upon the the density of charge carriers of the opposite sign, and also upon the time spent at that position. It is therefore found that high oxide fields, which cause charge carriers to be rapidly swept away from their site of creation, induce a greater yield than low oxide fields, and that radiation, such as low energy x-rays, which deposits its energy in tight bundles, induces a lower yield than radiation, such as high energy electrons, which deposits its energy in lower concentrations over a larger area [5,6,7,8].

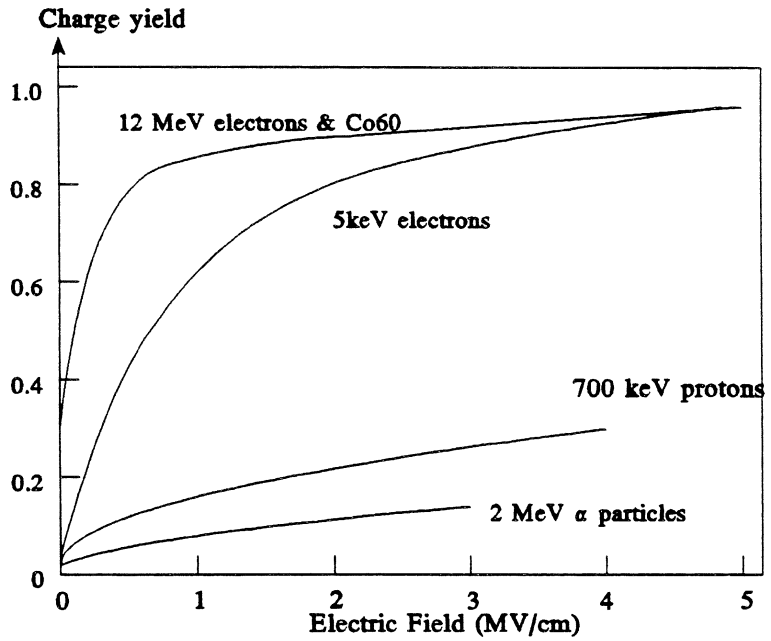


Fig 2.3. This plot shows the charge yield versus electric field strength for some types of radiation [6 fig 1].

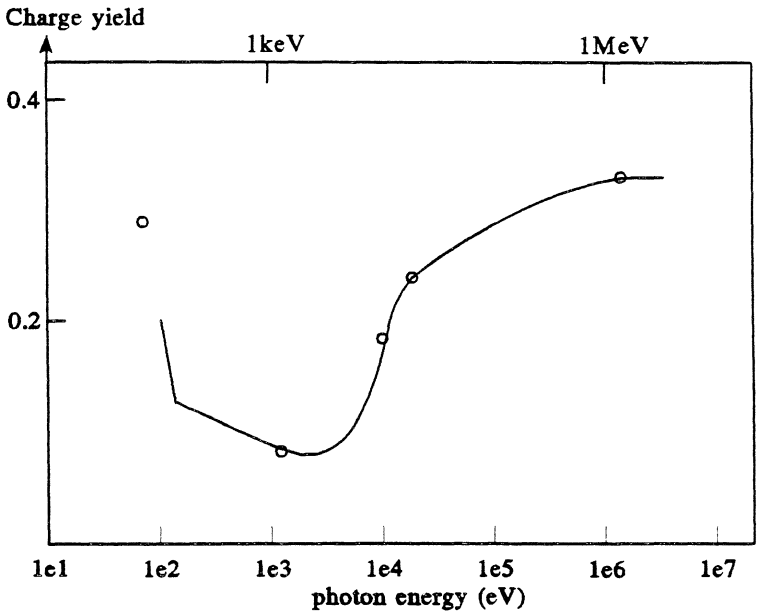


Fig 2.4 Plot showing electron-hole yield as a function of photon energy for a field of $0.3MVcm^{-1}$ [7 fig 7].

2.2.2. Permanent Effects caused by Radiation Induced Charge.

A number of effects have been identified in MOS systems, either directly caused by the charge carriers, or brought about as a result of interactions of the carriers within the oxide. Following the absorption of radiation, a cloud of electron-hole pairs will be formed. The high mobility electrons are swept out of the oxide within a few pico seconds, either towards the gate, or down into the substrate, depending upon the gate bias [5]. The holes, having a much smaller mobility will hardly have moved in this time. Those having escaped recombination are then able to migrate through the oxide, with a number of possible consequences.

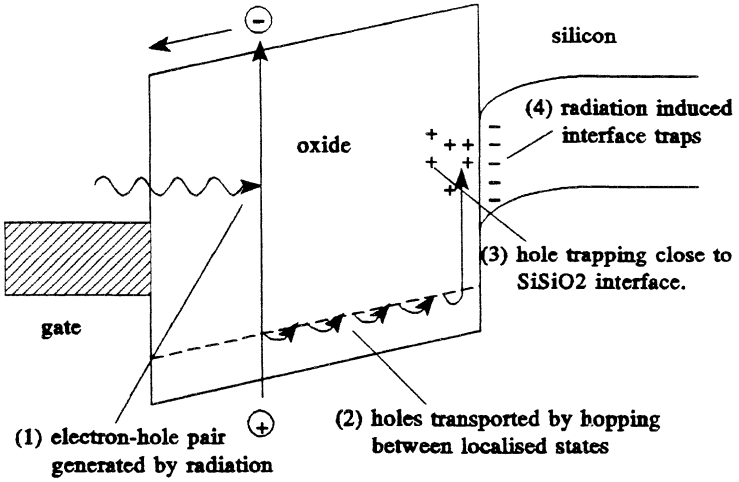


Fig 2.5. A schematic showing radiation induced effects in an MOS structure with positive gate bias [5 fig 3.1].

The course of this migration is dependent upon the structure of the device and the oxide field. In the case of an n-channel MOS structure under positive gate bias, the holes will move in the direction of the silicon/SiO_2 interface. Many will pass from the oxide into the substrate, where they will ultimately undergo recombination with electrons, but some will be retained in the oxide. Those holes failing to reach the substrate will either have have been trapped by local defects in the lattice or will have been annhilated as a result of interactions with agents in the oxide. As opposed to this, EEVs CCDs have an MNOS structure, and employ a negative oxide field, so it is necessary to consider the outcome of holes migrating in the direction of the SiO_2/Si_3N_4 interface. Hole trapping in the oxide can, for the purposes of CCD operation, be considered an instantaneous effect seen immediately after irradiation, whilst other hole interactions are likely to lead to more long term consequences.

2.2.2.1 Hole Trapping

Hole trapping in oxide layers is a function of both the radiation "hardness" of the oxide, and of the electric field in the oxide during irradiation. In radiation-hardened oxides (unlike the CCD) there are few traps in the bulk of the oxide, so most trapping occurs close to an interface where there is likely to be a higher concentration of lattice defects induced by mechanical stress. For the MOS structure this implies that for a positive oxide field most trapping of holes will occur at the silicon/oxide interface whilst for a negative field it would occur at the oxide gate interface. The

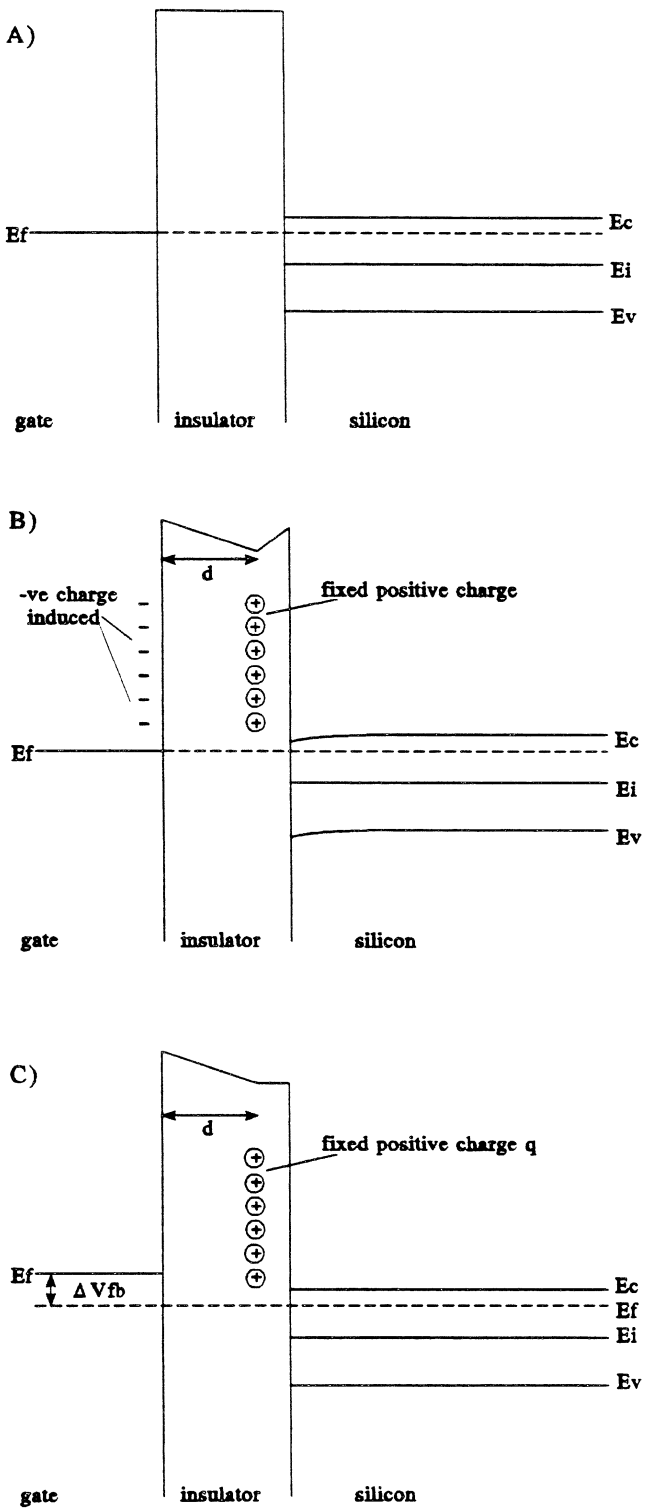


Fig 2.6 (a) An ideal n-MIS capacitor, (b) An MIS capacitor with band-bending induced by trapped +ve charge, and (c) Restoration of the flat-band condition by application of gate bias.

consequence of this hole trapping is to form a sheet of positive charge within the oxide. Fig 2.6 demonstrates the effect that a charge sheet positioned near to the silicon/oxide interface will have upon the operating characteristic of the device. A voltage is induced across the oxide, necessitating application of a gate bias in order to restore the structure to its original electrical "flat-band" condition.

In the case of a device fabricated with a soft oxide layer (less radiation hard) such as the CCD, hole trapping in the bulk of the oxide may not be negligible, and may cause the voltage shift to be greater than that predicted for the charge sheet alone.

Practically, the flat band condition of an unirradiated device is likely to be achieved for a non-zero gate bias, $V_G(fb)$ as a result of charge trapped in the oxide, and a mismatch between the work functions of the silicon and the gate material. It is therefore, the change in $V_G(fb)$ which is of interest and is referred to as the "flat-band voltage shift". The magnitude of the flat-band voltage shift is dependent upon a number of factors including dose, charge yield, oxide hardness and thickness (section 2.3.1.), and electric field direction (see fig 2.7 and 2.8).

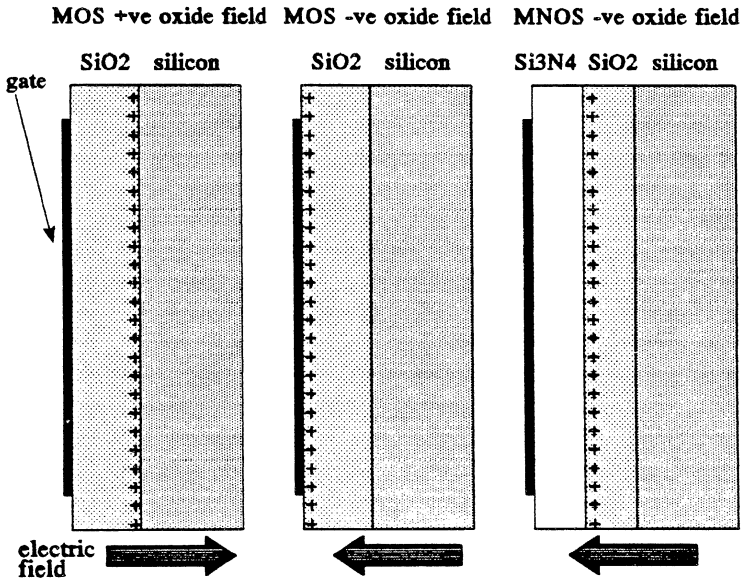


Fig 2.7. Position of sheet charge buildup for MOS and MNOS devices as a function of oxide field.

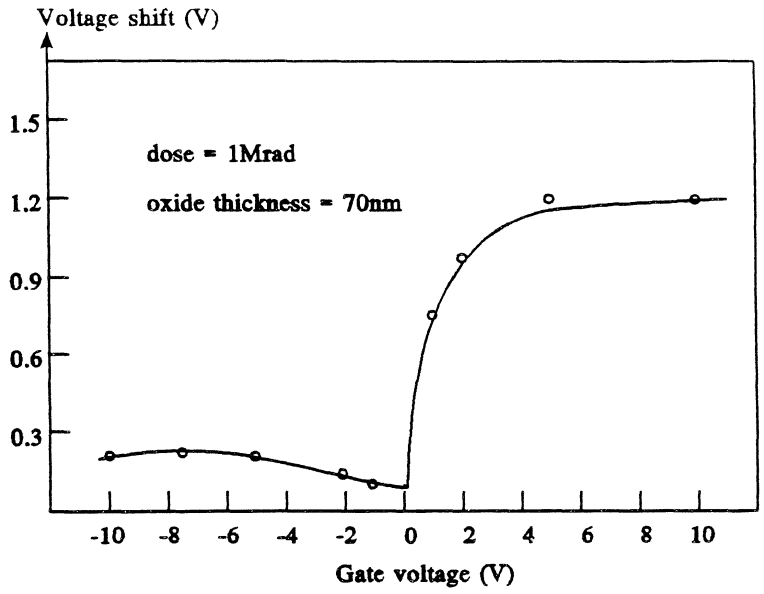


Fig 2.8. A typical radiation induced flat-band voltage shift in an MOS capacitor, as a function of gate bias during irradiation (for an oxide thickness of 70nm, and a dose of 1Mrad). [5 fig3.30].

As would be expected, the voltage shift seen for a MOS device device irradiated with a negative oxide field is smaller than that seen for a positive oxide field, because of the high capacitance which is presented to the sheet of trapped charge.

As mentioned in section 2.2.2., the CCDs being considered in this work have an MNOS structure (fig 1.12). An 85nm layer of Si_3N_4 separates the oxide layer from the polysilicon gate. The nitride itself can be considered hard because holes and electrons have a similar, low mobility, leading to a high rate of recombination [9,10]. Conduction in the Si_3N_4 films is a strongly dependent upon the defects present (see fig 2.9).

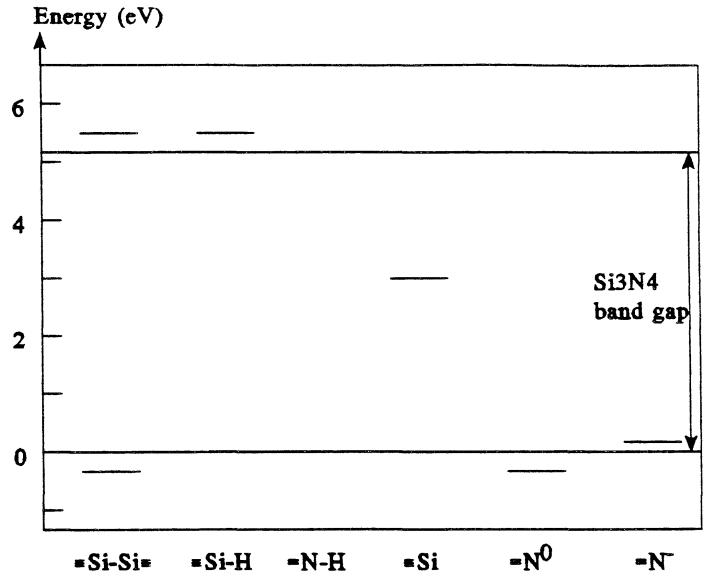


Fig 2.9. Summary of defect energy levels in Si_3N_4 [11].

The Si_3^0 dangling bond, positioned close to the centre of the bandgap, is amphoteric, and so can trap either a hole or an electron, whilst the N_2^0 dangling bond sits at the top of the valence band. Because of the relative positions of the states, it is found that at equilibrium only the states Si_3^0, Si_3^+, and N_2^- exist [12]. The N_2^- states are thought responsible for Poole-Frenkel hole conduction, whilst the deep Si_3^+ centres are responsible for trapping and consequently slowing the drift of electrons [12 p25]. Whereas for SiO_2, electron mobility is typically several orders of magnitude greater than hole mobility [5 p91], Yun [13] found that in CVD Si_3N_4 films the hole mobility exceeded the electron mobility by a factor of around 3.

Whilst the nitride does not contribute to the charge trapping directly, it does provide an interface with the oxide at which trapping of holes generated in the oxide can occur (see fig 2.7). Because of the negative oxide field employed during operation, this Si_3N_4/SiO_2 interface is of primary importance in determining the post-irradiation flat-band voltage shift seen in these devices.

For small doses the voltage shift may not be a problem, but for larger doses the it may take the device out of its operating domain, eventually resulting in device failure.

2.2.2.2. Interface State Buildup

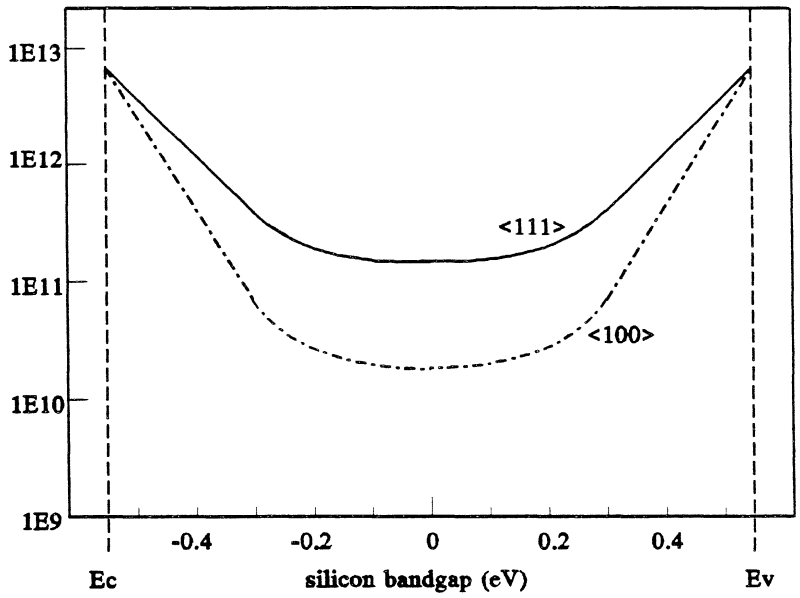


Fig 2.10. Typical density of Si/SiO_2 interface states, through the silicon bandgap [14,15].

The term "interface states" refers here, to electronic states in the proximity of the Si/SiO_2 interface with energy levels falling within the silicon bandgap. If they are within around 5nm of the interface they are able to exchange charge with the silicon conduction and valence bands [5]. Interface states exist at an Si/SiO_2 interface even in unirradiated structures (see fig 2.10). This is because during the oxidation of the silicon there is a deficiency of oxygen very close to the interface, which causes there to be strained, and dangling silicon bonds, which in turn act as traps within the bandgap. Whilst the behaviour of these states is still a matter of some contention [5 p196], it is considered most likely that those falling below mid-bandgap behave as donors, being positively charged when empty and neutral when full, and that those falling above mid-bandgap behave as acceptors, being negative when full and neutral when empty. This has consequences for the net charge of the interface states, as shown in fig 2.11.

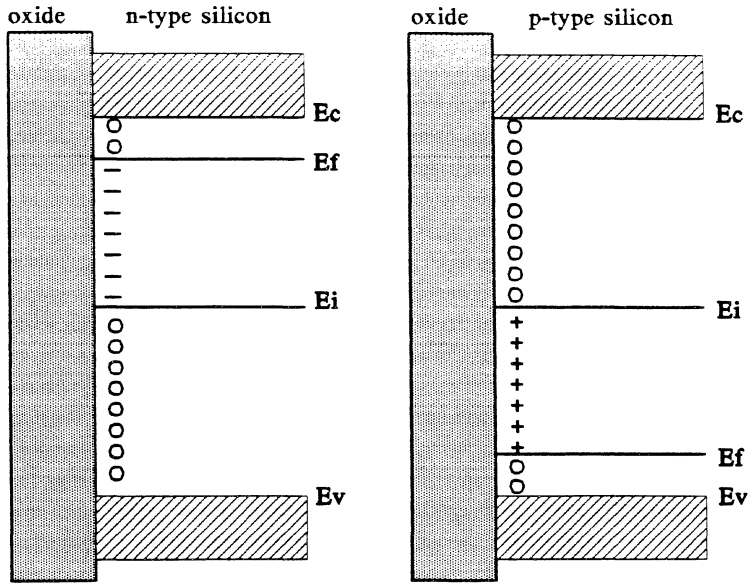


Fig 2.11. This shows the net charge caused by a buildup of interface states in n-MOS and p-MOS oxide interfacses.

Todays high quality stuctures have enabled the density of these process induced traps to be minimised (around 1 x 10^{10} $cm^{-2}eV^{-1}$ at the centre of the bandgap [12]), but in the case of CCD02s and CCD05s they are still responsible for almost all the dark current seen in unirradiated devices at room temperature. Also the presence of a high concentration of interface states can have implications for the flat-band condition of the device (see fig 2.11). The BCCD does not suffer a loss of CTE as a result of interface state buildup because its design specifically ensures that the signal charge remains remote from the interface, deep in the n-channel. Although for a SCCD, interaction between signal electrons and interface states is clearly possible, illustrating a weakness of this technology.

Interface state density is known to increase following irradiation of both MOS and MNOS structures, and brings about a corresponding increase in dark current in CCDs. Although the mechanism by which this happens has yet to be clearly understood, three models have been suggested [16].

By far the largest effect is the transport of hydrogen ions, liberated by radiation generated holes in the oxide, towards the Si/SiO_2 interface. It was proposed by Oldham et al [16] that the hydrogen ion is liberated by an interaction between the hole and the hydrogen's binding electron leading to the annhilation of both. Saks and Brown [17] however found that the maximum buildup in interface

states occurred for zero applied oxide field during irradiation. This led them to suspect that the generation of hydrogen ions in the oxide is proportional to the number of electron-hole pairs recombining, and that the hydrogen ions are freed from weak bonds (possibly the OH defect) as a result of the energy released in the recombination process. Once the hydrogen ion is created it is able to hop between adjacent oxygen atoms, bonding temporarily with the non-bonding lone pair orbitals of the oxygen atom. On reaching the interface the ion is able to combine with a hydrogen atom which is acting as passivation to an interface state, thus exposing the state [16]. There is also evidence to suggest that hydrogen ions can be generated post-irradiation if the SiO_2 is re-exposed to hydrogen. For this to occur it is thought that positively charged, radiation induced defects in the oxide lead to the cracking of hydrogen molecules, with one hydrogen ion being released as an ion and the other neutralising the defect [18].

This migration of ions through the SiO_2 is very heavily field dependent, and is the slowest of the processes, being responsible for a gradual buildup of interface states over a timescale varying from hours to years,as determined by temperature and oxide field. Oldham et al [16] suggest that the temperature dependence corresponds to an effective activation energy of 0.82eV for zero applied field.

The second largest process correlates with the expected time of arrival of radiation induced holes at the Si/SiO_2 interface (see also [19,20]), the implication being that on reaching the interface some of the holes undergo trapping/transformations which yield a defect, and that the process occurs much more quickly than the hydrogen ion migration (less than 1ms). This process typically accounts for around 10% of total buildup, although it is sometimes larger.

The process likely to make the smallest contribution to interface state buildup is fast and field independent. Believed to be caused by the diffusion of neutral hydrogen to the Si/SiO_2 interface, this process would normally not be seen at room temperature. As the activation energy of neutral hydrogen migration is around 0.3eV it has been observed at temperatures of 120 - 150K where the field dependent processes are eliminated (see Griscom et al [21]). One theory put forward to explain release of neutral hydrogen in the oxide is that excitons, or bound electron-hole pairs, generated by the radiation survive for long enough that they are able to reach a hydroxyl group in the oxide and then recombine so releasing sufficient energy to break the O-H bond.

The common factor linking each of these processes is the requirement that electron-hole pairs be

generated as a trigger. Although it is also possible that some interface states are caused directly by the interaction of radiation at the interface, what is not in dispute is that the minimum photon energy able to induce interface states corresponds to the 9eV energy bandgap of SiO_2 [5 p242]. Therefore it seems certain that all interface state buildup originates with the production of an electron-hole pair.

2.2.3. Atomic Displacements in the CCD

The formation of defects within the oxide layer may provide a sites for subsequent hole trapping and therefore have implications for buildup of fixed charge in the oxide but will not contribute to dark current in the silicon layer unless they are very close (5nm or less) to the interface. Atomic displacements within the silicon layer are of far greater concern. Defects providing traps with energy levels which fall into the silicon bandgap will be liable to cause an increase in dark current, (see section 2.3.2.) and also reduce charge transfer efficiency. CTE is affected by the inclination of these defects to act as trapping sites causing temporary removal of charge from the signal. [2 p221] If the charge is not released until a subsequent charge packet has arrived under the gate then a loss of signal results. The magnitude of the CTI resulting from such traps is a function of the trap density, and also of the clocking parameters of the device, and of the electron emission and capture time constants of the trap [22,23].

2.3 Relating Radiation Effects to Parametric Changes.

As the aim of this work is to characterise the response of BCCDs to 70kVp x-rays, atomic displacements, and consequently CTE degradation, are not a concern. The device parameters which are vulnerable to this nature of radiation are the dark current level and the flat-band voltage status.

2.3.1. Flat-band Voltage Shift

Two factors contribute to the flat-band voltage shift seen in MOS devices following irradiation. These are trapped charge in the oxide, and states formed at the Si/SiO_2 interface.

2.3.1.1. Effect of Trapped Oxide Charge on Flat-band Voltage.

For an MOS device irradiated with a positive oxide bias, a charge sheet will be therefore be formed close to the Si/SiO_2 interface (see fig 2.8). Assuming that few holes are trapped in the bulk of the oxide, and that recombination of electrons with trapped holes is negligible, the number of trapped holes, N_h, forming this sheet is given by [5 p152];

$$N_h = 2.2\times10^{-2}\times\frac{Dd_{OX}A_{OX}F_YF_T}{\epsilon}$$

where the constant takes account of the density of SiO_2 and the krad as the unit of dose, D is the dose, d_{OX} is the oxide thickness,(cm), A_{OX} is the area of the oxide interface,(cm^2), F_Y is the field and radiation dependent charge yield, F_T is the field dependent fraction of trapped holes, and ϵ is the mean energy cost of creating each electron-hole pair,(eV^{-1}).

the charge per unit area Q_{OT}, is therefore given by;

$$Q_{OT} = 2.2\times10^{-2}\times\frac{qDd_{OX}F_YF_T}{\epsilon}$$

where q is the electronic charge.

Assuming that the charge sheet is effectively positioned adjacent to the interface, then from fig 2.7 it can be seen that this sheet of trapped holes is effectively charging the capacitance of the oxide layer. The flat-band voltage shift resulting from this charge sheet, ΔV_{OT}, is therefore given by;

$$\Delta V_{OT} = \frac{Q_{OT}d_{OX}}{\xi_0\xi_{OX}}$$

or,

$$\Delta V_{OT} = 2.2\times10^{-2}\times\frac{qDF_YF_Td_{OX}^2}{\epsilon\xi_0\xi_{OX}} \qquad (2.4)$$

where ξ_0 is the permittivity of free space ($C^2N^{-1}m^{-2}$), and ξ_{OX} is the dielectric constant of the oxide.

This expression illustrates the strong dependence of voltage shift upon oxide thickness, for MOS devices operated with a positive oxide field, and implies that an effective way to improve the radiation hardness of a device is to reduce the oxide thickness.

If hole trapping in the bulk oxide proves to be significant, as may be the case in some soft oxides then another term has to be added to equation 2.4, to take account of the voltage induced by the trapped bulk charge, so ΔVot becomes;

$$\Delta V_{OT} = \frac{Q_{ST} d_{OX}}{\xi_0 \xi_{OX}} + \int_0^{d_{OX}} \frac{Q_B(x)}{\xi_0 \xi_{OX}} dx$$

where Q_{ST} is the charge density of the charge sheet, (Ccm^{-2}), and $Q_B(x)$ is the trapped charge concentration (Ccm^{-2}) as a function of depth x (cm) from the gate into the bulk oxide.

For an MNOS device irradiated with a negative oxide field (as is the case for a BCCD), the situation is somewhat different. The charge sheet is formed at the SiO_2/Si_3N_4 interface, and so the capacitance of the nitride layer is charged. Consequently the voltage shift induced by the charge sheet is now given by;

$$\Delta V_{ot} = 2.2 \times 10^{-2} \times \frac{qDd_{ox}F_y F_{t(nit)} d_{nit}}{\epsilon \xi_0 \xi_{nit}}$$

where d_{nit} is the thickness of the nitride layer, and $F_{t(nit)}$ is the field dependent fraction of holes trapped at the SiO_2/Si_3N_4 interface.

In either case the accumulation of fixed positive charge means that the flat-band voltage shift will be negative.

2.3.1.2. Effect of Interface States on the Flat-band Voltage.

The density of interface states, $D_{it}(E)$ normally has a continuous distribution throughout the silicon bandgap (fig 2.9). As mentioned in section 2.2.2.2., states positioned above the silicon midgap are expected to behave as acceptors, whilst those below are expected to behave as donors. Therefore in the case of an oxide interface with n-type silicon, the net charge of the interface traps is negative, whilst for an interface with p-type silicon the net charge is positive. For an n-type substrate, the charge per unit area Q_{it} resulting from the interface states, is given by [22] (see fig 2.11);

$$Q_{it}=q\int_{Ef}^{Ei}D_{it}(E)dE$$

It should be remembered that an applied field will cause some states to pass through the Fermi level, so affecting the net charge of the interface states.

If an additional number of interface states $\Delta D_{it}(E)$ are generated by irradiation. Then in the case of an MOS device, this will cause a flat-band voltage shift ΔV_{it} given by;

$$\Delta V_{it}=q\int_{Ef}^{Ei}\frac{\Delta D_{it}(E)}{C_{ox}}dE$$

where $C_{ox} = \xi_0\xi_{ox} / d_{ox}$

and in the case of an MNOS device it will cause a flat-band voltage shift given by;

$$\Delta V_{it}=q\int_{Ef}^{Ei}\frac{\Delta D_{it}(E)}{C_{ins}}dE$$

where C_{ins} is the capacitance per unit area of the double layer dielectric, $(C_{ox} + C_{nitride})^{-1}$

2.3.1.3 Overall Flat-band Voltage Shift

The total radiation induced flat-band voltage shift ΔV_{tot}, is the sum of the two components described in section 2.2.1.2., and is given by;

$$\Delta V_{tot} = \Delta V_{ot} + \Delta V_{it}$$

2.3.2. Dark Current Increase

There are several possible sources of dark current in the CCD. In the silicon bulk, charge can be generated in both the depleted and undepleted regions, and also at the interface between the p-type epitaxial layer and the heavily doped p+ substrate. In addition, there are two Si/SiO_2 interfaces, that of the n-channel, and that of the p-stop, which will contribute charge generation Defects either in the silicon or at the oxide interface, are able to interact with charge carriers in the ways shown in fig 2.12.

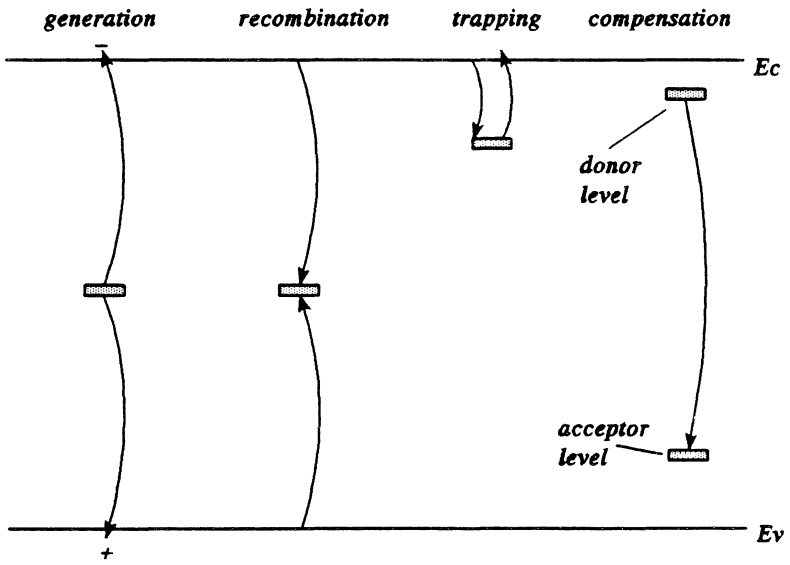


Fig 2.12. Interactions between traps and charge carriers

Electron and hole recombination rates via such a trap, are are governed by Schockley-Read-Hall statistics [24] and predict the steady state dark current contributions described in the next section [12 p67-76, after 25].

2.3.2.1 Bulk Silicon Dark Current

For depleted bulk silicon, it is assumed that electron and hole concentrations are equal to zero, which leads to the following expression for generation from a single trap level;

$$J_{DB} = \frac{qW_D n_i^2}{\tau_h(\epsilon_e/c_e) + \tau_e(\epsilon_h/c_h)} \qquad (2.5)$$

where J_{DB} is the dark current density in Acm^{-2}, and W_D is the depletion region depth in cm.

c_e and c_h are the electron and hole capture coefficients (cm^3s^{-1}), and are given by $c = \sigma v_{th}$, where σ is the capture cross-section of the particle (cm^2), and v_{th} is the thermal velocity (cms^{-1}).

ϵ_e and ϵ_h are the electron and hole emission constants (s^{-1}) given by; $\epsilon_e = c_e n_i \exp[(E_t - E_i)/KT]$ and $\epsilon_h = c_h n_i \exp[-(E_t - E_i)/KT]$, where E_t and E_i are the trap level, and the intrinsic fermi level.

τ_e and τ_h are the electron and hole minority carrier lifetimes, given by; $\tau = (\sigma v_{th} N_t)^{-1}$, where N_t is the trap density (cm^{-3}).

this can be simplified to

$$J_{DB} = \frac{qW_D n_i}{\tau_0}$$

where τ_0 is the effective generation lifetime within the depletion region, and is given by

$$\tau_0 = \tau_h \exp\frac{(E_t - E_i)}{KT} + \tau_e \exp\frac{-(E_t - E_i)}{KT}$$

Charge generation from undepleted p-type silicon is treated by assuming the electron concentration to be zero. If we also assume that the width of the epitaxial silicon layer is much less than the minority carrier diffusion length L_e, then charge contribution to the dark current approaches total

charge generation, and approximates as;

$$J_{UB} \approx \frac{qW_D n_i^2}{\tau_h(\epsilon_e/c_e)+\tau_e(\epsilon_h/c_h)+N_A\tau_e}$$

Roy [12] estimated the minority carrier duffusion length in the epitaxial layer to be of the order of 330μm. This suggest that about 95% of the generated charge will actually reach the n-channel to contribute to the dark current. However, for temperatures below 100°C the term, "$N_A \tau_e$" dominates the denominator, so suppressing dark current generation (c.f. equation 2.4 for the depleted region dark current) and imposing a dependence upon n_i^2. At room temperature this diffusion current can be neglected [12].

2.3.2.2. Dark Current from Silicon Surfaces

For a depleted silicon surface, with a continuous distribution of traps throughout the silicon bandgap, assuming that the charge generation all takes place via traps close to the peak energy level for charge generation,E_m, given by, $E_m = E_i - KT/2 \ln(\sigma_{es}/\sigma_{hs})$ where E_i is the intrinsic fermi level, and assuming that trap density is not a strong function of energy close to this level, then;

$$J_{DS}=0.5\times q\pi KT\frac{D_{it}^*}{\tau}$$

where J_{DS} is the dark current density from the silicon surface, D_{it}^* is the average interface density close the energy level E_m ($cm^{-2}eV^{-1}$) and $\tau = (n_i v_{th} (\sigma_{es}\sigma_{hs})^{0.5})^{-1}$, where $\sigma_{es}$and σ_{hs} are the surface state equivalents of $\sigma_e$and σ_h [12,25].

For surfaces which are not permanently depleted, the time dependent dark current contribution has to be considered, and is given normalised to the steady state contribution, as;

$$\frac{J_{DS}(t)}{J_{DS}(\infty)} = \frac{2}{\pi}\int_0^{\infty} \exp[-(X+X^{-1})\frac{t}{\tau}]\frac{dX}{(1+X^2)}$$

where

$$X = \sqrt{\frac{\sigma_{en}}{\sigma_{hn}}}\exp[\frac{(E-E_i)}{KT}]$$

Roy solved this expression numerically, and found that for any given duration of depletion, two temperature thresholds exist. Above the higher of these thresholds charge generation reaches the steady state value, whilst below the lower threshold charge generation is negligible. In the intermediate region $J_{DS}(t) / J_{DS}(\infty)$ is temperature dependent. Therefore, any surfaces which are intermittently depleted as a resulting of clocking of the CCD, will show an extra temperature dependence as far as dark current is concerned. The temperature thresholds are a function of the duration for which the surface is depleted, and also of the electron and hole capture cross-sections.

References for Chapter 2

[1] G.F. Knoll, "Radiation Detection and Measurement", Published by John Wiley and Sons, 1989.

[2] A.H. Siedle, and L. Adams, "Handbook of Radiation effects", Published by Oxford University Press, 1993.

[3] M.W. Thompson, "Defects and Radiation Damage in Materials", Published by Cambridge University Press, 1969.

[4] G.P. Summers, "Damage Correlations in Semiconductors Exposed to Gamma, Electron, and Proton Radiations", IEEE Trans. Nucl. Sci., Vol 40, 6, 1372-1379, 1993.

[5] T.P. Ma, and P.V. Dressendorfer, "Ionizing Radiation Effects in MOS Devices and Circuits", Published by John Wiley and Sons, 1989.

[7] C.M. Dozier, and D.B. Brown, "Effect of Photon Energy on the Response of MOS Devices", IEEE Trans. Nucl. Sci. NS-28, 6, 4137-4141, 1981.

[8] C.M. Dozier, and D.B. Brown, "Photon Energy Dependence of Radiation Effects in MOS Structures", IEEE Trans. Nucl. Sci., NS-27, 6, 1694-1699, 1980.

[9] N.S. Saks, "Response of MNOS Capacitors to Ionizing Radiation at 80K", IEEE Trans. Nucl. Sci., NS-25, 6, 1226-1233, 1978.

[10] N.S. Saks, J.M. Killiany, P.R. Reid, and W.D. Baker, "A Radiation Hard MNOS CCD for Low Temperature Applications", IEEE Trans. Nucl. Sci., NS-26, 6, 5074-5079, 1979.

[11] J. Robertson, "Electronic Structure of Silicon Nitride", Phil. Mag. B, 63(1), 47-77, 1991.

[12] T. Roy, "Ionising Radiation Induced Surface Effects in Charged Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, 1993.

[13] B. H. Yun, "Electron and Hole Transport in CVD Si_3N_4 Films", Appl. Phys. Lett., 27(4), 256-258, 1975.

[14] M.H. White, and J.R. Cricchi, "Characterization of Thin-oxide Memory Transistors", IEEE Trans. Electron. Dev., Vol ED-19, 12, 1280-1288, 1972.

[15] P. Balk, "The Si-SiO_2 System", Published by Elsevier Science, 1988.

[16] T.R. Oldham, F.B. McLean, H.E Boesch Jr, and J.M. McGarrity, "An Overview of Radiation -induced Interface Traps in MOS Structures", Semicond. Sci. Technol. Vol 4, 986-999, 1989.

[17] N.S. Saks and D.B. Brown, "Interface Trap Formation Via the Two-Stage H^+ Process", IEEE Trans. Nucl. Sci., Vol 36, 6, 1848-1857, 1989.

[18] B.J. Mrstik, and R.W. Rendell, "Si/SiO_2 Interface State Generation During X-ray Irradiation and During Post Irradiation Exposure to a Hydrogen Ambient", IEEE Trans. Nucl. Sci. Vol 38, 6, 1101-1110, 1991.

[19] J.R. Schwank et al, "The Role of Hydrogen in Radiation Induced Defect Formation in Polysilicon Gate MOS Devices", IEEE Trans. Nucl. Sci., NS-34, 6, 1152-1157, 1987.

[20] H.E. Boesch Jr, "Time-dependent Interface Trap Effects in MOS Devices", IEEE Trans. Nucl. Sci., Vol 35, 6, 1160-1167, 1988.

[21] D.L. Griscom, D.B. Brown, and N.S. Saks, "Nature of Radiation Induced Point Defects in Amorphous SiO_2 and their Role in SiO_2-on-Si Structures" part of "Physics and Chemistry of SiO_2 and the Si-SiO_2 Interface", edited by C.R. Helms and B.E. Deal,Published by Plenum, 1988.

[22] M.S. Robbins, "Radiation Damage Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, 1992.

[23] S.J. Watts, H. Holmes-Siedle, and A, Holland, "Further Evaluation of X-ray Sensitive Charge Coupled Devices (CCDs) for the XMM Telescope", Final Report, ESTEC Contract 8815/90/NL/LC(SC), Brunel University, Uxbridge, UB8 3PH. 20 Oct 1995.

[24] W. Shockley, and W.T Read, "Statistics of the Recombination of Holes and Electrons", Phys. Rev., Vol 87, 835-842, 1952.

[25] R.F. Pierret, "Advanced Semiconductor Fundamentals", Volume VI of "Modular Series on Solid State Devises", Published by Addison Wesley, 1987.

X-ray Dosimetry Considerations

3.1. Radiation environment

Previous work by Robbins [1] and Roy [2] has characterised the effects in these devices when used for scientific purposes in a radiation environment. Here the threat was likely to come predominantly from unwanted background levels of radiation, rather than from the signal particles themselves. The aim of this project was to appraise the damage incurred by devices used for X-ray imaging in an otherwise non-hostile environment. In this instance all performance degradation is caused by the X-ray photons themselves. The maximum operational lifetime of a device will be determined by the relationship between the damage caused by a photon, and the signal information imparted by it. A typical spectrum used in dental imaging is 70kVp from a tungsten source (see fig 3.1 and [3]), hardened by 2mm of aluminium. Photons with energies ranging from about 15keV to 70keV are incident upon the device itself.

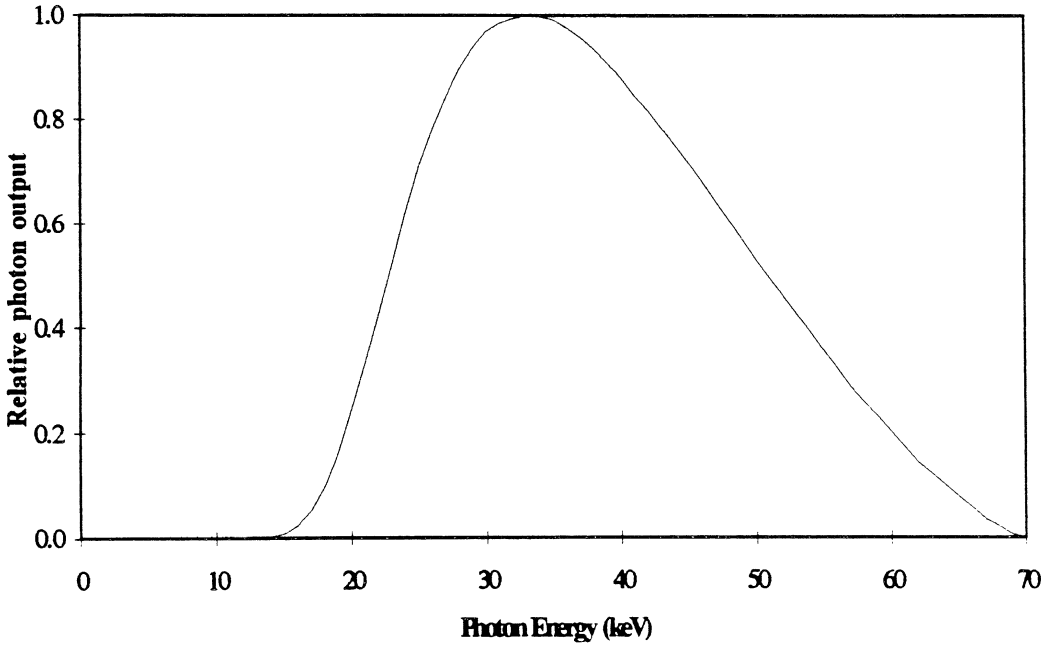


Fig 3.1. A normalised 70kVp X-ray spectrum from a tungsten source (see [3]).

The source used throughout this work is a d.c. self-rectifying single peak source, whereas the spectrum shown in fig 3.1 is for a constant potential source. The Hospital Physicists' Association Catalogue [3] implies that the spectrum from a single peak source is softer than that from a constant potential source, with fewer photons towards the peak energy. This difference is quantified in terms of the penetration of a 60kVp beam through various thicknesses of aluminium.

In order to test for any significant discrepancy between the single peak 70kVp X-ray beam used in this work, and the constant potential spectrum shown in fig 3.1, the relative penetrations of the two were compared, as shown in fig 3.2. The penetration values for the single peak source were determined experimentally, whilst the penetration values for the constant potential source were calculated from fig 3.1, and known attenuation coefficients.

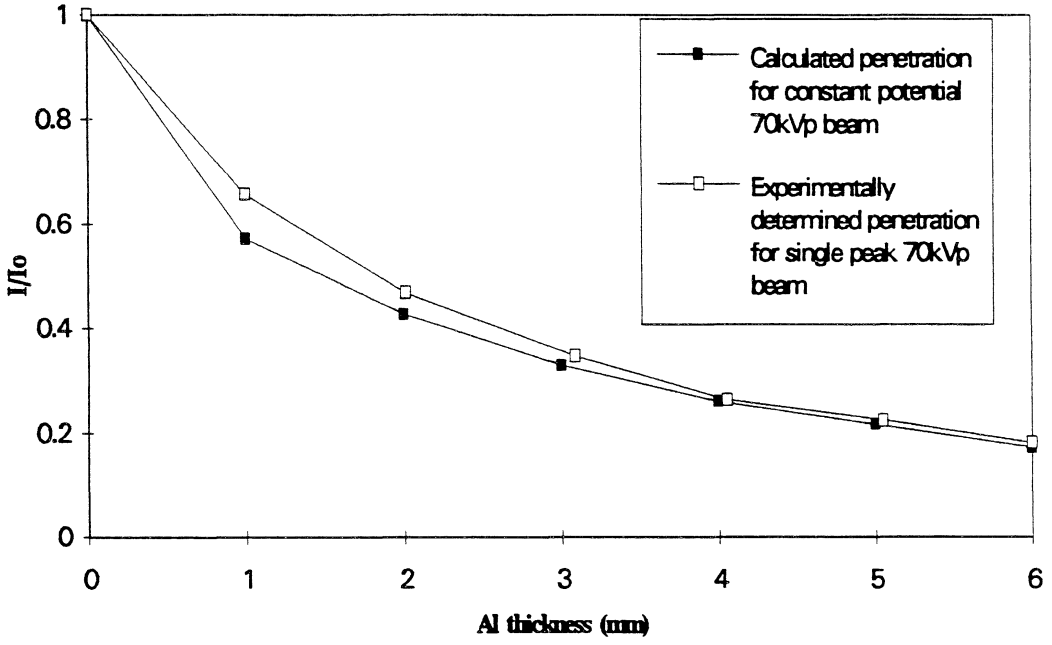


Fig 3.2. Comparison between the penetration (through aluminium) of the constant potential 70kVp spectrum shown in fig 3.1, and the 70kVp spectrum obtained from the self-rectifying, single peak, source used for this work.

As shown in fig 3.2. the penetrations of the two beams differ significantly only for thicknesses of

aluminium upto 2-3mm. In this region the penetration observed for the single peak source is greater than that predicted for the constant potential source. This suggests that the internal hardening filters in the single peak source do not harden the beam as effectively as the 2mm aluminium hardening filter quoted for spectrum 3.1 [3]. For thicknesses of aluminium greater than 3mm the penetration of the two beams are similar suggesting that once the soft X-rays are removed, both spectra are of similar hardness. For the irradiations performed during this work an external 2mm aluminium filter was used to remove the soft X-rays.

The principal cause of radiation induced flat-band voltage shifts is the build up of holes, as a result of photon absorption in the dielectric, whereas the signal is derived from photon absorption in the epitaxial silicon layer. Approximately 17eV is required to liberate one electron-hole pair in the oxide, compared to 3.6eV in the silicon (see for example, [4]). Thus one 70keV X-ray photon has the capacity to generate thousands of electron-hole pairs which may either contribute to the signal, or cause damage, dependent upon where the photon is absorbed. For the EEV CCDs it is found that a dose of 0.4 rad (silicon), which is approximately 0.05 rad (tissue) in this energy range (see fig 3.3), is sufficient to give good image quality. This corresponds to approximately 1.6×10^5 electrons per pixel, for conventional devices without a scintillator coating.

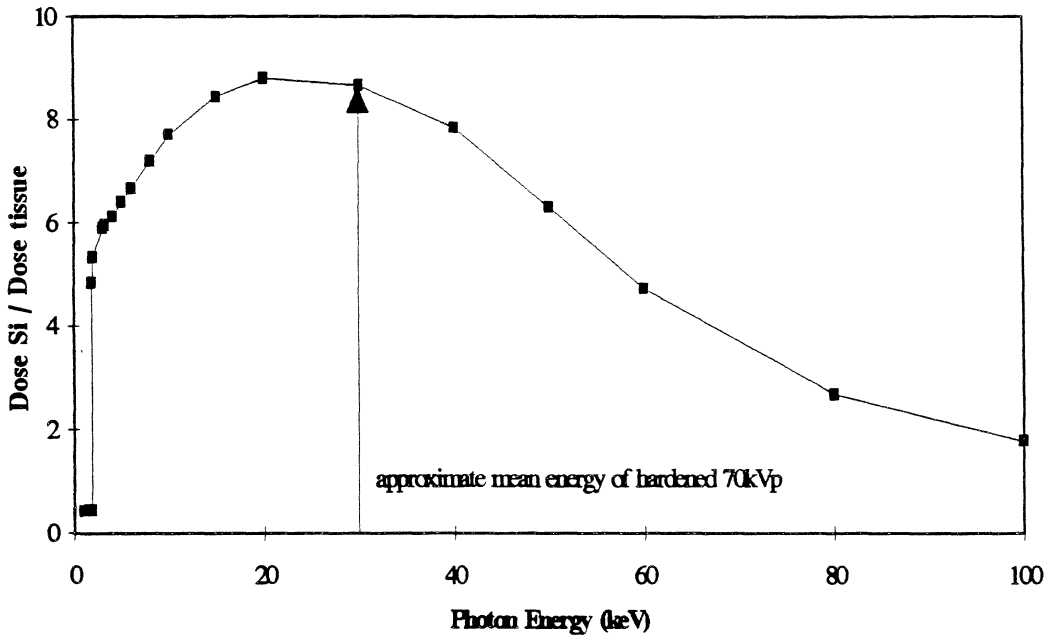


Fig 3.3. The ratio of dose seen by Si to dose seen by tissue for low energy X-rays

3.2. X-Ray Absorption by the CCD

The CCD is a multilayered structure consisting of silicon layers, oxide layers and a nitride layer (see fig 1.12). For each of these materials, absorption of low energy photons is almost excusively due to the photoelectric effect (see fig 3.4).

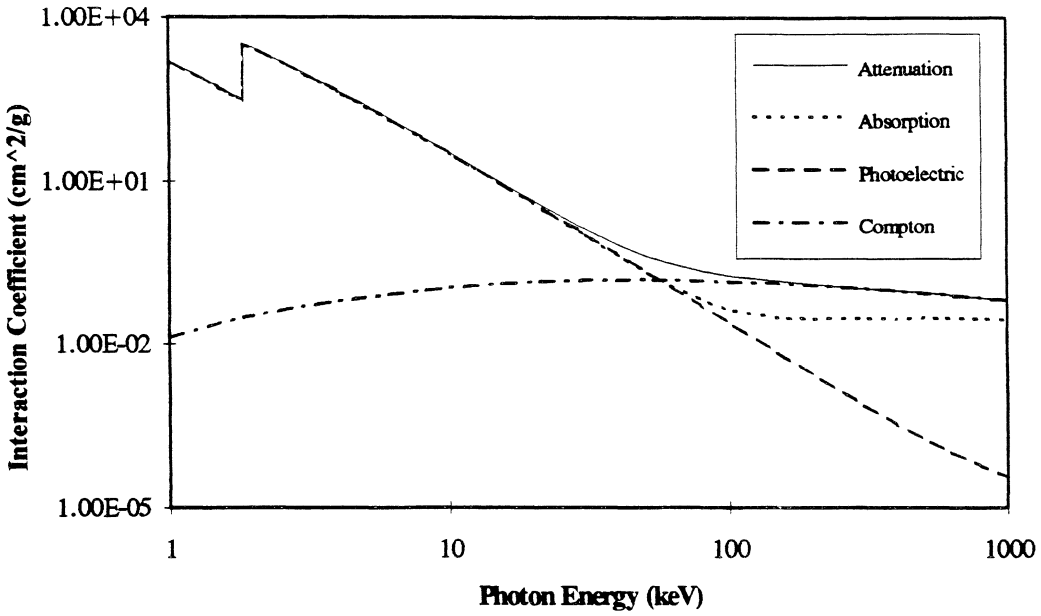


Fig 3.4. Interaction coefficients for silicon, showing that for photons of less than 100keV, absorption is mostly due to the photoelectric effect, although compton scatter contributes to the attenuation

The photoelectric effect involves the absorption of all of the photon's energy in exciting a bound electron. The photoelectron so produced, has an energy equal to the difference between the photon energy and its own initial binding energy. The most likely origin of a photoelectron is the tightly bound K-shell [5], which for silicon has binding energy of 1.8keV. As the photon energies being considered are of greater than 20keV, the photoelectron will have an energy similar to the original photon. This electron is able to travel a short distance (upto about 5μm for a 30keV electron in silicon [6]) through the material, and to collide with other bound electrons so generating many electron hole pairs. Because the photoelectrons have a short range all of the charge generated by one photon is concentrated in a tight ball (see fig 3.5). By comparison, high energy gammas tend to deposit energy by Compton scattering of electrons. These electrons themselves are then likely to be of high energy and so can travel long distances through silicon (around 80 microns for 100keV electron, rising to 2mm for a 1MeV electron) generating charge as they go.

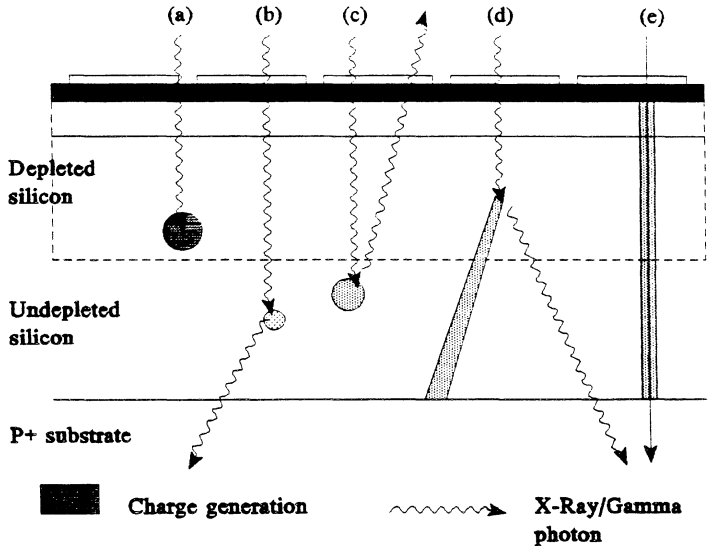


Fig 3.5 shows some possible interactions in the silicon. a) Low energy x-ray photon is absorbed by photoelectric effect and gives up all of its energy. b) Low energy x-ray photon is scattered through a small angle. This yields little signal, but contributes to beam attenuation. c) Low energy x-ray photon is scattered through a large angle, thus yielding a significant signal. d) High energy gamma is only likely to be scattered through small angles but can still give considerable energy to a knock-on electron. This pimary electron itself then travels through the material colliding with, and giving energy to secondary "delta" electrons which in turn undergo collisions. In addition to these collisions the primary knock-on electron gives off x-ray radiation as it decelerates (Bremsstrahlung) e) A minimum ionising electron of between 1 and 2MeV shows less energy loss, and consequently less charge generation than the lower energy knock-on electron.

Some Compton scattering also occurs at energies in the 20-70keV range, but this contributes significantly only to the linear attenuation by the CCD, and not to the energy absorption. Compton scattering becomes the dominant process for energy absorption at energies in excess of around 100keV, dependent upon the material.

3.3. Dosimetry

3.3.1. Units of Dose

The SI unit of dose is the Gray, which corresponds to an energy deposition of $1Jkg^{-1}$. The principal unit of dose employed in this work is the krad which is equal to 10 Grays. All exposures referred to in this work are dose (Si) unless otherwise stated.

3.3.2. Dosimeters

The irradiations carried out for this work were made with a radiography x-ray source emitting a 70kV pk spectrum. The output from this unit tends to fluctuate with time, so controlled dosimetry requires that the dose rate received by the devices be monitored during irradiation to allow adjustment of the driving current when necessary, and that the accumulated dose be measured so as to record any unseen fluctuations. For ongoing dose rate measurement a PIN diode is situated adjacent to the device during irradiation and the induced photocurrent noted. As an additional safeguard the photocurrent in the actual device is also noted and crosschecked against the PIN diode current. As a record of the accumulated dose seen by the device a RadFET dosimeter [7,8] is used (see fig 3.6).

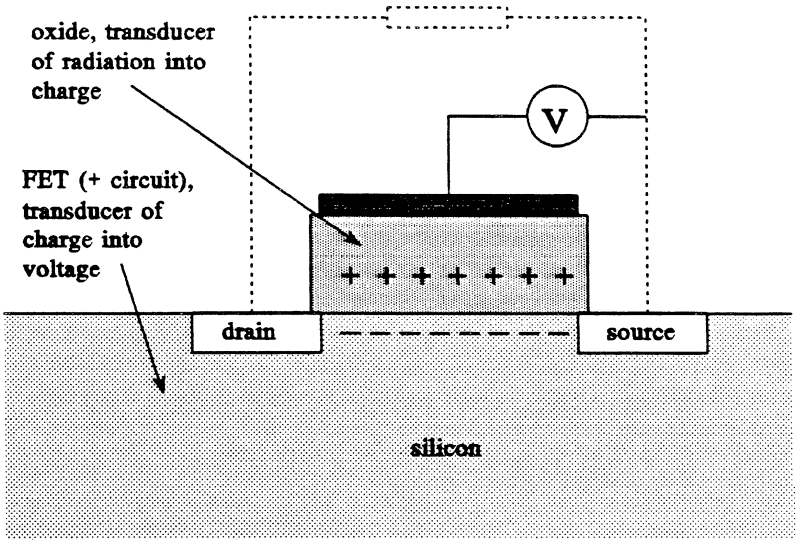


Fig 3.6. The principle of operation of the RadFET chip.

The RadFET has previously only been calibrated for gammas, so it was necessary to recalibrate against the PIN diode. The RadFET voltage shifts are therefore calibrated in terms of dose as defined by the PIN diode (see section 3.3.2.1).

The PIN diode and the RadFET were the principal dosimeters, and were in position for all the irradiations described in this work. However as the devices are used for medical applications it was thought prudent also to check the dose tissue corresponding to these exposures. To this end a series of irradiations was carried out relating the dose seen by LiF thermoluminescent devices to those seen by the silicon based dosimeters [9]. Whilst the dose seen by LiF does depart slightly from that seen by tissue at low energies, it gives a good indication of dose tissue (fig 3.7).

The calibration of these dosimeters was verified by comparison with a Farmer ionisation chamber loaned by the CRC Gray Laboratory. The ionisation chamber itself is calibrated annually and provided a standard.

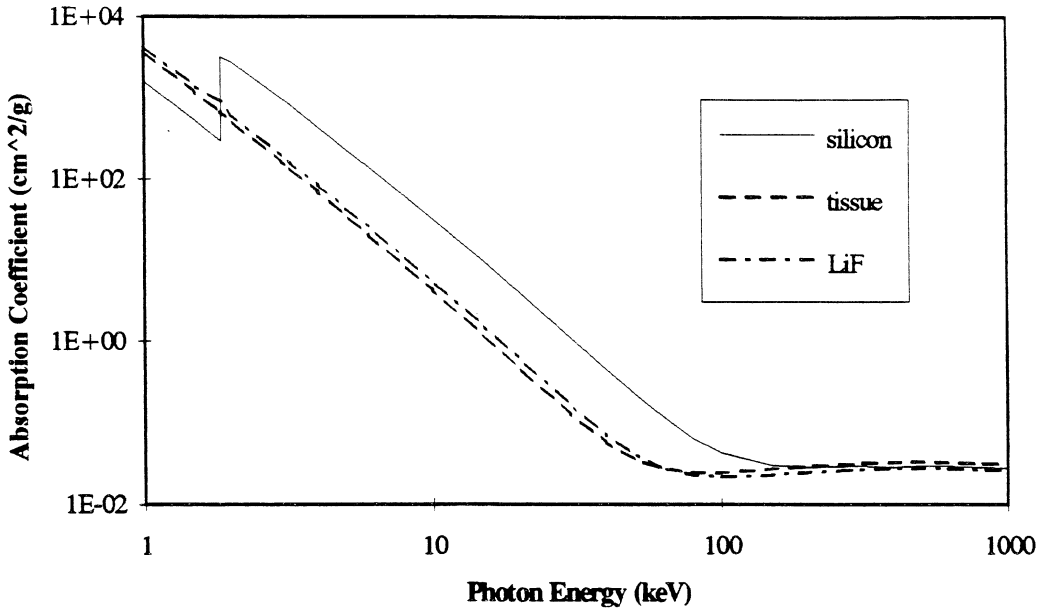


Fig 3. 7 Mass Energy absorption coefficient with photon energy for important materials.

3.3.2.1. Dosimeter Calibration.

Two PIN diodes were used during the course of these measurements, the Hamamatsu S1723-03 and the Hamamatsu S3590-03. Both devices have an active area of $1cm^2$ but the S1723-03 has a depetion region thickness of 150μm, whilst the newer S3590-03 has a depletion region thickness of 210μm. Assuming that 3.6eV is absorbed for every electron-hole pair produced, then the dose rate in krad per hour is given by;

$$\frac{dD}{dT} = 5.6 \times \frac{I_{ph}(nA)}{d(\mu m)A(cm^2)}$$

where I_{ph} is the photocurrent induced by the radiation, d is the thickness of the depletion region, and A is the active area of the PIN diode.

The RadFET was calibrated against the dose measured by PIN diode. There are four FET structures on each RadFET chip, two with thick gate oxide (0.85μm) and two with thin gate oxide (0.25μm).

The thick oxide structures show a greater voltage shift than the thin oxide structures, and so are more sensitive if doses of 10krad or less are being measured (see fig 3.8), but the thin oxide structures are able to record higher doses before saturation occurs (see fig 3.9).

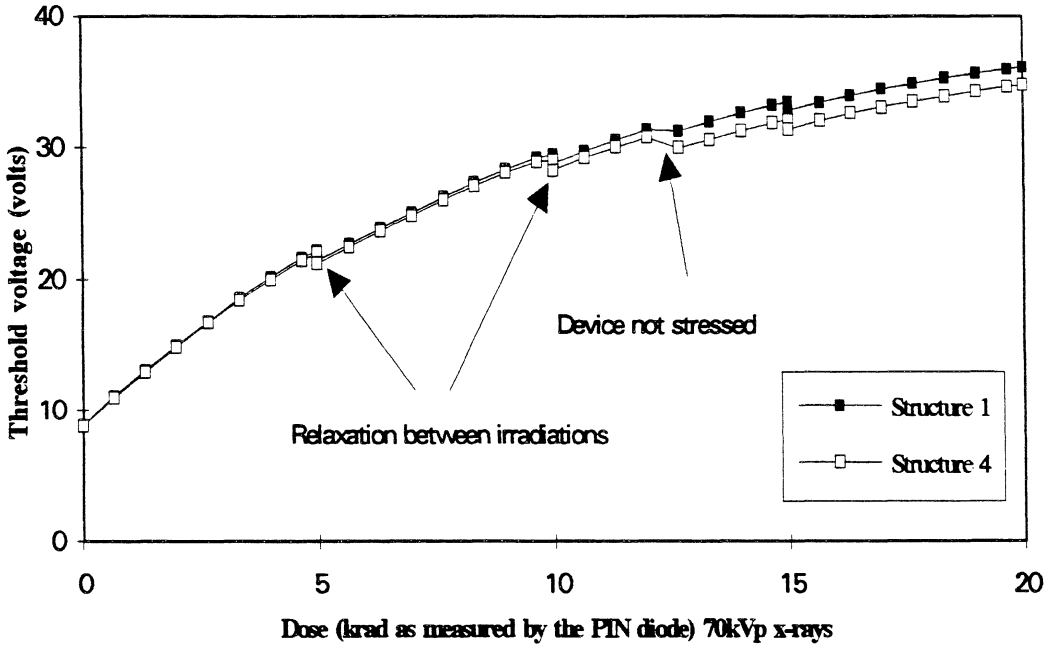


Fig 3.8. The response of the thick oxide (85μm) RadFET gates to 70kVp X-rays. Each data point indicates an irradiation step. The small discontinuities after 5krad, 10krad and 15krad, followed gaps of several days between irradiations, and indicate a slight relaxation in voltage shift. The drop after 12krad was caused by failure to stress the gates with the cirrect bias for this irradiaton step.

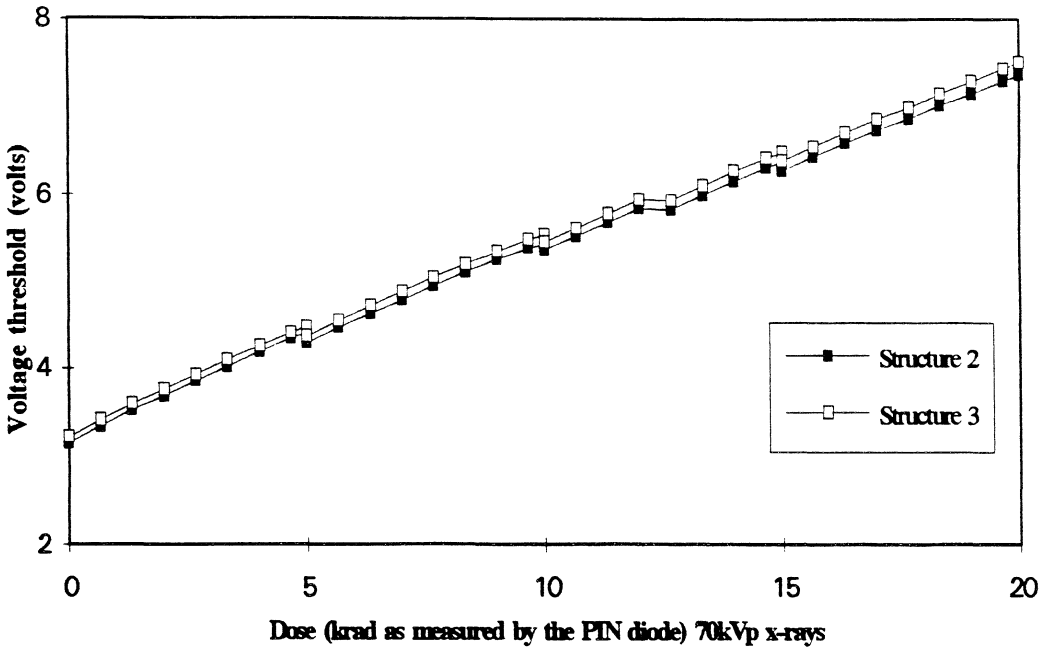


Fig 3.9. The response the thin oxide (25μm) RadFETgates to 70kVp x-rays. Each data point indicates an irradiation step. The discontinuities are explained as for fig 3.8.

3.3.3. Other Dosimetry Considerations

Relating the dose seen by the dosimeter to that seen by the device is not straightforward for x-ray irradiation, especially with a multilayered structure like the CCD. For gamma sources such as Co^{60} emitting photons of around 1 MeV the energy absorption coefficients for each of the different layers are similar. This means that provided appropriate buildup material (typically 2mm of aluminium is sufficient for 1MeV gammas [6]) is used to ensure a uniform flux of knock-on electrons and back scattered photons, with depth, the dose profile will approximate to that of equilibrium (see appendix 1.pVII). However for x-rays of less than 100keV or so, the absorption coefficient is heavily dependent upon both the energy of the photon and the composition of the layer (see fig 3.7). If the layers were very thick with respect to the range of the photoelectrons generated, then the dose in each layer would still approximate to the equilibrium value, and could be calculated from the known

absorption coefficients. Fig 3.10 shows the 70kVp spectrum multiplied by the absorption coefficient function for Si and SiO_2, it can be seen that most of the absorption is of photons in the range 20-40keV.

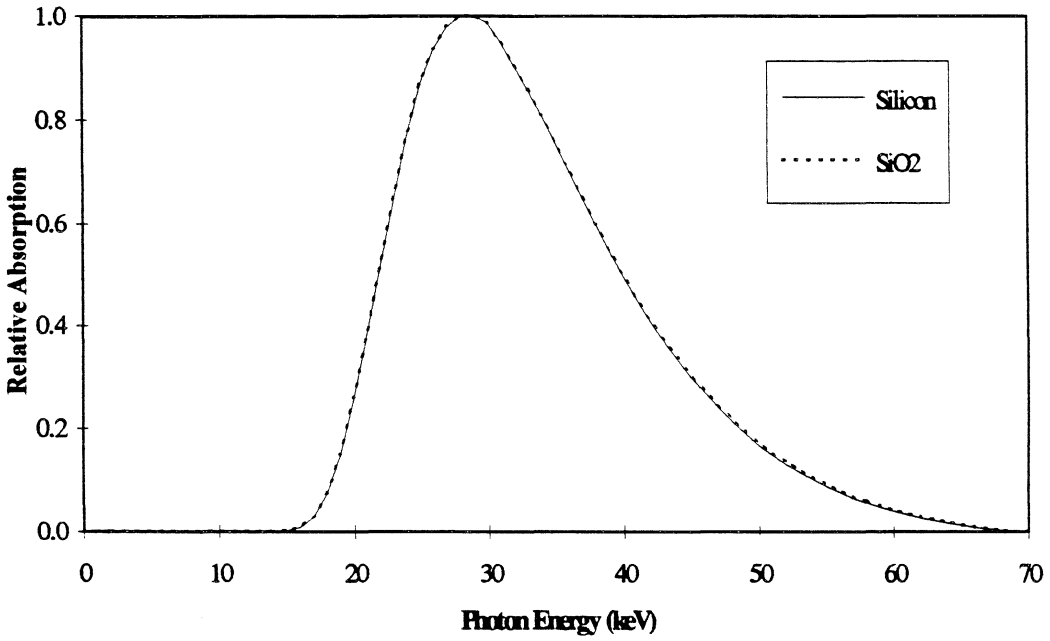


Fig 3.10. This plot is derived by multiplying the hardened 70kV x-ray spectrum by the energy absorption coefficients for silicon and SiO_2, and shows the relative number of photons of each energy which are absorbed in the two layers.

As mentioned in 3.2, the range of electrons of this energy is approximately 5 microns, whereas the thinnest layers, the gate oxide and the gate nitride, are 85nm in depth. As a result of this, the dose profile in these layers does not approach the equilibrium value even towards the middle of the layer, but is determined by the transport of electrons from neighbouring layers. Whilst the epitaxial silicon at 20 microns in depth is thick enough to ensure that equilibrium dose is reached in regions well away from the oxide interface, the dose seen by the few microns of silicon closest to the oxide would be expected to see a modulated dose profile. In order to predict the likely dose profile through the CCD it is necessary to use PHOTCOEF simulations.

3.3.4. PHOTCOEF [10]

3.3.4.1 About PHOTCOEF

This package has a data base containing the photon interaction coefficients for all elements, and is able to calculate the coefficients of complex mixtures and compounds. The dose deposition calculation includes the use of semi-empirical algorithms to account for electron transport across interfaces between dissimilar substances. For mono-energetic radiation the operation need only be carried out on a "one-bin" energy spectrum and so could be completed in a few seconds, depending upon the structural complexity of the device to be irradiated, and the speed of the computer.This software is designed for use by IBM compatible 286 or better. If the operation were to be carried out on every energy bin of a radiation spectrum, the run times would be much longer. Because of this PHOTCOEF uses an approach whereby the equilibrium dose is calculated precisely for each energy bin in the spectrum, but for the purpose of determining electron transport between layers, an individual "effective" photon energy is chosen, such that it is representative of those actually absorbed. Assuming the photons absorbed to be of this "effective energy" the generation of electrons by all possible interactions is calculated [10]. The operator should be aware of the limitations likely to be caused by such an approximation. As far as x-ray simulations are concerned, it is important that individual layers in a model are thin enough that the photons absorbed in any given layer fall into a narrow range of energies, and so can accurately be represented by one "effective energy". Sometimes this will necessitate the representation of a thick layer by several thin layers in the simulation model.

3.3.4.2 CCD Dose Profile Simulation with PHOTCOEF

Dose deposition profiles were obtained for 70kVp irradiations of the following structures; (fig 3.11)

1) EEV's conventional CCD architecture
2) EEV"s CsI(Tl) coated CCD
3) EEV's $Gd_2O_2S(Eu)$ coated CCD

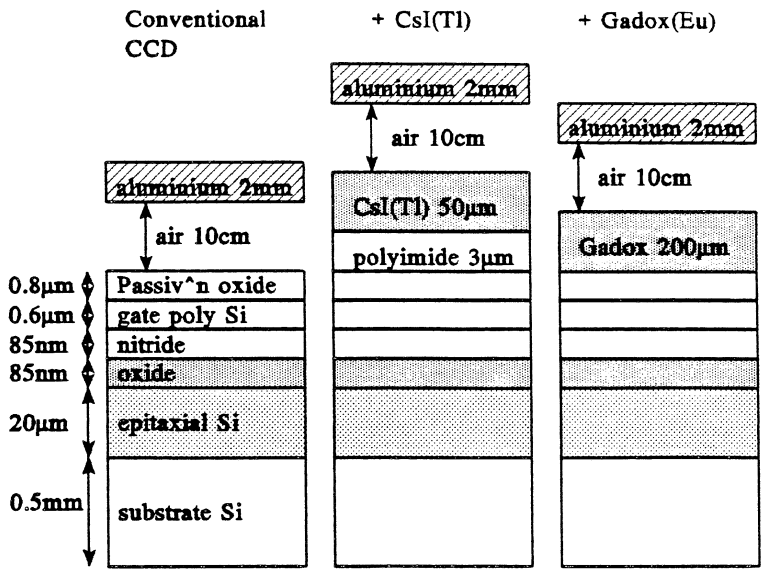


Fig 3.11. CCD models used for PHOTCOEF dose deposition profiles.

As an aluminium filter was used to harden the spectrum throughout these irradiations, this was incorporated into the models. Further dose deposition profiles were also obtained for irradiation of the conventional CCD by 70kVp x-rays and 1.25MeV gammas, to allow comparison between the "equilibrium" and "actual" dose values predicted for the respective radiation types. These are shown in appendix 1.

Fig 3.12 shows the relative dose depositions through the conventional CCD structure after irradiation by an arbitary fluence of 70kVp x-rays. Layer 6 is the gate oxide, which can be viewed in the expanded plot shown in fig 3.12.b, and layer 7 is the epitaxial silicon layer. The dose profile is not similar to the equilibrium dose in either layer (see appendix 1) . The dose throughout the 85nm oxide layer is enhanced by electron transport from the denser silicon layer. The silicon layer itself has a region of low dose extending about 5μm from the oxide interface, although beyond this point the dose reaches the equilibrium value.. The region of low dose in the silicon is caused by electron loss into the other layers, and also into the air, and will lower the average dose of the epitaxial layer by a few percent. No corresponding effect is seen at the back surface of the epitaxial layer, as it is in equilibrium with the substrate. Similarly derived plots for the CsI(Tl) and Gd_2O_2S(Eu) coated devices are shown in appendix 1.

During actual irradiations the separation between the filter and the device was varied between 10

Fig 3.12.a Irradiation by 70kVp x-rays. Relative dose through epitaxial silicon (layer 7) of conventional device.

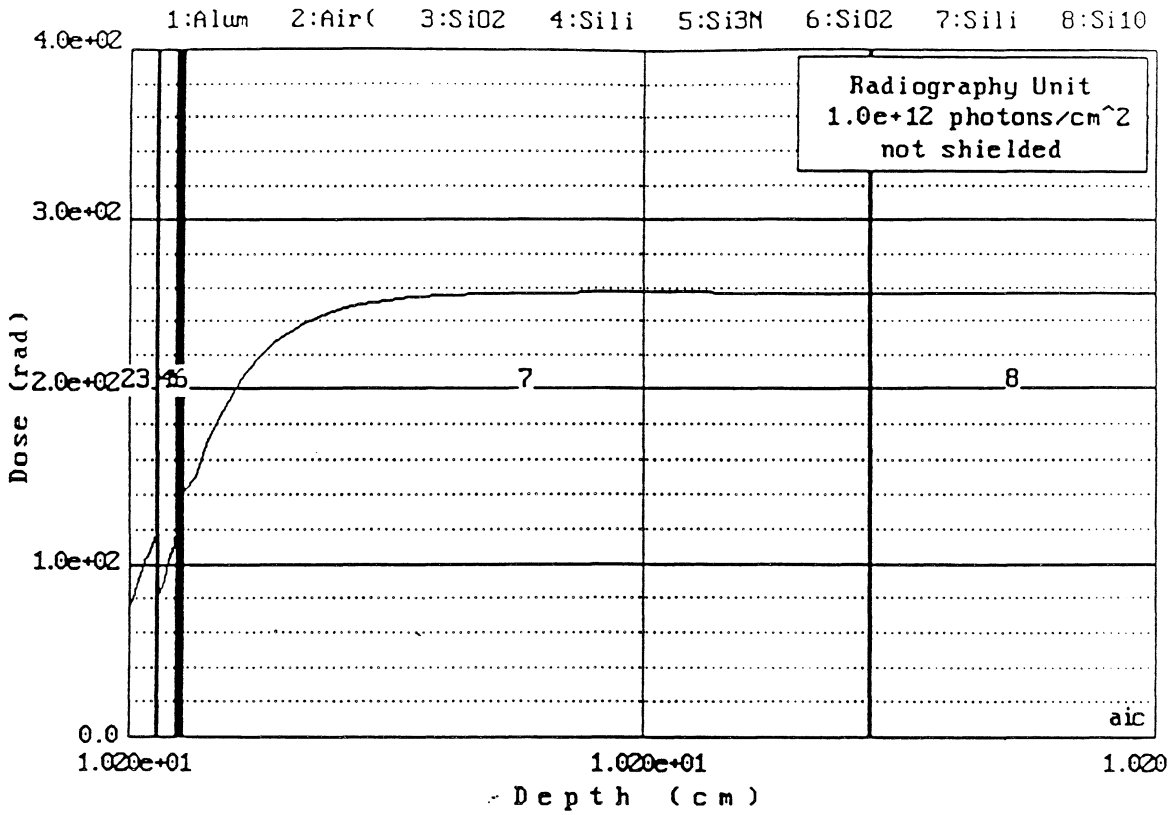
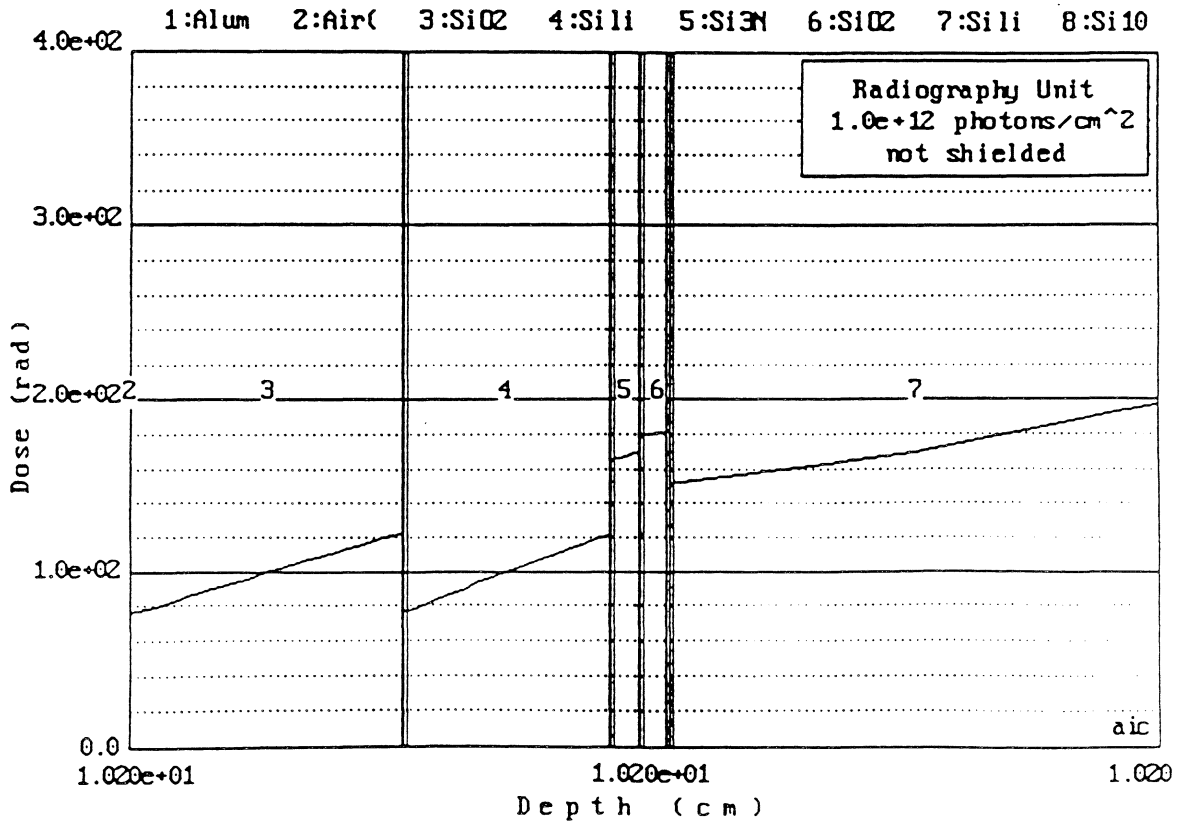


Fig 3.12.b Expanded plot of above showing gate nitride (layer 5), gate oxide (layer 6), and epitaxial silicon (layer 7)



and 30cm depending upon the dose rate being employed. Simulations were carried out using a range of separations but it was found that any separation of above 1cm resulted in effectively no dose enhancement (fig 3.13).

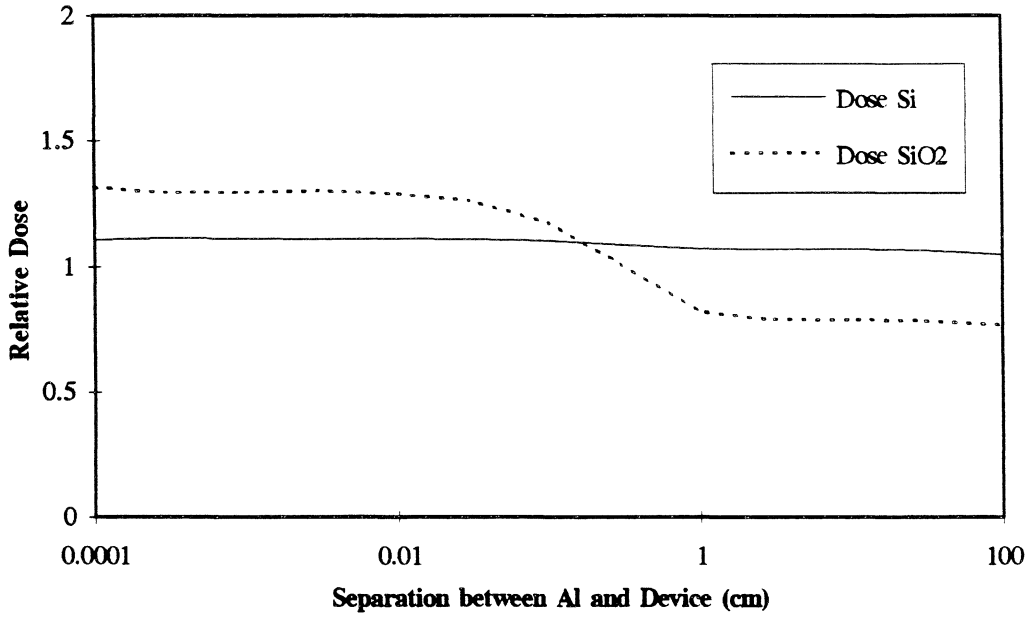


Fig 3.13. shows the relationship between gate oxide dose and the proximity of the aluminium filter.

3.3.5. Relating the Dose seen by the Gate oxide and Epitaxial Silicon of the CCD, to that seen by the PIN Diode

3.3.5.1. Discussion

As shown in appendix 1, the different CCD layers and the PIN diode see approximately the same dose during irradiation by high energy gammas. In order to express the dose of an x-ray irradiation though, it is necessary to define the device or layer concerned. Although the equilibrium dose in the PIN diode is similar to that in the epitaxial layer of the CCD, electron transport between

neighbouring layers causes different effects in the two structures. The PIN diode active depth is much greater than the active depth of the CCD silicon, so there is virtually no reduction in the average dose in the PIN diode resulting from electron transport at the Si/SiO_2 interface, whilst the average dose in the CCD is reduced by a few percent. Also some dose enhancement occurs in the PIN diode as a result of electron transport from the silver electrode layer at the opposite silicon interface. No such enhancement occurs in the CCD, because the 0.5mm silicon substrate shields the epitaxial layer from any electrons which are transported from the substrate electrode. Taking these factors into account, the PHOTCOEF simulation implies that a dose of 1kRad in the PIN diode indicates a dose of approximately 0.91kRad in the CCD epitaxial layer.

The dose profile simulations shown in fig 3.12, imply that the dose seen by the oxide will be about 74% of that seen by the epitaxial silicon layer, and therefore 67% of that measured by the PIN diode, for the irradiations carried out on the conventional architecture devices. However the dose seen by the oxide is very much dependent upon the device environment during irradiation. Fig 3.13. shows the modelled dose, in the oxide, as a function of proximity of the aluminium filter. Many plastics and glasses are of similar density to aluminium, so this gives an indication of the possible dose enhancement that may occur if the device is effectively "builtup" by its encapsulation or housing during exposure. It can be seen that the oxide dose could be as great as 10 percent above the silicon dose. It is therefore necessary either to eliminate this possibility by design, or to make appropriate allowance in any lifetime guarantee. For the irradiations described here 1krad dose in the PIN diode indicates a dose of 0.67krad in the gate oxide. All doses mentioned in this work refer to dose seen by a PIN diode.

3.3.5.2 Summary of PHOTCOEF Predicted Dose Depositions.

The predicted average dose (relative to PIN diode dose), for each layer of the CCDs, both conventional and scintillator coated, is shown in fig 3.14. The PHOTCOEF dose profile simulations corresponding to these results are shown in appendix 1.

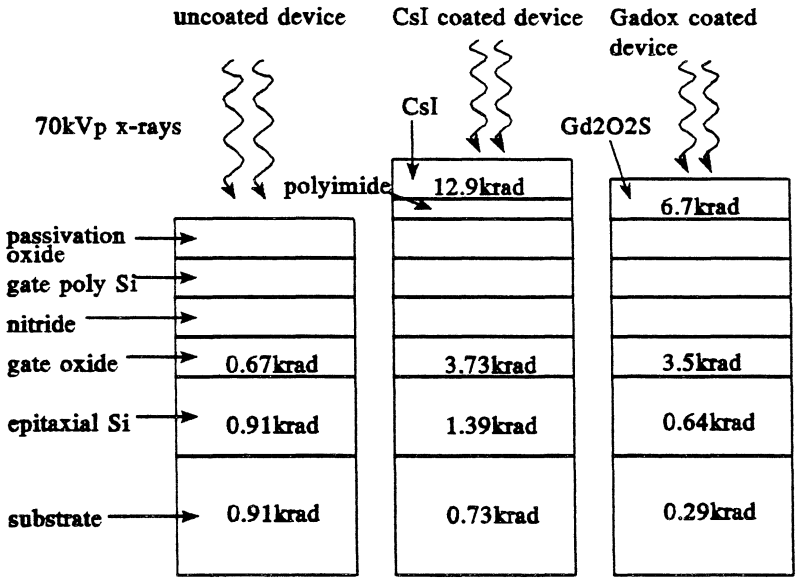


Fig 3.14. This figure shows the average dose deposition predicted by PHOTCOEF for relevant layers of the three CCD structures, after an irradiation corresponding to a dose of 1krad in the PIN diode.

References for Chapter 3

[1] M.S. Robbins, "Radiation Damage Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, 1992.

[2] T. Roy, "Ionising Radiation Induced Surface Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, 1993.

[3] Birch, Marshall, and Ardran, "Catalogue of Spectral Data for Diagnostic X-rays", The Hospital Physicists Association, Scientific Report Series 30, 1979.

[4] T.P. Ma, and P.V. Dressendorfer, "Ionizing Radiation Effects in MOS Devices and Circuits", Published by John Wiley and Sons, 1989.

[5] G.F. Knoll, "Radiation Detection and Measurement", Published by John Wiley and Sons, 1989.

[6] A.H. Siedle, and L. Adams, "Handbook of Radiation Effects", Published by Oxford University Press, 1993.

[7] A. Holmes-Siedle, "The Space Charge Dosimeter - General Principles of a New Method of Radiation Detection", Nucl. Inst. Meth., Vol 121, 169-179, 1974.

[8] A. Holmes-Siedle, and L. Adams, "Dosimetric Silica Films: The Influence of Fields on the Capture of Positive Charge", IEEE Trans. Nucl. Sci., NS-29, 6, 1975-1979, 1982.

[9] Raj Mundra, MSc Thesis, Brunel University, 1993.

[10] PHOTCOEF, AIC Software, PO Bx 544, Grafton, Mass 01519, USA.

Experimental Details

4.1. Operation of the CCDs

4.1.1. Drive Electronics

The drive electronics used during this work originated from the prototype electronics designed for the NA32 experiment at CERN [1]. A block diagram outlining the setup is shown in fig 4.1 [2].

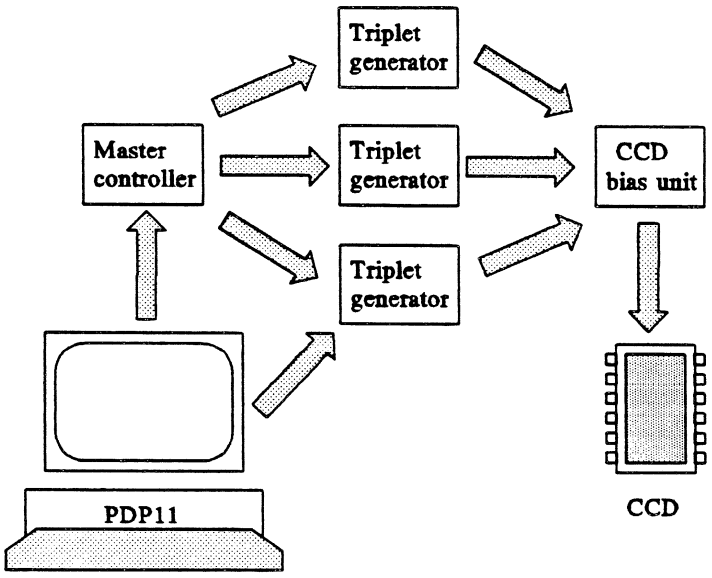


Fig 4.1. The CCD drive electronics.

The user loads the master controller with a file containing the chronological instructions for the triplet generators, from the PDP11 microcomputer. Four triplet generators are used, for the device image region, the storage region, the output register, and the reset pulse. On receiving the trigger from the master controller, a triplet generator supplies the bias unit with three pulses, one for each clocking phase. The bias unit also provides the necessary d.c. biases for device operation.

This system is capable of a readout rate of about 1MHz, but typically 83kHz is used for devices of

the size of the CCD02. For the larger CCD05 devices the readout rate was increased to 166kHz in order to prevent potential well saturation at room temperature.

4.1.2. Device Characterisation

For the purposes of this work it was not necessary to image the device, instead the device was clocked continually, with the output voltage levels monitored on an oscilloscope. Dark current was measured by the use of a high impedance voltmeter placed across a 10MΩ resistor in the reset drain line (see fig 1.11)

For static dark current measurement the standard procedure is to operate the device with all gates grounded, and all drains connected to the reset drain line (see fig 4.2). The output circuit is biased as for clocking, except that the reset transistor gate bias (ϕ_R) is held high (10V). The substrate bias

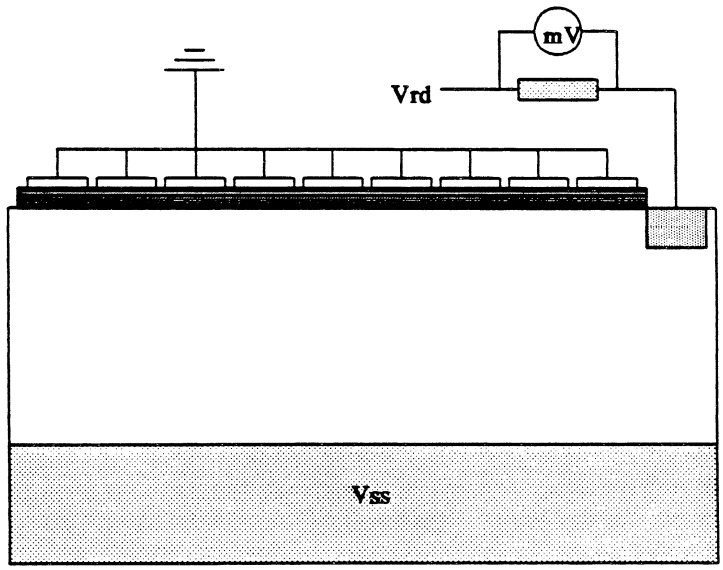


Fig 4.2. Schematic of the device set-up for measurement of static dark current

can then be varied, whilst the current collected by the reset drain is monitored. This set-up was ideal for dark current measurements made with a positive substrate bias, but does not lend itself to application of a negative substrate bias, as this is prohibited by the bias unit. For the measurement

described in section 5.1, the effect of negative substrate bias was simulated by application of a positive bias to the gates. This was done by inverting the signals from the triplet generators to the bias unit, so that in the "unclocked" condition they were high, and then varying the high gate bias. The substrate bias was then set to the lowest permissable value, such that the device saw a negative substrate to phase gate bias.

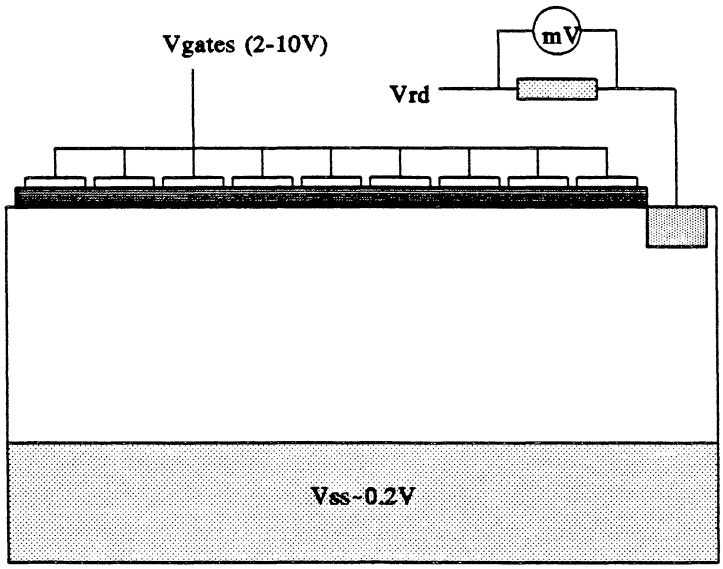


Fig 4.3. Schematic of the device set-up for measurement of static dark current with application of a negative substrate to phas gate bias.

Device temperature was controlled by positioning the device on a copper heatsink using heatsink compound to improve thermal contact. The device could be cooled by passing cold nitrogen gas through a steel tube welded to the heatsink, or heated by passing current through a wire wound resistor mounted on the heatsink. This apparatus was set-up in a vacuum cryostat to minimise temperature non-uniformities. The temperature was monitored using a T-type thermocouple screwed to the heatsink. The non-uniformity in temperature across the surface of a dummy device cooled to 20K below ambient, in this cryostat, was measured to be less than 0.1K.

4.2. Device Irradiation.

All irradiations were carried out using a Scanray radiography x-ray unit based in the Brunel University Physics Dept. This is a d.c. self rectifying source loaded with a tungsten target (see section 3.1 further discussion), and has an operating current range of 1-3mA, and an operating voltage range of 40-120kV. All the irradiations were done with the source driven at 70kV, and the beam filtered by 2mm of aluminium, in order to simulate the x-ray spectra used for dental purposes. The endpoint of the x-ray spectrum was verified using a silicon detector connected to an MCA. Whilst the spectrum itself was verified approximately by a testing the attenuation of the beam by different thicknesses of aluminium.

The set-up for irradiation of CCD05 devices is shown in fig 4.4. The two dosimeters were placed alongside the CCD in a ZIF (zero insertion force) socket. The set-up for irradiation of CCD02 devices only differed from this in the respect that each device was held in a separate socket, as the ZIF sockets were not yet available. The dosimetry is discussed in Chapter 3.

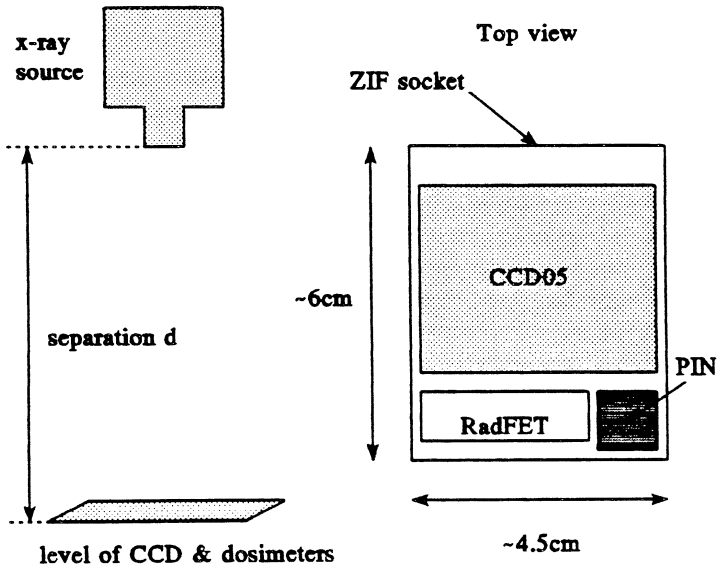


Fig 4.4. The set-up for irradiation of CCDs with 70kVp x-rays. The separation, d, was varied between 30cm (for greater uniformity) and 15cm (for greater dose rate).

Using this set-up it was possible to achieve a dose rate of 4krad per hour if the separation between the source and device was reduced to 15cm, although to improve unifomity of dose across the device most irradiations were carried out a separation of around 30cm, and a dose rate of 1krad per hour.

During irradiation a device was powered by use of a simple bias box comprising voltage dividing resistors (see fig 4.5). This enabled all the bias voltages to be obtained from one source, and allowed the dark/photocurrent to be monitored. The box also ensured that the device pins were protected against static damage independently of the power supply. A shorting D connector was used if a device was to be irradiated unpowered.

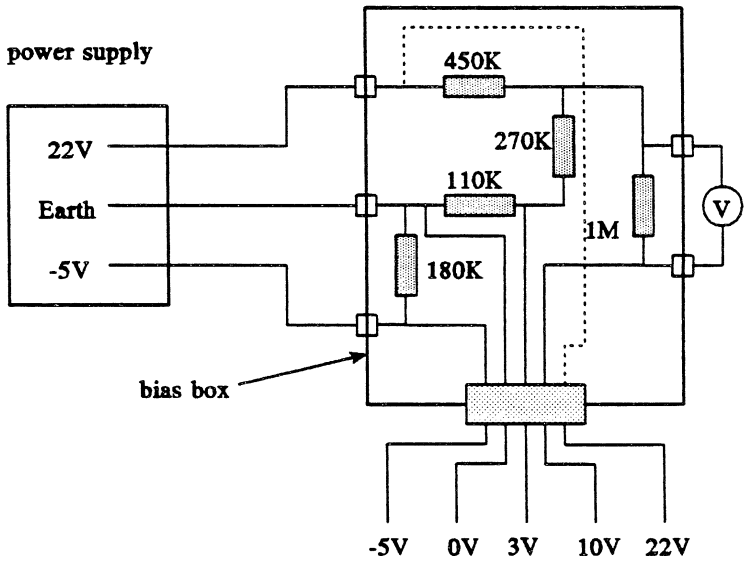


Fig 4.5. The arrangement for biasing devices during irradiation. The device pins were connected as follows; output drain 22V, antiblooming and reset drains 10V, substrate 0V, antiblooming and output gates -5V, all other gates 3V.

4.3. Device Annealing.

Devices were annealed at three temperatures for this work, 373K, 388K, and 408K. An environmental chamber was used to perform the 373K anneals, but for higher temperatures a copper hotplate, heated by wirewound resistors, was used. The hotplate was machined to allow the device

pins to pass through it, and ZIF sockets were positioned appropriately on the reverse side. The device pins were then shorted via the ZIF sockets. The temperature of the hotplate was regulated by an Omega CN 76000 temperature controller. The environmental chamber is accurate to approximately ±0.5K, the hotplate was measured to be accurate to approximately ±1.5K.

Powered anneals were only carried out at 373K, in the environmental chamber. For this purpose an anneal box, compatible with the bias box described in section 4.2, was made. The conventional biasing connections were as for the irradiations, whilst the positive oxide bias was contrived by connecting the gates to 10V, and all other connections to 0V.

References for Chapter 4.

[1] R. Bailey et al., "First Measurement of Efficiency and Precision of CCD Detectors for High Energy Physics", Nucl. Inst. Meth., A213, 201-215, 1983.

[2] M.S. Robbins, "Radiation Damage Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1992.

Biasing Implications in the CCD

5.1 Bias Dependence of the CCD

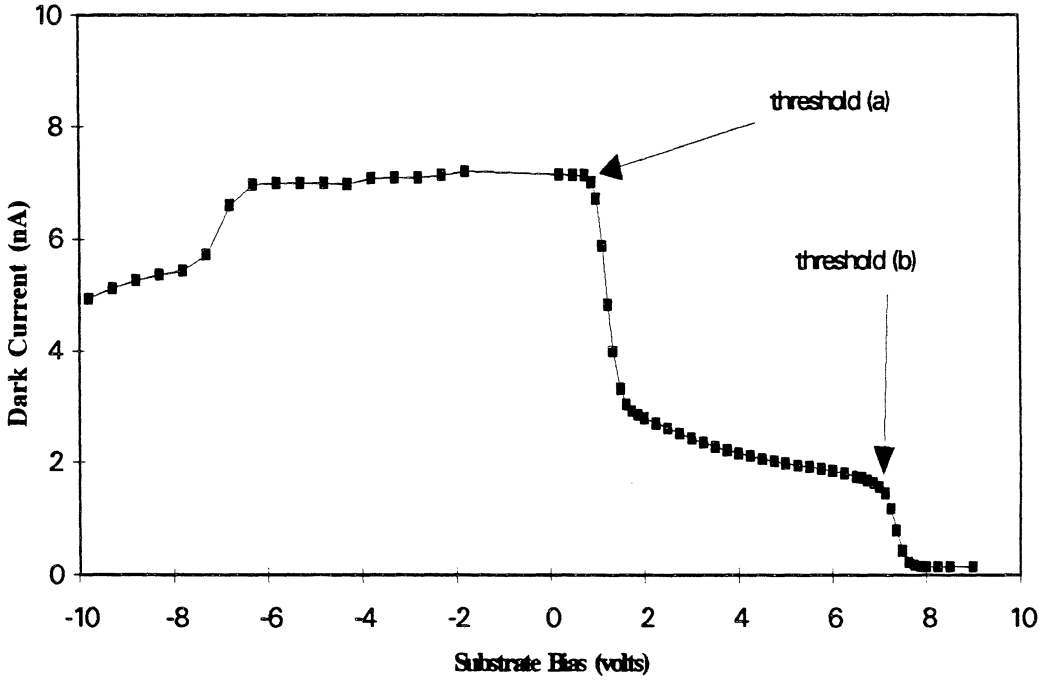


Fig 5.1 Dependence of static dark current upon substrate bias. These data were obtained for a CCD05 device at 275K

The principal bias parameters of the CCD are the gate bias V_G, and the substrate bias V_{SS}. As long as the reset drain voltage V_{rd}, is sufficiently high to maintain the "punch through" condition as described in section 1.1.4, the electrical condition of the buried channel structure is determined by V_G and V_{SS}, or more specifically the difference between them. For a device in static mode with V_G = 0V, it is therefore necessary only to consider the substrate bias. Fig 5.1 shows the dependence of static dark current upon substrate bias for a CCD05 device. For practical reasons the substrate bias was not actually taken to negative values, but the condition was simulated by holding all the gates at positive biases. (This is equivalent to applying a negative substrate bias in all respects other than that referred to in sect 5.2.2.2.). There are at least four clearly distinguishable domains, excluding transient regions. Roy [1] has demonstrated that the threshold "a" marks the substrate bias at which

the p-stop surface becomes accumulated with holes, so suppressing dark current generation from the p-stop surface, whilst threshold "b" marks the substrate bias at which holes are injected from the p-stop surface into the n-channel, so suppressing current generation at this surface. It was also suggested that if V_{ss} was reduced below threshold "a" to negative values, then an inversion layer would form at the p-stop surface suppressing current generation once more.(see section 2.3.2) However, from fig 5.1 it can be seen that this inversion effect does not occur, although at high negative values of substrate bias the dark current does reduce. The purpose of this chapter is to put forward an explanation of the detail of the V_{ss} versus I_d curve, including in particular, the gradual rise in dark current between thresholds "a" and "b", and the shape of the curve for negative values of V_{ss}.

5.2 Explanation of dark Current Dependence upon V_{ss}

5.2.1. Positive Substrate Bias

The physics of the CCD as a function of substrate bias is understood by reference to the structure shown in fig 5.2.

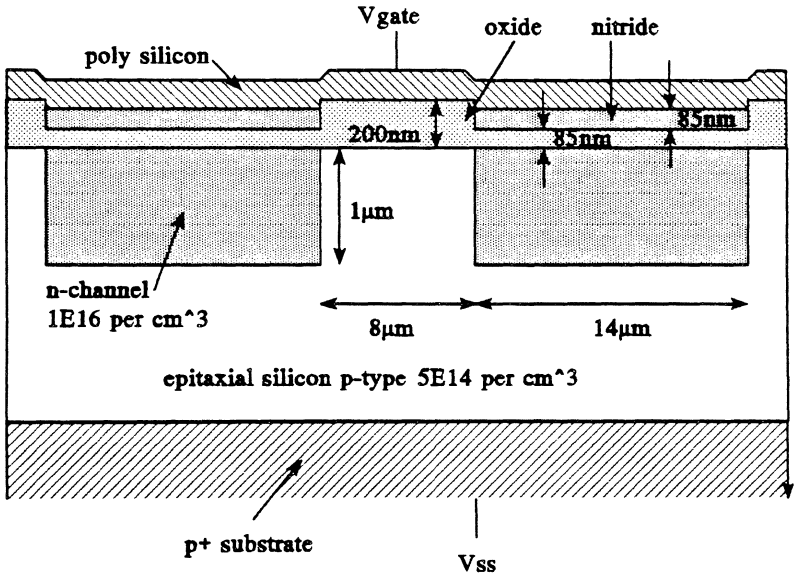


Fig 5.2 The structure of the CCD05, showing the MNOS capactitor formed by the gate over the n-channel, the MOS capacitor formed by the gate over the p-stop and the p-n junction between the n-channel and the p-stop.

The electrical environment in the device silicon is a function of the effective gate bias,V_G(eff), the substrate bias, and the inter-related conditions of the MIS capacitors and the p-n junction. V_G(eff) takes account of the difference in work function between the gate and the silicon, and also any trapped charge in the gate oxide. It is understood that at biases in excess of threshold "b" all Si/SiO_2 surfaces are undepleted, and that at substrate biases below threshold "a" all Si/SiO_2 surfaces are depleted. Consequently, in these regions dark current is independent of substrate bias, and is determined as described in section 2.3.2. However in the intermediate region it is clear that the dark current is slightly dependent upon bias, suggesting that the p-stop surfaces become at least partly depleted.

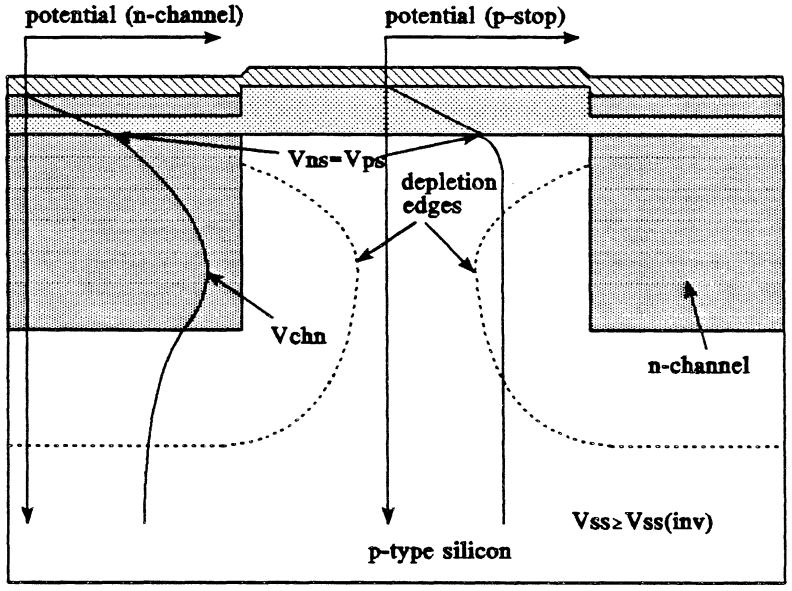


Fig 5.3. The electrical condition of the CCD for n-channel surface inversion.

Fig 5.3 shows the electrical condition of the device for substrate biases above threshold "b" (see fig 5.1). The potential at the p-stop surface, V_{ps}, is equal to the potential at the n-channel surface, V_{ns} with the device in this state. Provided V_{SS} remains above threshold "b" any change in bias results in a transfer of holes between the surfaces, such that equality of potential is maintained. The potential barrier at the p-stop surface, ψ_B, as a function of V_{SS}-V_G(eff) [3 p26], and the potential profile into the p-stop for the case where V_{SS}-V_G(eff) = 5V [4 p58], were determined numerically, and are shown in figures 5.4 and 5.5 respectively. (see appendix 2)

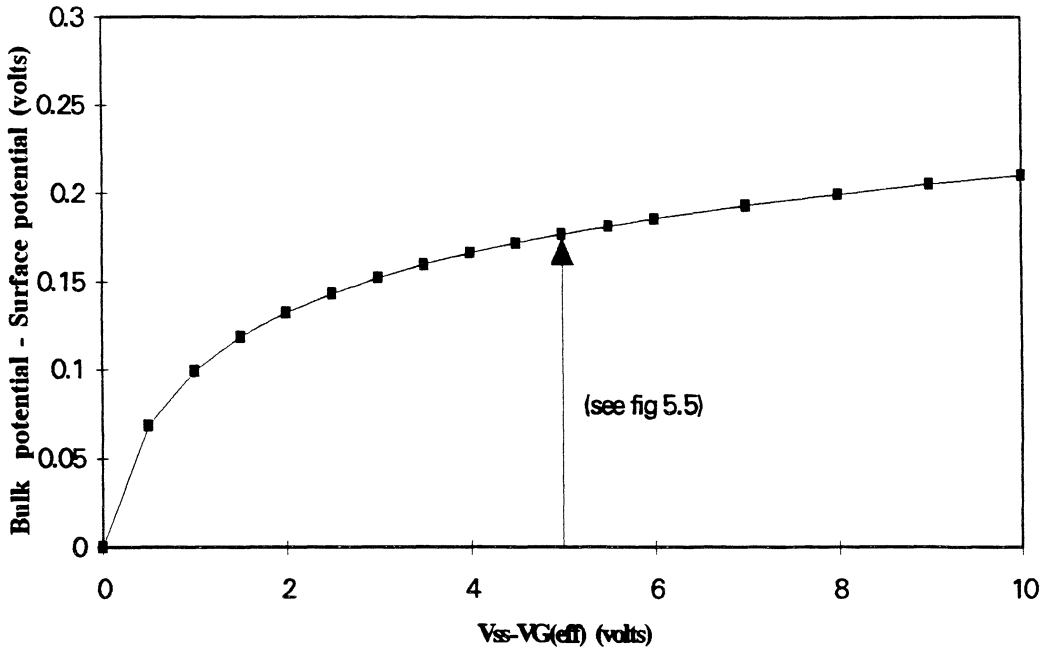


Fig 5.4 The potential barrier at the p-stop surface as a function of substrate bias

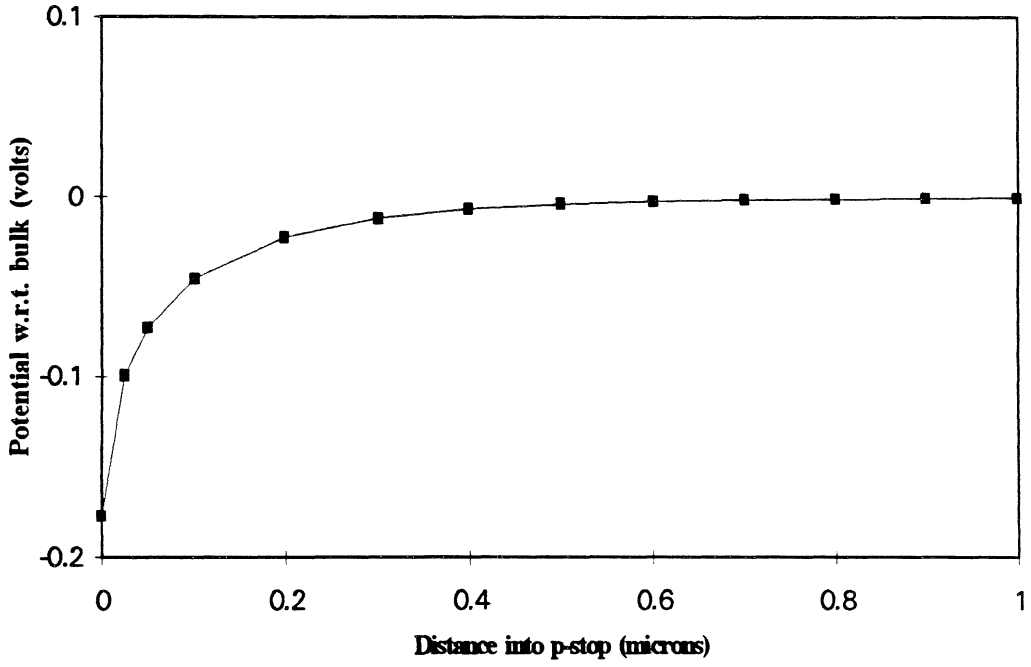


Fig 5.5. The potential profile through the p-stop region as a result of a substrate bias of 5V with respect to V_G(eff).

From fig 5.4 and 5.5 it can be seen that V_{PS} approximates to V_{SS}-0.2V, for the region of interest, and that the potential barrier extends about 0.3μm into the p-stop.

On reducing V_{SS} to threshold "b" a change takes place in the condition of the device. V_{ps} falls below the value of V_{ns} for a depleted n-channel surface, and any holes in the n-channel are swept into the p-stop, with the result that the n-channel surface starts to generate dark current. At this point V_{ps} is almost equal to V_{ns}, so although the n-channel surface is depleted there is no effective reverse bias of the p-n junction to induce a depletion region at the p-stop surface. As V_{SS} is further reduced however V_{ns} remains almost constant, whilst V_{ps} follows V_{SS}, (neglecting the change in p-stop surface barrier) therefore a **reverse bias** is applied at the p-n junction. If we consider the potential at the n-channel surface only, then the magnitude of this reverse bias approximates as;

$$V_{RS} \approx V_{SS}(b) - V_{SS}$$

where V_{RS} is the reverse bias, and $V_{SS}(b)$ is the substrate bias at threshold "b".

A depletion edge then extends into the p-stop at the surface so leading to current generation here. Unfortunately calculation of the extent of this depletion edge as a function of V_{SS} is non-trivial (see fig 5.6).

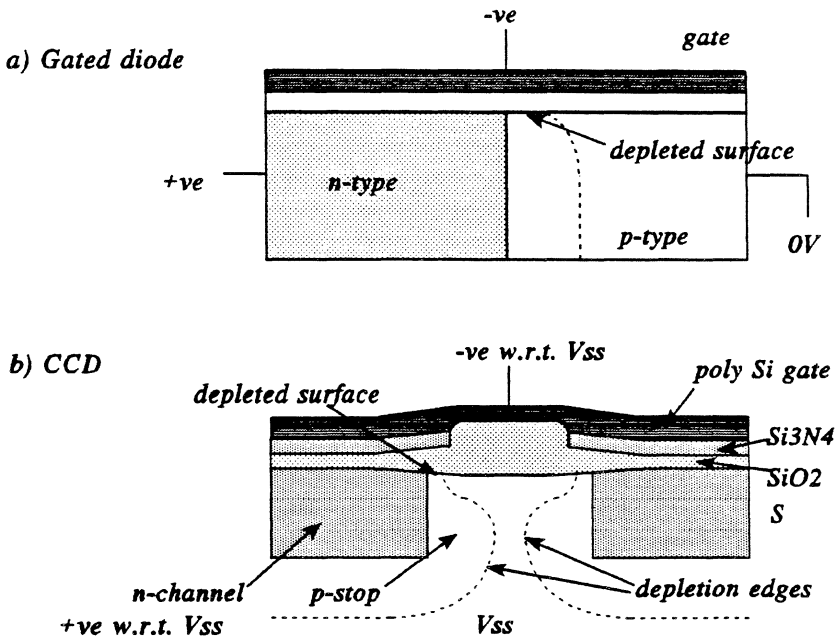


Fig 5.6. Reduction in depletion region caused by a gate bias in a) a gated diode, and b) a buried channel CCD.

Fig 5.6a shows qualitatively, the effect of a negative gate bias upon the depletion region extending into the p-type side of a reverse biased gated diode junction [4,5]. The effect is to reduce the depletion depth close to the oxide surface. Whereas the depletion depth elsewhere can be approximated by solution of Poissons equation in one dimension, here a three dimensional numerical solution of Poisson's equation would be necessary [5].

The situation is complicated further in the BCCD because of the dielectric system above the n-channel and p-stop. The dielectric is not a uniform layer, but is a double layer (85nm Si_3N_4, upon 85nm SiO_2) over the n-channels and a single layer (200nm SiO_2) over the p-stop. Because of this, the flat-band voltage above the p-stop region is likely to differ from that above the n-channels, both before, and especially after irradiation. General MOS irradiation theory (see section 2.2.2.1, and [6 p262]) suggests that for a conventionally powered CCD, the oxide layer above the p-stop will develop a smaller voltage shift than the double layer above the n-channel. More specifically Roy [1 fig 7.11] demonstrated that for conventionally powered CCD01 devices (similar technology to the CCD02 and CCD05), irradiated with betas from a Sr^{90} source the voltage shift above the p-stop

region (~40mV/krad) was approximately half of that above the n-channel (~80mV/krad). Thus when the substrate bias is adjusted following irradiation, in order to correct for the flat-band voltage shift above the n-channels, it will over-correct for the voltage shift above the p-stop.

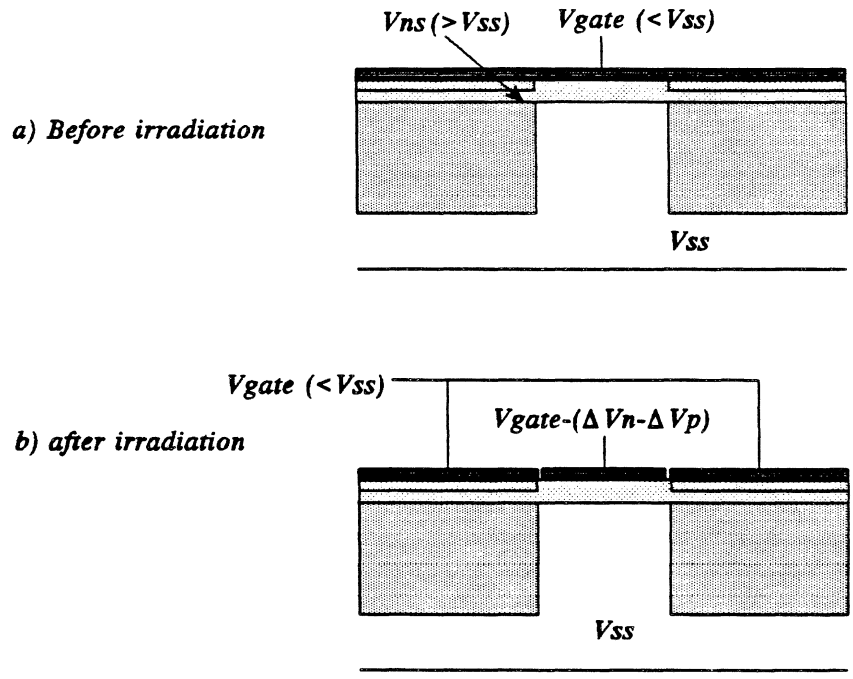


Fig 5.7. This shows the consequence of the difference in flat-band voltage shift above the n-channels and p-stops, for the case where the device is operated between thresholds "a" and "b", and correction has been made for ΔV_n. ΔV_n and ΔV_p are the voltage shifts above the n-channels and p-stops respectively.

This effective gate bias above the p-stop is therefore reduced relative to the effective gate bias above the n-channels, as shown in fig 5.7, and so will be expected to inhibit the depletion edge at the p-stop surface to a greater degree. The uncertainty in the nature of transition of the dielectric between regions, and in the diffused p-n junction, mean that it is not possible to predict quantitatively the effect that this difference in V_G(eff) will have. However experimental findings suggest that it is significant (see fig 5.8).

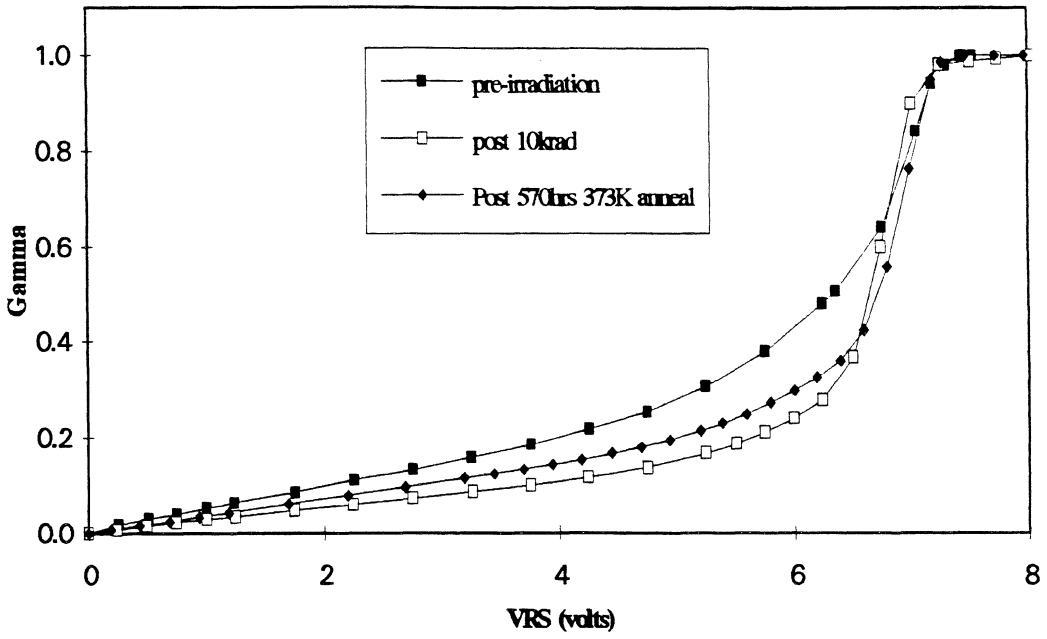


Fig 5.8. This shows γ as a function of V_{RS} (where V_{RS} is defined on page 87) for a CCD05 device before irradiation, after irradiation and then after prolonged anneal at 373K. This data was taken from device CCD05-1.

The fraction of p-stop surface falling within the depletion edges, γ, is shown in fig 5.8 as a function of V_{RS} for a CCD05 device. These values were calculated using equation 5.1, which assumes all dark current in excess of that at V_{SS}(b) to be caused by the depletion edges (see section 8.3.2.1 and esp. fig 8.11).

$$\gamma_{(V_{RS})} \approx \frac{I_{d(V_{RS})} - I_{d(b)}}{I_{d(a)} - I_{d(b)}} \qquad (5.1)$$

where $I_{d(a)}$ and $I_{d(b)}$ are the dark current levels at thresholds "a", and "b", respectively.

As can be seen from fig 5.8 it was found that γ, as a function of V_{RS}, did reduce following irradiation, and then increased by a smaller amount following the anneal. The 10krad irradiation corresponds to a voltage shift above the n-channels of approximately 450mV, and the anneal to a recovery of 80mV.

5.2.2. Negative Substrate Bias.

5.2.2.1. $-6V \leq V_{SS} < 0V$,

Roy [1] had suggested that reducing V_{SS} to negative values would induce an inversion layer at the p-stop surface, as is the case for a gated diode [4]. However it was found that in the range $-6V \leq V_{SS} < 2V$, dark current is reasonably independent of substrate bias.

Fig 5.7 [4 fig 10.3] shows the formation of an inversion layer at a p-type surface for the case of a gated diode structure. In the absence of an external bias, the potential barrier across the p-n junction is determined by the difference in Fermi level of the two types, or $\phi_{Fp} - \phi_{Fn}$. On application of a positive gate bias a depletion region will extend into the p-type region from the gate oxide surface, and a potential barrier ϕ_S, will be formed. If the gate bias is increased such that ϕ_S becomes greater than ϕ_{Fp}, the Fermi potential in the undepleted p-type, then an inversion layer begins to form at the surface. The surface is generally regarded to be in full inversion when $\phi_S = 2\phi_F$, and the concentration of electrons at the surface is equal to the concentration of holes in the undepleted bulk. In the event of a reverse bias, V_R applied to the p-n junction, the condition for onset of full p-type surface inversion becomes $\phi_S = 2\phi_F, +V_R$, such that the potential at the p-type surface is at approximately the same potential as the n-type bulk.

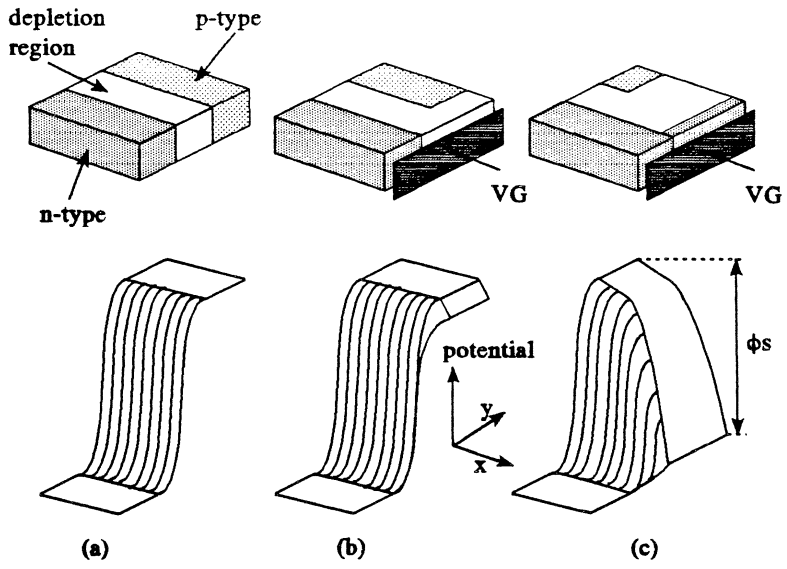


Fig 5.7. The effect of applying a gate bias over a p-n junction with $N_D \gg N_A$, showing a) the potential profile with no gate, b) The potential caused by a small positive bias, and c) the potential profile caused by a positive bias sufficient to induce an inversion layer at the surface of the p-type [4 fig 10.3].

A critical requirement for the formation of an inversion layer at the surface of the p-type silicon, (as shown in fig 5.7) is that the potential (for electrons) at the surface decreases relative to the potential at the surface of the n-type. If not, then the condition shown in fig 5.7.c, is unattainable, and the potential gradient existing between the p-type and n-type surfaces will ensure that electrons are swept away from the p-type surface. In the case of a gated diode as shown in fig 5.7, the larger doping concentration of the n-type, and the accumulation condition of the surface, determine that the potential barrier at the surface will be negligible compared to that in the p-type. Fig 5.8 shows the potential at both of these surfaces as a function of gate bias, as well as the the potential at the n-channel of a CCD. The potential in the accumulated n-type silicon was determined numerically by solution of Poissons equation, taking account of free carriers [3], whilst the potential in the depleted p-type silicon was calculated using the depletion approximation.

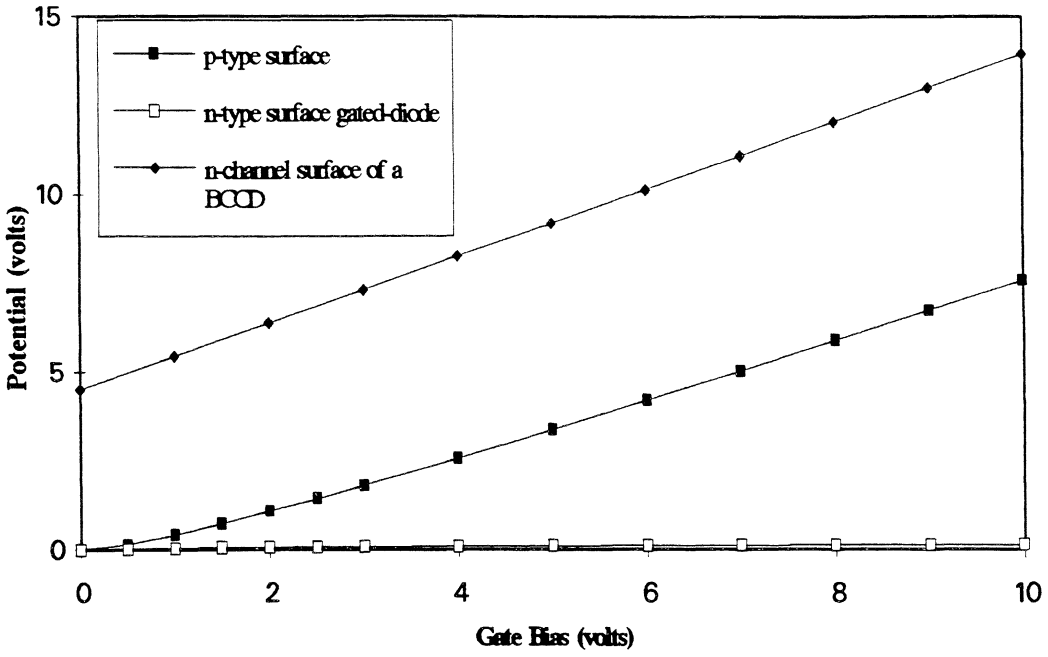


Fig 5.8. The variation of potential as a function of gate bias for; the surface of the p-type region in a gated diode (or CCD), the surface of the n-type region in a gated diode, and the surface of the n-channel in a BCCD. Assuming no substrate bias, $N_D = 1 \times 10^{16} cm^{-3}$

It can be seen from fig 5.8 that the inversion layer cannot develop in the p-stop of a BCCD, because on application of a positive gate bias (or negative substrate bias) the decrease in electron potential at the p-stop surface is matched by a similar decrease at the n-channel surface. Therefore the potential gradient between the two surfaces remains, and any electrons present in the p-stop are swept to the n-channel and the potential well.

5.2.2.2. $-10V \leq V_{SS} < -6V$

As explained in section 5.2.2.1., dark current is independent of V_{SS} for negative substrate biases upto about -6V. However, further increase in negative bias leads to sharp decrease in dark current in the range $-7V \leq V_{SS} < -6V$, followed by a gradual decline for $V_{SS} < -7V$.

When static dark current is measured by d.c. biasing of the CCD, as in this instance, generated charge is not clocked from the device, but diffuses from the device due to the concentration gradient of electrons. In order to reach the device output, the charge has to flow under the output gate, which is held at 2V (V_{og}) As mentioned in sect 5.1., the negative substrate bias was actually simulated by application of a postive gate bias. Although for all purposes discussed so far this is electrically equivalent, the equivalence breaks down if the device is taken into a regime where V_{og} is critical. This is because V_{og} is effectively following V_{SS} instead of following V_G as it would if the substrate bias were being varied. As shown in fig 5.9, V_{og} can become critical for high positive gate biases.

If all other device gates are at zero volts, then the electrons have an incentive to diffuse into the channel under the output gate, and so dark current flows instantaneously (see fig 5.9.a.). If however the bias applied to the gates is increased above 2V then the output gate will present a barrier to their exiting from the device. This barrier prevents current flow from the device until the accumulation of charge is sufficient to raise the potential in the device buried channel to that of the buried channel under the output gate, as shown in fig 5.9.c. If V_G is futher increased to around 6.5V then V_{ns} reaches the potential under the output gate. (fig 5.9.d.) Once this condition is achieved, the charge accumulating in the device is able to reach the n-channel surface, so preventing further charge generation here. From fig 5.1 it can be seen that the drop in dark current observed at V_{SS}= -6.5V, is equal in magnitude to the drop observed at threshold "b" and is therefore consistent with the suppression of dark current generation from the n-channel surface.

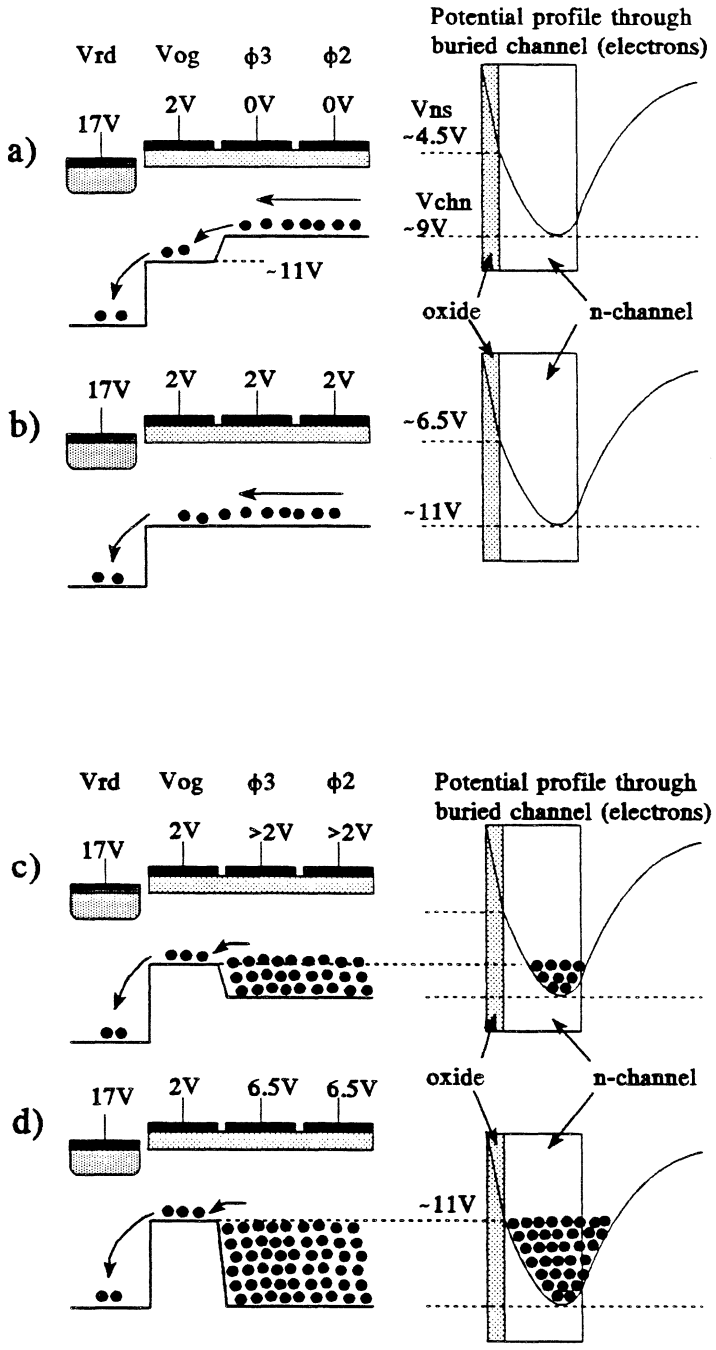


Fig 5.9. This shows the potential path for electrons diffusing from a device under static bias, for the cases where; a) $V_G = 0V$, b) $V_G = V_{og}$, c) $V_G > V_{og}$, and d) V_G is increased to the value at which V_{ns} is equal to the potential in the channel under the output gate.

As would be expected, changing the output gate bias causes a corresponding shift of the onset of this condition (see fig 5.10).

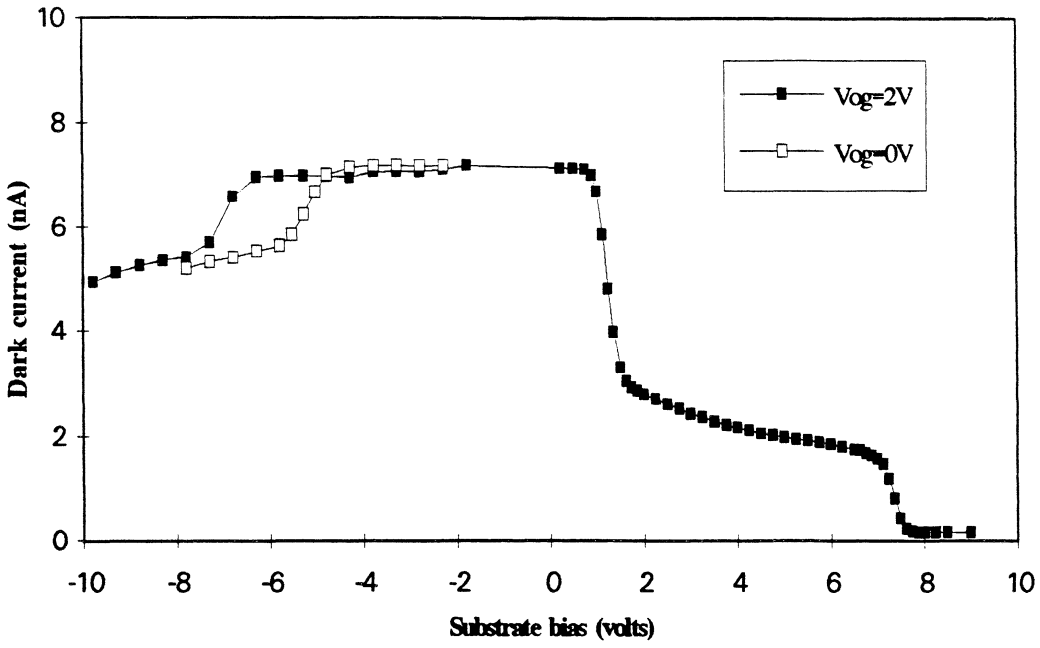


Fig 5.10. This plot shows how a change in output gate bias causes a corresponding shift in the onset of dark current suppression at the n-channel surface.

The gradual drop in dark current taking place in the range $-10V \leq V_{SS} < -7V$, must be caused by suppression of current generation at the p-stop surface, as this is the only significant source of current with the device in this state.

Fig 5.11 is a schematic showing the potential well in the n-channel, and the confinement barrier presented by the p-stop. As V_G is increased ψ_B, will increase and so the potential (for electrons) at the p-stop surface reduces. For the case where $V_{SS} = -7V$, the electrons accumulate until they reach the potential at the n-channel surface, but none are able to spread to the p-stop surface. Increasing the negative substrate bias beyond -7V however pulls the edges of the p-stop surface down to the level of the buried channel under the output gate (see fig 5.9) and accumulated electrons are now able to reach these edges and suppress current generation. As negative V_{SS} is increased further the electrons spread further along the p-stop surface and so the dark current continues to fall.

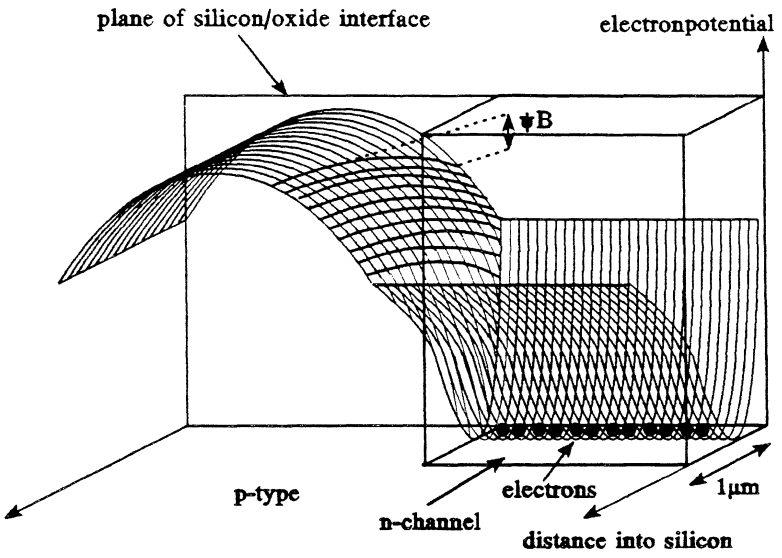


Fig 5.11. Schematic showing the approximate potential variation in the p-stop / n-channel system.

References for Chapter 5

[1] T. Roy, "Ionising Radiation Induced Surface Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1993.

[2] J.T. Wallmark, and H. Johnson, "Field-Effect Transistors: Physics, Technology and Applications", Published by Prentice-Hall, 1966.

[3] E.H. Nicollian, and J.R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology", Published by John Wiley and Sons, 1982.

[4] A.S. Grove, "Physics and Technology of Semiconductor Devices", Published by John Wiley and Sons, 1967.

[5] A.S. Grove, O. Leistiko Jr, and W.W. Hooper, "Effect of Surface Fields on the Breakdown Voltage of Planar Silicon p-n Junctions", IEEE Trans. Electron. Dev., Vol 14, 3, 157-162, 1967.

[6] T.P. Ma, and P.V. Dressendorfer, "Ionizing Radiation Effects in MOS Devices and Circuits", Published by Wiley Interscience, 1989.

Flat-band Voltage Shifts due to X-ray Irradiation

6.1 Measurement of the Flat-band Voltage Shift

There are several bias thresholds concerned with CCD operation. If a voltage shift is induced in the device by irradiation then each of these thresholds will also shift. Monitoring of the position of any these thresholds therefore provides a means of determining the size of the voltage shift. Those parametric thresholds employed during this work are outlined below.

6.1.1. Anti-blooming Drain Bias.

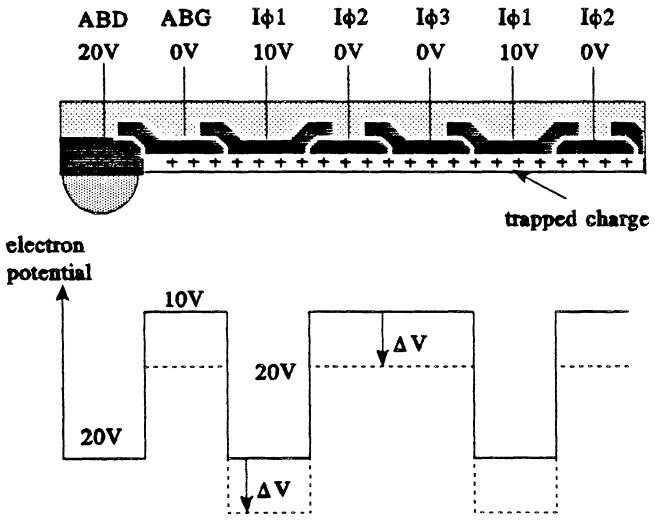


Fig 6.1. The channel potential under the anti-blooming drain compared to that under the gates. The continuous line denotes channel potential pror to irradiation and the dashed line denotes channel potential after a voltage shift, ΔV.

The anti-blooming drain is present only on the CCD02 structure. Fig 6.1 is a schematic showing the anti-blooming drain and its neighbouring gates. If the bias applied to the anti-blooming drain, V_{abd} is reduced sufficiently, such that its channel potential falls below that under the anti-blooming

gate, then charge injection from V_{abd} into the device results, and a large increase in dark current is seen. Typically in an unirradiated device V_{abd} would have to be lowered to around 10V for this threshold to be reached, but any voltage shift caused by trapped charge below the anti-blooming gate will cause a corresponding change in this threshold.

6.1.2. Reset Drain Bias

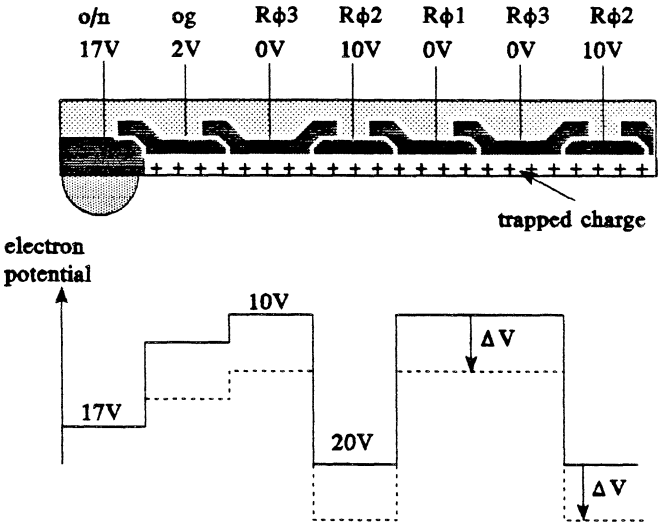


Fig 6.2. The channel potential under the output node (o/n), output gate (og), and neighbouring gates. The output node is floating, but is reset to the reset drain bias by ϕ_R (see fig 1.11). The continuous line denotes channel potential prior to irrdaiation, and the dashed line denotes channel potential after a voltage shift, ΔV.

Fig 6.2 shows the channel potential close to the reset drain. If the reset drain voltage, V_{rd}, is reduced such that its potential falls below that of the channel under the output gate, then it is no longer attractive to charge residing under the output gate, following clocking from the device. When this happens, no charge passes onto the output node until sufficient electrons have accumulated under the output gate, to reduce its channel potential to that of the reset drain. Consequently current still flows, but the image recorded by the device is no longer "read out" correctly. If V_{rd} is reduced still further, such that its channel potential falls to the level of that under the RΦ3 gate (with gate at 0V) then no charge passes to the output node, and no current flows. Reducing V_{rd} below this point

causes electrons to be injected into the device from the output node, and so current flows in the opposite direction. As with the anti-blooming drain bias, a voltage shift in the device causes a corresponding change in the V_{rd} threshold at which dark current falls to zero.

6.1.3. The Reset FET

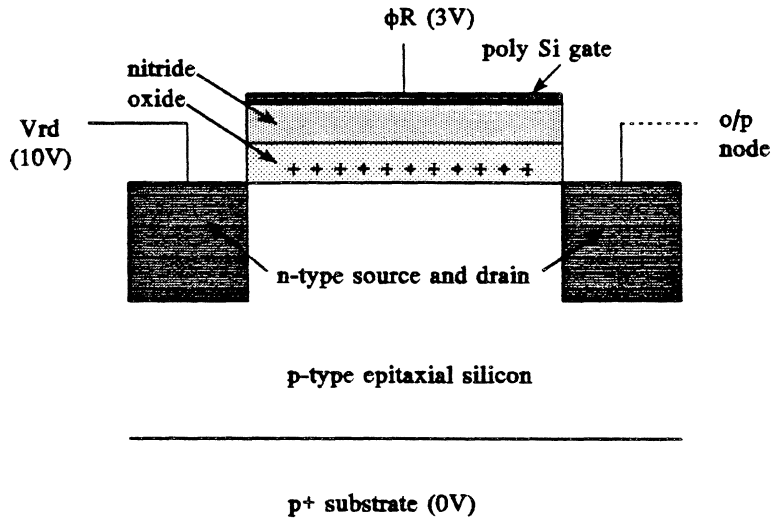


Fig 6.3. The reset transistor. Voltages shown are those applied during irradiation.

The reset transistor (see section 1.1.7.) is on-chip, and therefore sensitive to radiation induced voltage shifts. A flat-band voltage shift in the gate dielectric of the reset transistor, causes a corresponding reduction in its gate threshold voltage. This threshold voltage can be measured by passing a small signal square wave down the reset drain line, with the device d.c. biased. The square wave is then seen on the device output, provided that the reset transistor is switched on. If the gate bias, Φ_R is reduced below the threshold, then the rest transistor switches off, and the square wave is no longer seen on the device output.

The voltage shift associated with the reset transistor may differ from that measured above the n-channels in the body of the device. Unlike the electric field in the oxide over the n-channels, the field in the oxide above the reset transistor is a function of gate bias, and so voltage shift is likely to be a function of bias condition of the transistor during irradiation. The bias used during these irradiations is shown in fig 6.3.

6.1.4. The Onset of Inversion

When the substrate bias is increased to a threshold value (typically between 7 and 9V, see section 5.1), such that it reaches the potential at the n-channel surface, holes are injected from the substrate with the result that an inversion layer is formed at the n-channel surface. Consequently charge generation here is suppressed and a step reduction in dark current is observed. The threshold for this step is determined by the potential at the n-channel surface, and so is linearly related to the gate bias, and any built-in bias due to fixed charge in the oxide. Therefore any flat-band voltage shift seen in the oxide above the n-channel following irradiation, causes a corresponding shift in the threshold for inversion [1].

6.2. The Conventional Device

The CCDO2 was the principal device used for these measurements. Voltage shift as a function of dose, was measured both for a device unpowered during irradiation, and for devices powered during irradiation. The measurement of radiation voltage shift for the powered case was reproduced on several devices. However, as this work is concerned with devices used for medical imaging, which are not likely to be irradiated whilst unpowered, and taking account of the limited supply of devices, it was not considered necessary to reproduce the "unpowered" measurement on a second device.

6.2.1. Conventional Device Unpowered

Typical plots for the device before, and after irradiation are shown in figs 6.3, and 6.4. The voltage shift was found to be approximately 10mV per krad. This compares with the shift of 14mV per krad for irradiation by Co^{60} gamma [2].

The reduced voltage shift caused by the x-rays (about 70% of that for high energy gammas) is explained by the reduced dose seen by the gate oxide during x-ray irradiation (see section 3.3.5.). Therefore, whilst this measurement is significant in the sense that it indicates that a beam of 70kVp x-rays will induce a smaller voltage shift in the device than a beam of gammas which generates an equivalent signal, this difference is consequence of the interaction between neighbouring layers in the device, and not of the intrinsic hardness of the oxide to x-rays as opposed to gammas.

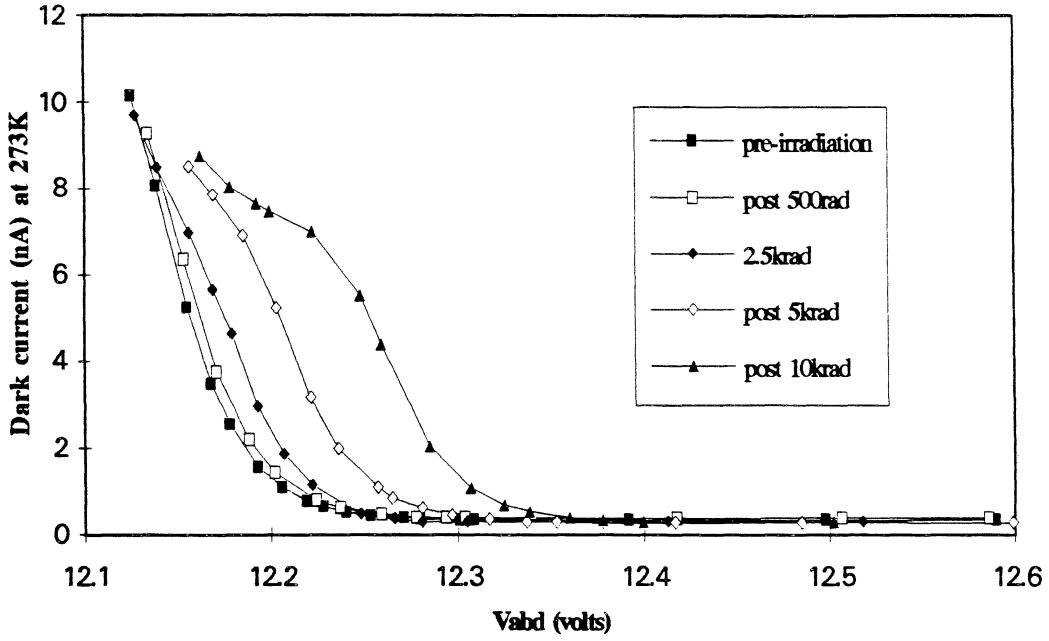


Fig 6.4. The shift in V_{abd} vs I_d characteristic of a CCD02 device (irradiated with x-rays unpowered).

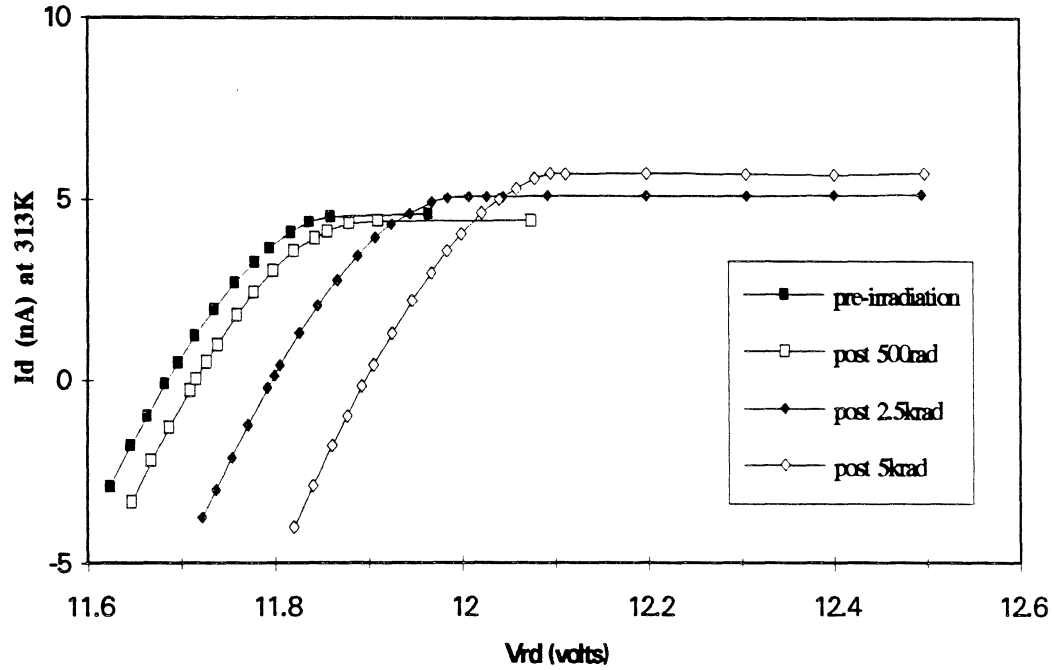


Fig 6.5. The shift in V_{rd} vs I_d characteristic of a CCD02 device (irradiated with x-rays unpowered).

6.2.2. Conventional Device Powered

The voltage shift in a device powered during irradiation was found to be 45mV per krad, with the spread in measurements implying an uncertainty of about ±5mV per krad. Typical plots for the device before, and after irradiation are shown in figs 6.6, and 6.7.

These results compare with voltage shifts of 120mV per krad for Co^{60} gammas [2], and 85mV per krad for Sr^{90} betas [1]. As was explained in the previous section, for irradiations with 70kVp x-rays, the dose seen by the gate oxide is smaller than that seen by both the epitaxial layer, and the PIN diode . However this dose factor (approximately 0.67 compared to the PIN diode) only partially explains the difference in voltage shifts observed for the case of powered devices. Allowing for the difference in oxide dose the voltage shift is still only around 60% of that seen for the gammas. This is explained by considering the yield of holes which escape recombination following absorption of the two types of radiation. From fig 2.4, it can be seen that the reduced flat-band voltage shift observed, is consistent with the reduced hole yield which would be expected for x-ray photons in the range 20-40keV, relative to the hole yield for the 1.25MeV gammas. (20-40keV is the predominant range of absorption by a CCD from a 70kVp spectrum, see section 3.3.3.).

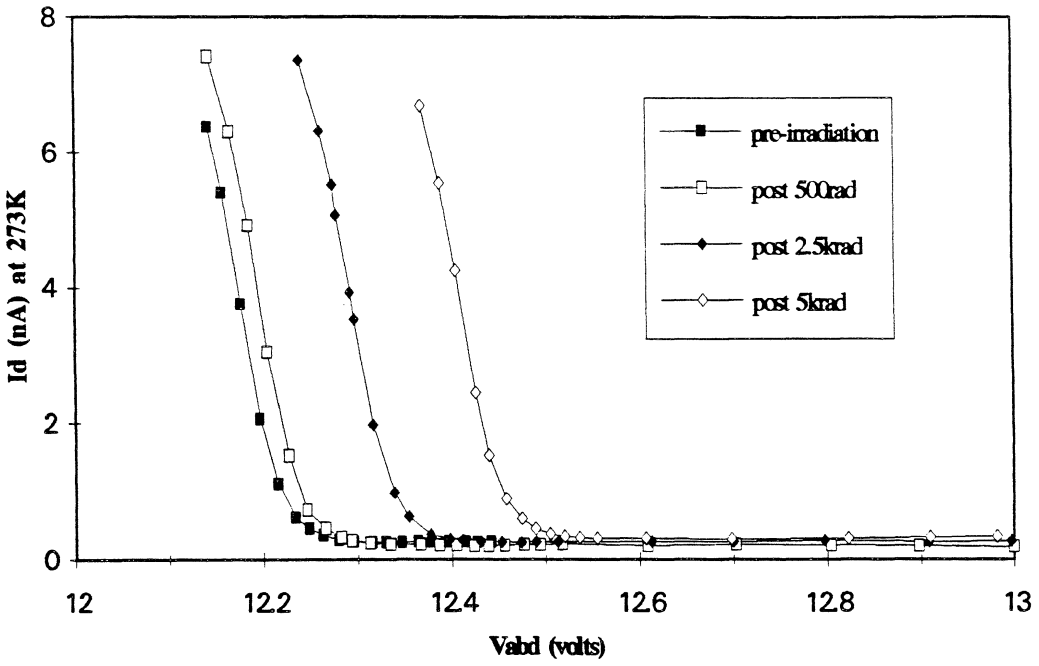


Fig 6.6. The shift in V_{abd} vs I_d characteristic of a CCD02 device (irradiated with x-rays powered).

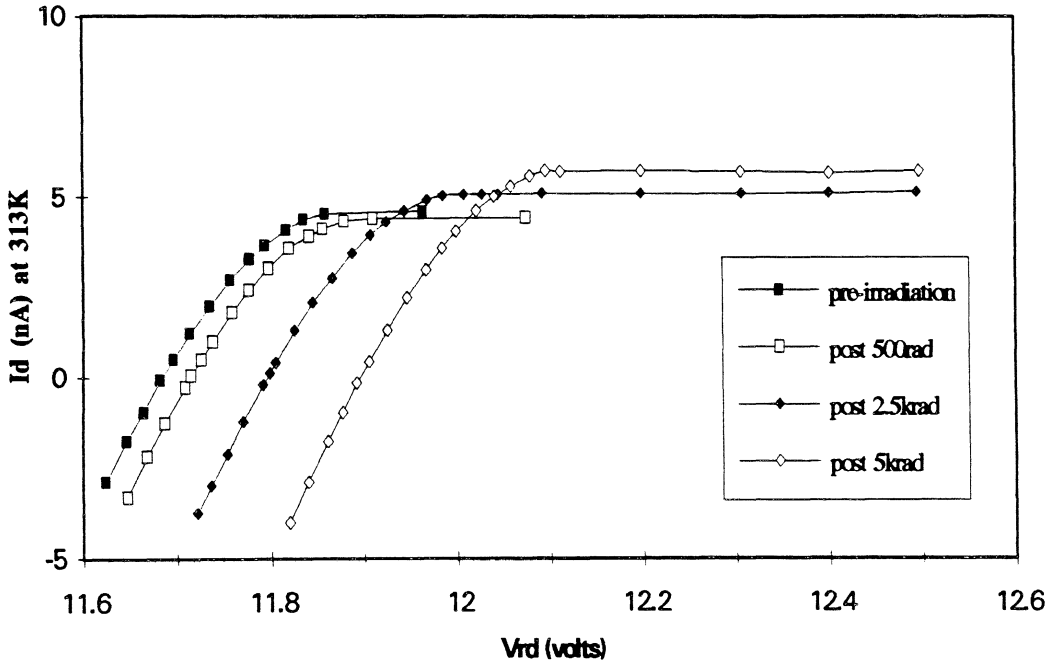


Fig 6.7. The shift in V_{rd} vs I_d characteristic of a CCD02 device (irradiated with x-rays powered).

The following measurements refer to the shift in reset threshold voltage (section 6.1.3), and onset of inversion threshold (section 6.1.4), and were made using conventional CCD05 devices. This provides the control data for the irradiation of scintillator coated devices described in section 6.3.

Whereas the electric field in the oxide above the n-channels was negative during irradiation, so causing holes predominantly to be trapped close to the SiO_2/Si_3N_4 interface, the field in the oxide of the reset transistor was positive, so driving holes to the Si/SiO_2 interface (see section 2.3.1.1). In this instance the charge sheet is acting across the capacitance of the dual dielectric rather than just the nitride layer, so, taking into account the smaller capacitance of the SiO_2 layer, the voltage shift per unit charge would be expected to increase three-fold.

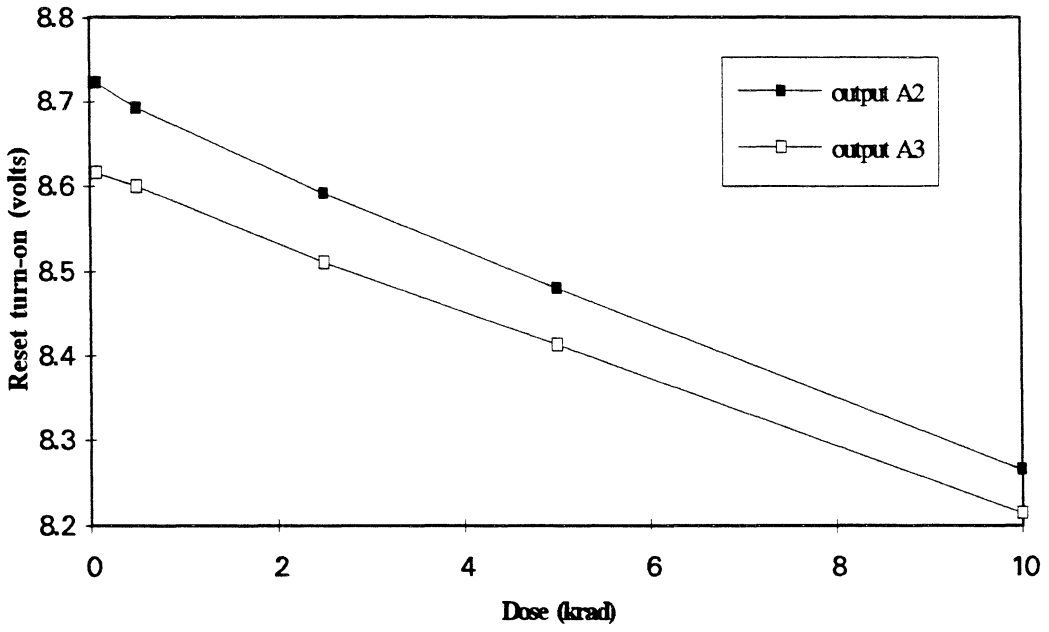


Fig 6.8. The reset transistor turn-on as a function of dose for a CCD05 device, at 300K. A2 is one of the two slow scan outputs, whilst A3 is one of the two high speed scan outputs. (Device powered during irradiation)

For the biasing conditions used during these irradiations (V_{ss}=0V, and ϕ_R permanently "on" at 3V) the actual voltage shift was found to be of a similar magnitude to that above the n-channels, at 40-45mV per krad (see fig 6.8). This is understood to be largely a consequence of radiation generated electrons passing from the SiO_2 layer into the Si_3N_4 layer and becoming trapped, so partially

compensating the effect of the trapped holes in the SiO_2 [3], although it may also be partly explained by a smaller trap density at the Si/SiO_2 interface, or a smaller field dependent cross-section for capture of holes than for traps at the SiO_2/Si_3N_4 interface.

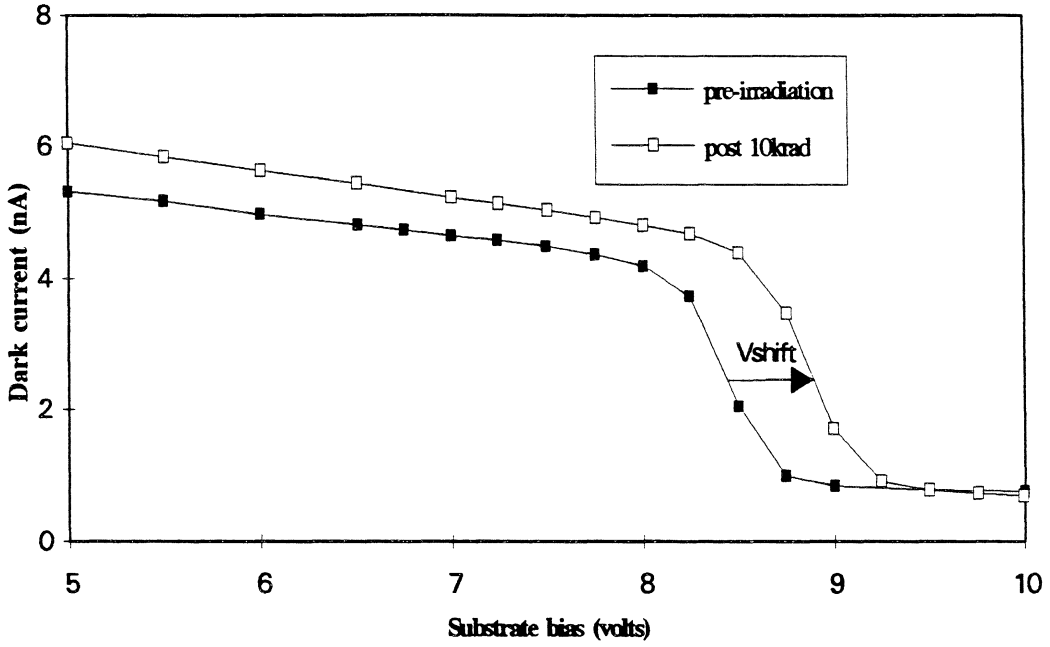


Fig 6.9.The static dark current (at 300K) of a conventional CCD05 device as a function of substrate bias, before and following x-ray irradiation (device powered during irradiation).

As expected the voltage shift measured from the shift in the onset of inversion, is similar to that measured for the V_{abd}, and V_{rd} thresholds at 45mV per krad.

6.3. Scintillator Coated Devices

The scintillator coated devices investigated here were CCD05 devices. As such they do not have an anti-blooming drain, and their multiple output nodes make determination of the reset drain bias threshold impractical to measure. Because of this, the principal measurement performed with these devices was the reset transistor turn-on as described in section 6.1.3. The dependence of dark current upon substrate bias was also recorded, before and after irradiation, so that the shift measured from the reset transistors, which are located at the extreme edge of the chip, could be at least

approximately verified by a measurement taken from the body of the device. The orientation of the CCD05 device is shown in fig 6.10.

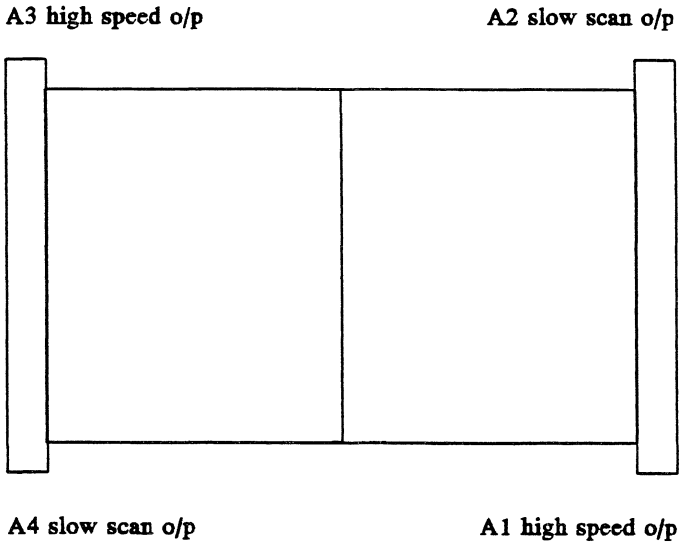


Fig 6.10. The orientation of the CCD05 outputs.

6.3.1. The CsI(Tl) Layer

The voltage shift in a CsI(Tl) coated device, powered during irradiation, was found to be in the range 90-110mV per krad (see figs 6.11 and 6.12). Thus in terms of flat-band voltage shift, the damage sustained by the device is approximately twice that sustained by a conventional device for the same fluence of x-rays. However the signal measured in the device during exposure to 70kVp x-rays was approximately five times greater than that measured for conventional devices for the same radiation flux. This suggests the possibility of greater device longevity, and **smaller patient dose**, if the enhanced sensitivity could be used to allow the device dose per exposure to be reduced.

The increase in voltage shift caused by the CsI(Tl) layer is significantly **less** than the increase in gate

oxide dose predicted by the PHOTCOEF simulation, of 5-fold (see appendix 1). However this is to be expected, because much of the dose absorbed by the oxide, when the scintillator is in place, is in the form of low energy secondary electrons transported from the scintillator. Consequently the hole yield is reduced, and so the voltage shift per unit dose in the oxide is also reduced.

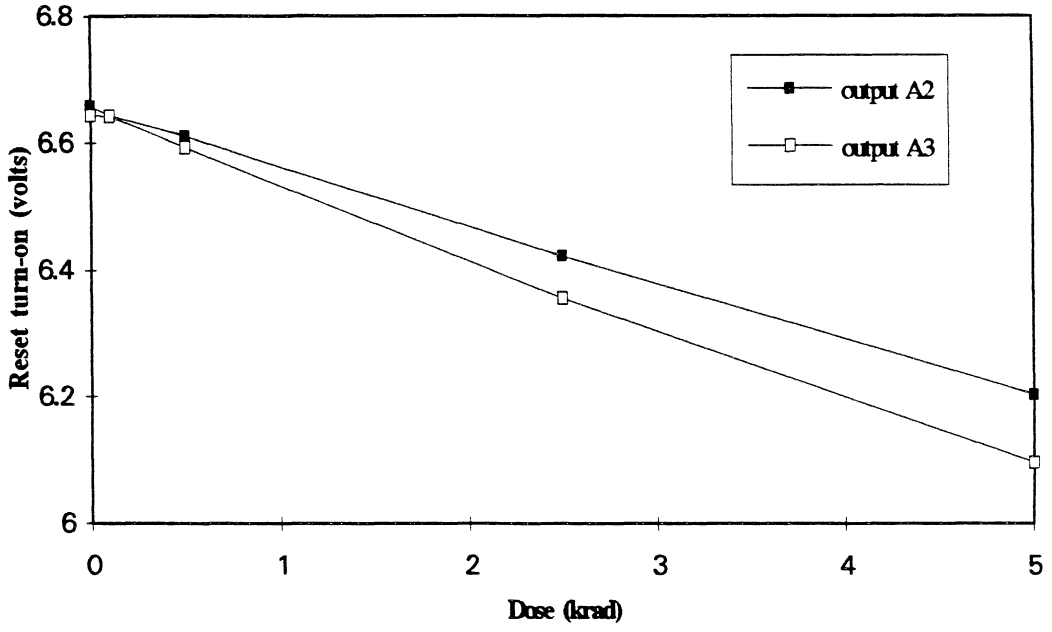


Fig 6.11. The reset transistor turn-on as a function of dose for a CsI(Tl) coated CCD05 device. A2 and A3 as explained for fig 6.8 (device powered during irradiation).

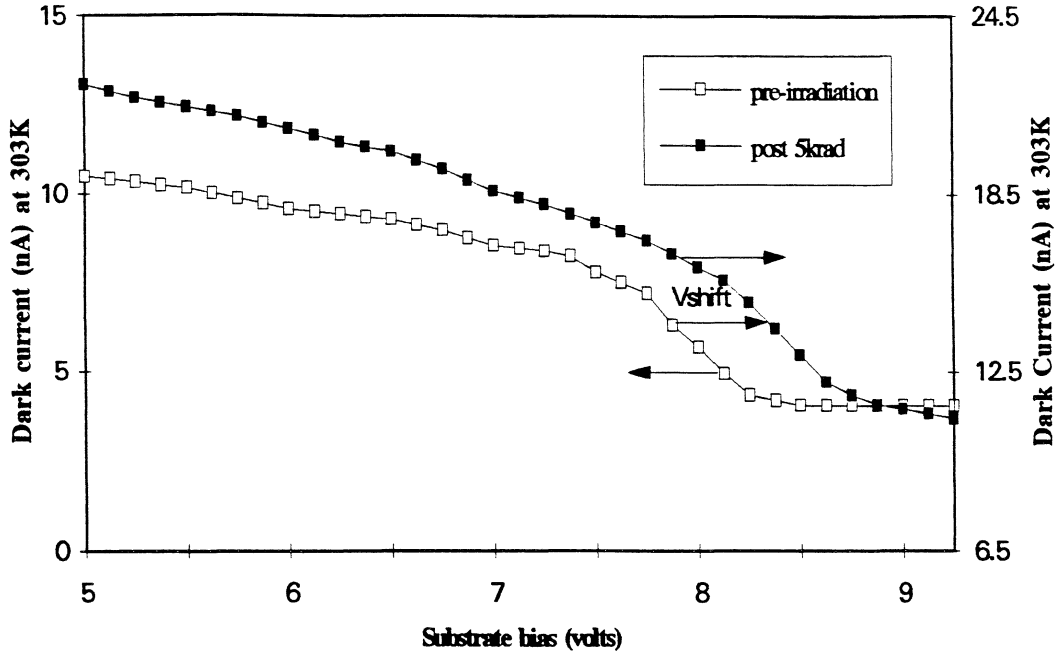


Fig 6.12. Clocked dark current versus substrate bias for the CsI(Tl) coated CCD05, before and after 5krad irradiation. The arrows indicate the appropriate scale for each plot (device powered during irradiation).

6.3.2. The Gadox(Eu) Layer

The principal voltage shift characterisation for a Gadox(Eu) coated device was performed on a device (CCD05GC-1) being used as part of an annealing programme, as described in section 7.3.2. Consequently the device irradiations were punctuated by 15 hour anneals at a temperature of 408K. At a later stage however a second Gadox(Eu) coated device (CCD05GC-2) was received and so further measurements were made.

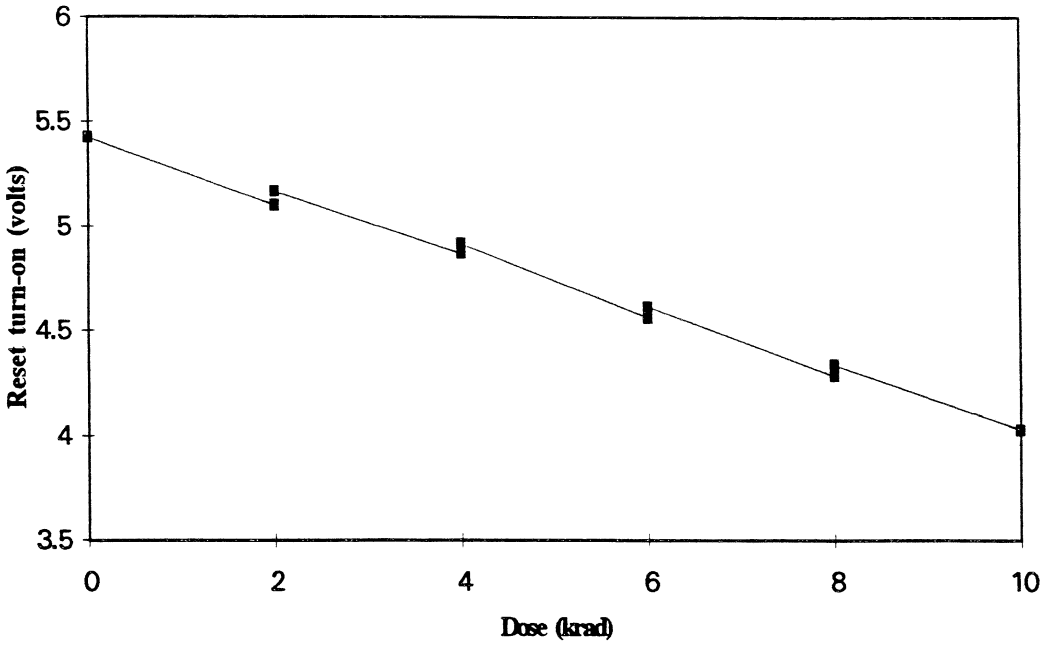


Fig 6.13. The reset transistor turn-on as a function of dose, for the Gadox(Eu) coated device, CCD05GC-1. The measurements were made using the slow scan output, A2 (device powered during irradiation).

The shift in reset turn-on for the Gadox(Eu) coated device is shown in fig 6.13. The slight recovery in between irradiations is a consequence of annealing. The voltage shift was found to be approximately 160mV per krad for this device, significantly greater than was seen for the CsI(Tl) coating.

The second Gadox(Eu) coated device (CCD05GC-2) was primarily intended for an experiment to test for high temperature damage to the scintillator. This experiment was quickly completed however, and so the device was available for further voltage shift measurements. A greater range of measurements was carried out on this device and it was found that the voltage shift was not uniform over the whole area, as had been the case for the conventional device and the CsI(Tl) coated device. In addition to the reset turn-on of output A2, the reset turn-on of A4 (diametrically opposite A2, see fig 6.10) was monitored. Also the static dark current as a function of substrate bias, was measured to allow the central area of the device to be investigated.

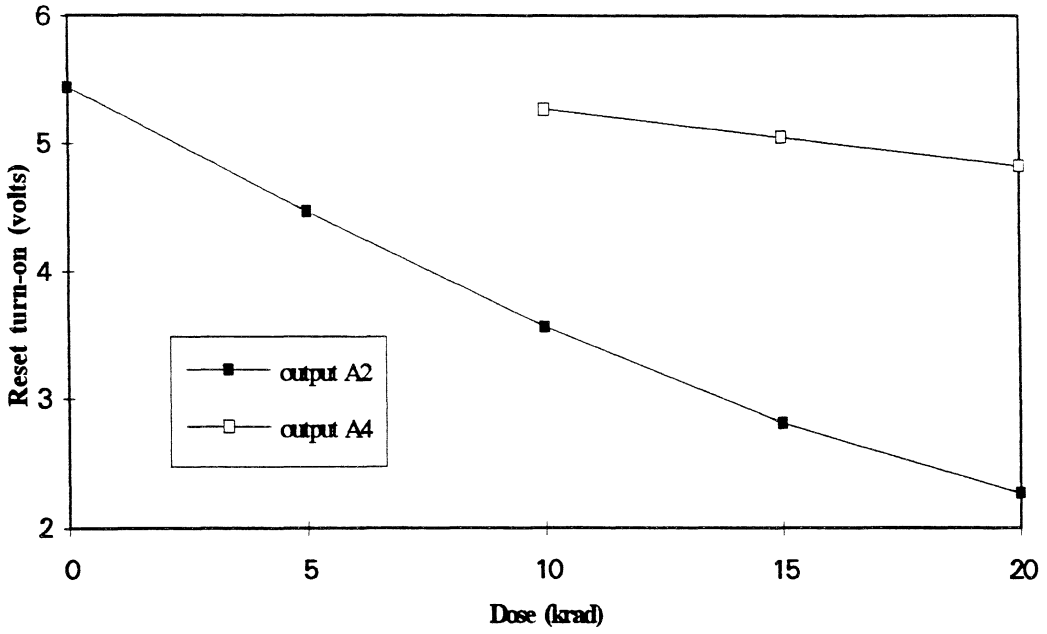


Fig 6.14. The reset transistor turn-on as a function of dose for the Gadox(Eu) coated device, CCD05GC-2 (device powered during irradiation).

The shift in reset transistor turn-ons with dose are shown in fig 6.14. The initial voltage shift for output A2, at approximately 190mV per krad, was even greater than that in CCD05GC-1, although the shift per unit dose decreased with accumulated dose to approximately 110mV per krad by the final irradiation (note the increased dose levels used here). The reset turn-on for A4 was only measured for the later irradiation stages. It was found that the voltage shift was similar to that of an uncoated device at approximately 43mV per krad, which suggested that the Gadox(Eu) coating does not cover the output circuitry on this side of the device.

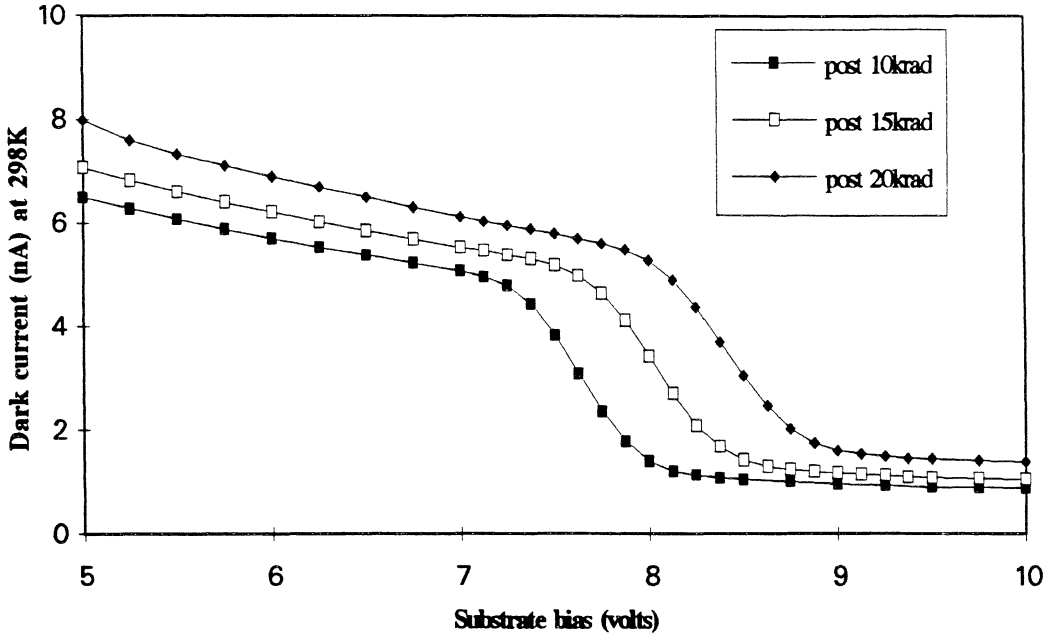


Fig 6.15. The static dark current of device CCD05GC-2 as a function of substrate bias, at three irradiation stages (device powered during irradiation).

The shift in the onset of inversion, with dose, is shown in fig 6.15. As the with reset turn-on of output A4, the static dark current as a function of substrate bias was measured only for the later irradiation stages. The voltage shift, as measured from this parameter was found to be in the range 90-100mV per krad, approximately the same as that seen for the CsI(Tl) coated device.

Device CCD05GC-2 was inspected with a microscope and it was found that the output circuitry corresponding to output A4 (including the output gate) was not covered by the Gadox(Eu) layer, as suspected, and that the covered output circuits were close to the edge of the layer. It is believed that the the inconsistency in voltage shift across the device is a result of thinning of the layer at the edges. As shown in fig 6.16, the increased voltage shift seen close to the edge of the layer is not fully accounted for by the dependence of oxide dose (as predicted by PHOTCOEF, see section 3.3.4) upon Gadox(Eu) thickness. The more likely explanation is that for thinner Gadox(Eu) layers the oxide dose is made up increasingly of photons from the original beam, rather than low energy electrons transported from the Gadox(Eu). This is demonstrated in fig 6.17, which shows the fractional penetration of 30keV photons through the Gadox(Eu), as a function of thickness.

Photons in the region of 30keV are the most important as far as direct dose deposition into the CCD is concerned (see fig 3.10). For the 200μm Gadox(Eu) layer only 15% of these photons reach the CCD, whereas for a thickness of 100μm the penetration reaches 40%. As the gate oxide dose is similar in both cases, it has to be concluded that the lack of direct oxide dose deposition with the thicker layer is compensated for by an increase in electron transported dose. These transported electrons are inevitably of lower energy than the original photons, and so the charge yield reduces (see section 2.2.1, esp fig 2.4).

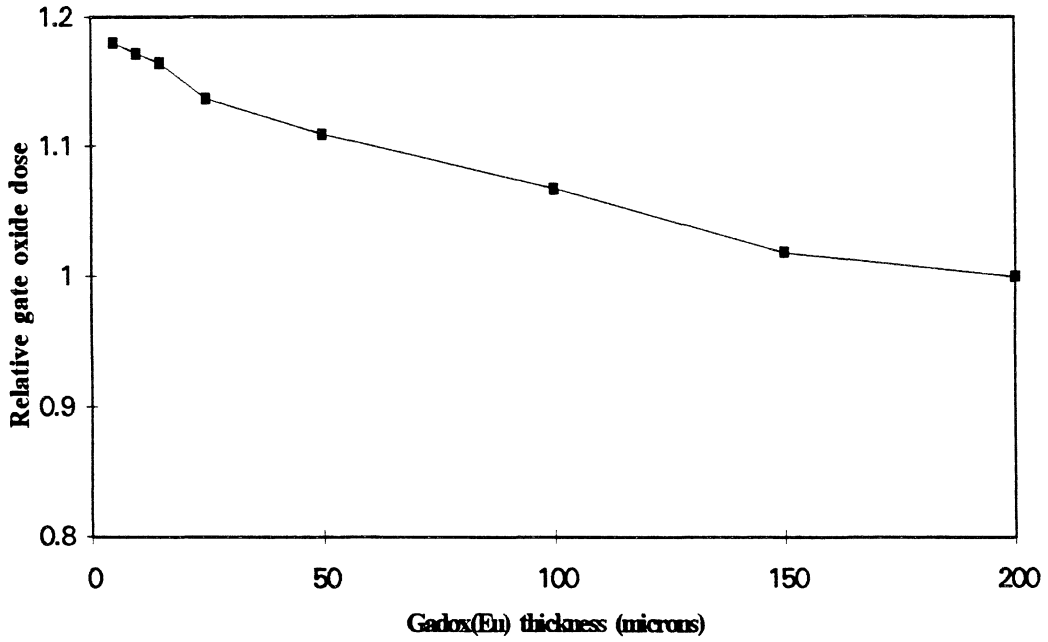


Fig 6.16. Relative gate oxide dose as a function of Gadox(Eu) thickness, as predicted by PHOTCOEF.

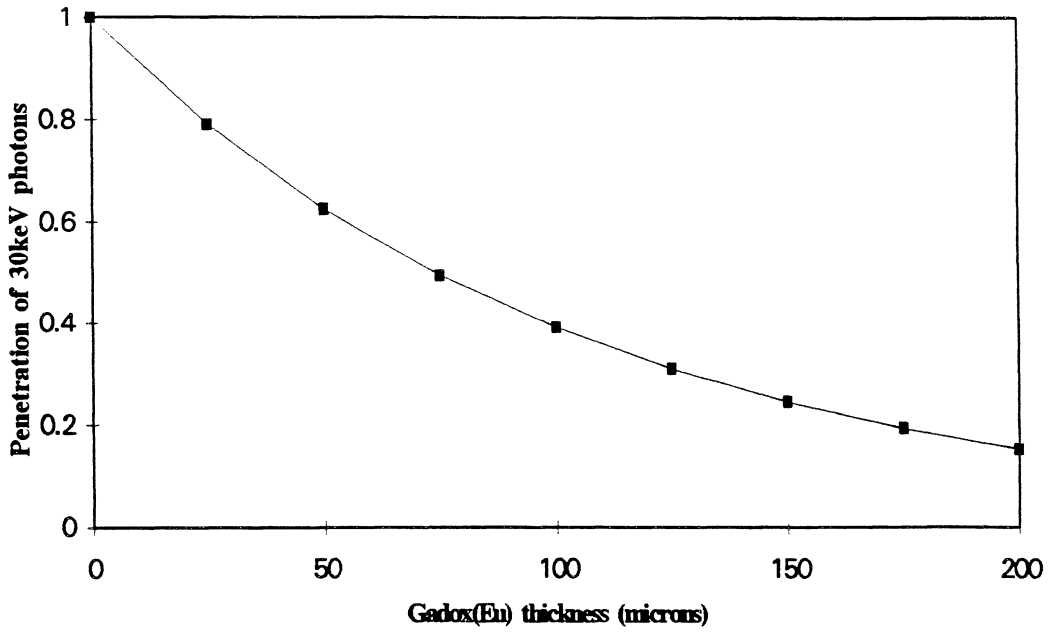


Fig 6.17. The penetration of 30keV photons through Gadox(Eu), as a function of thickness

If this hypothesis is correct then the voltage shift in the Gadox(Eu) coated devices should be reducible to approximately 100mV per krad, by extending the layer a few mm further at the device edges. As the layer is deposited at present though, the limiting factor for device longevity will be the enhanced shift which can be expected in the output circuitry and under the output gates.

As with the CsI(Tl) coated device the Gadox(Eu) layer was found to enhance device sensitivity to 70kVp x-rays by a factor of five..

6.4 Annealing out of Flat-band Voltage Shifts.

Whilst the anneals, described in section 7.3, were being performed, the flat band voltage of the devices was monitored by checking the reset turn-on threshold. As shown in fig 6.18, at high temperatures a significant proportion of the initial radiation induced voltage shift was recovered.

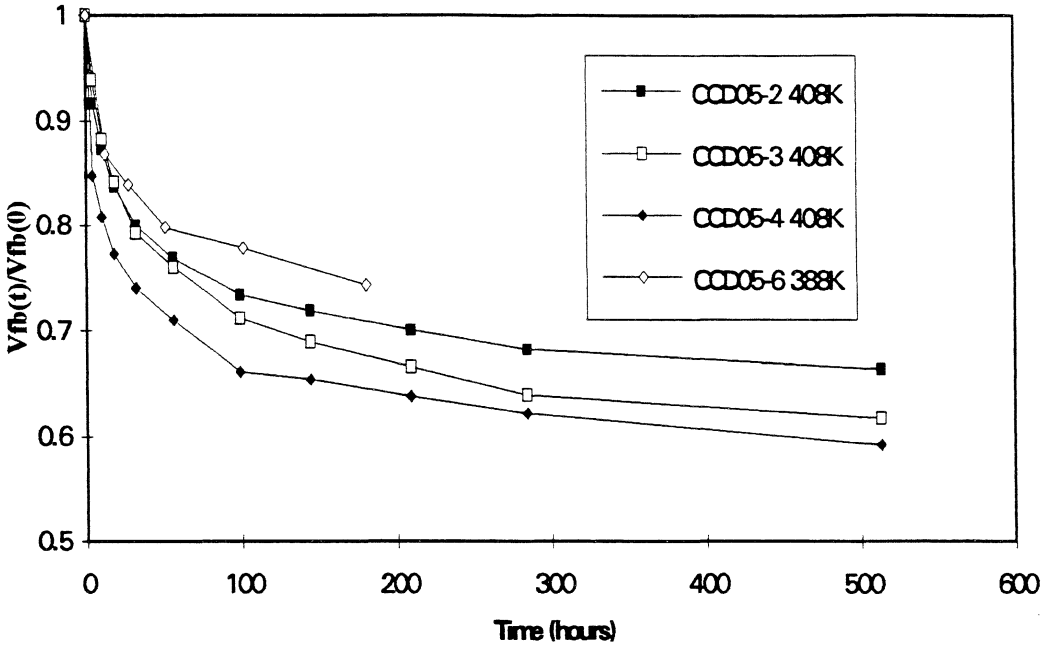


Fig 6.18 Recovery of flat band voltage shift in CCD05 devices irradiated to 10krad, with a nominal shift of 450mV. The plot shows the fraction of the initial shift remaining, as a function of anneal time for the temperatures shown.

Although generally temperatures of 420K-470K (150°C- 200°C) are considered necessary to remove trapped charge quickly [4], some relaxation occurs at lower temperatures, especially after prolonged anneals. The extent of recovery found here is fairly typical for the duration and temperature of the anneals [5 p421]. However the annealing characteristic is very process dependent, and significant annealing has been observed by Lelis et al [6] at temperatures as low as 325K (~50°C).

References for Chapter 6

[1] T. Roy, "Ionising Radiation Induced Surface Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1993.

[2] M.S. Robbins, "Radiation Damage Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1992.

[3] N.S. Saks, J.M. Killiany, P.R. Reid, and W.D. Baker, "A Radiation Hard MNOS CCD for Low Temperature Applications", IEEE Trans. Nucl. Sci., NS-26, 6, 5075-5079, 1979.

[4] A. Holmes-Siedle, and L. Adams, "Handbook of Radiation Effects" Published by Oxford University Press, 1993.

[5] T.P. Ma, and P.V. Dressendorfer, "Ionizing Radiation Effects in MOS Devices and Circuits", Published by Wiley Interscience, 1989.

[6] A. J. Lelis, T.R. Oldham, and W.M. DeLancey "Response of Interface Traps During High Temperature Anneals", IEEE Trans. Nucl. Sci., NS-38, 1590-1597, 1991.

Dark Current Changes Due to X-ray Irradiation

7.1 Introduction

As described in section 2.3., dark current in the CCD is generated via defects sites either in the bulk silicon, or at the Si/SiO_2 interfaces. Exposure to radiation can lead to an increase in the number of these states, and hence a corresponding increase in dark current level. It is known that 70kVp X-rays do not carry sufficient energy to cause defects in the silicon bulk (section 2.1.1.), therefore, as far as this work is concerned, states at the Si/SiO_2 interfaces are responsible for increases in dark current. This chapter is concerned primarily with the magnitude of the dark current increases, caused by such as buildup of interface states. The location and concentration of these states is investigated in chapter 8.

The change in dark current following irradiation can be considered to consist of two components, a prompt component seen immediately following irradiation, and a time dependent component (reverse annealing) which occurs gradually. The overall change is given by the sum of these components.

7.2 The Prompt Increase in Dark Current

7.2.1. The Conventional Device

These measurements were performed using CCD05 devices, although the results are also applicable to devices with similar architecture, such as the CCD02. As this architecture is employed in devices of varying surface area, all current measurements are quoted in terms of the dark current density, ($nAcm^{-2}$).

Fig 7.1. shows the dark current at 300K, in a CCD05 device as a function of substrate bias, V_{SS}, both

before, and after a 10krad irradiation with 70kVp X-rays. The dark current increase caused by the radiation is approximately 0.7 $nAcm^{-2}$ in the range $5V<V_{SS}<7V$, where the device is typically operated. Fig 7.2 shows the dark current dependence upon temperature for another CCD05 device before and after a 10krad irradiation. No allowance was made for the change in flat-band voltage caused by the radiation dose, but V_{SS} was set at 6V to ensure that the device was operating well away from the transient regions in which current becomes a strong function of substrate bias.

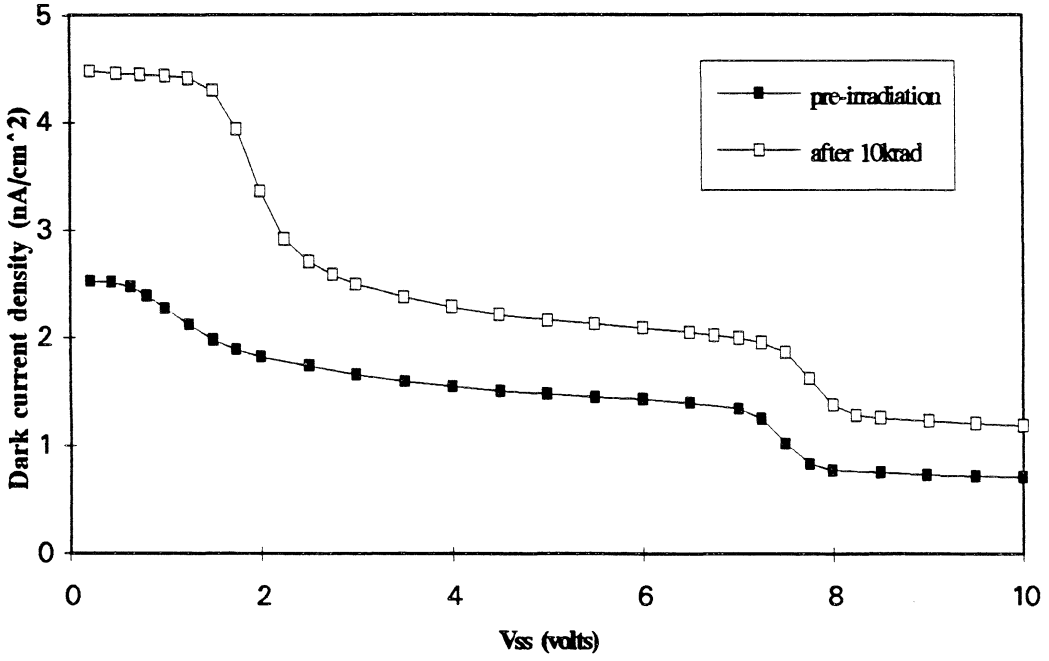


Fig 7.1. Clocked dark current as a function of V_{SS} for a CCD05 at 300K, before and after irradiation (device powered during irradiation).

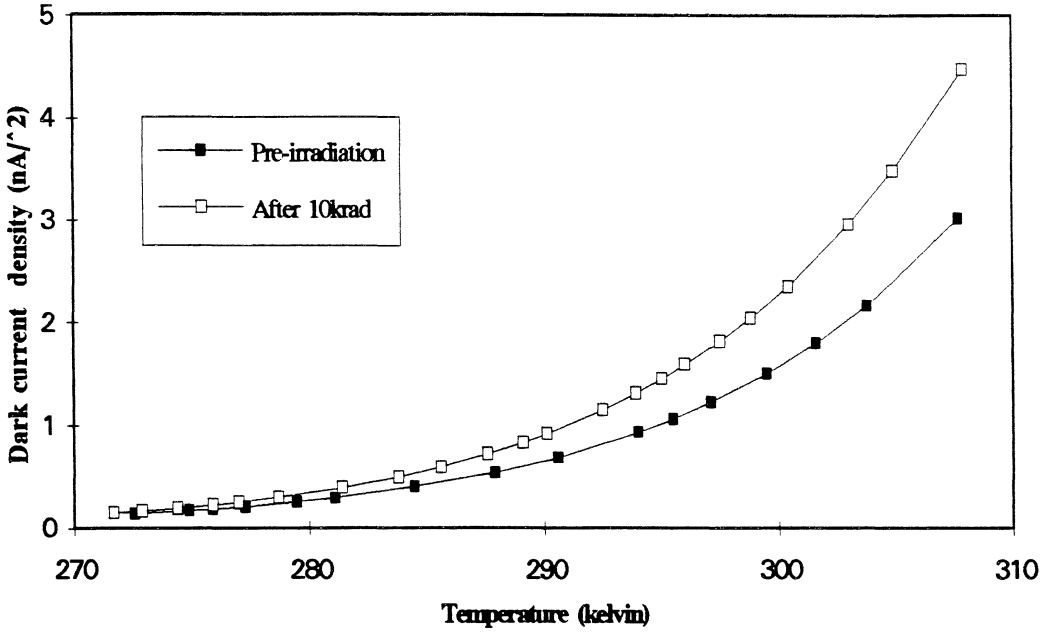


Fig 7.2 Clocked dark current (at V_{SS}=6V) as a function of temperature for a CCD05 (device powered during irradiation).

Fig 7.3 shows the change in dark current with dose for a CCD05 device irradiated to 10krad in steps. For the smaller doses the dark current increase is consistent with that expected from figs 7.1 and 7.2, assuming linearity with dose. However for accumulated doses of 5krad, and 10krad the dark current departs from that observed for the "one-off" 10krad irradiations. This is because the time intervals between successive irradiations is sufficient to allow a time dependent increase in dark current as described in section 7.3.

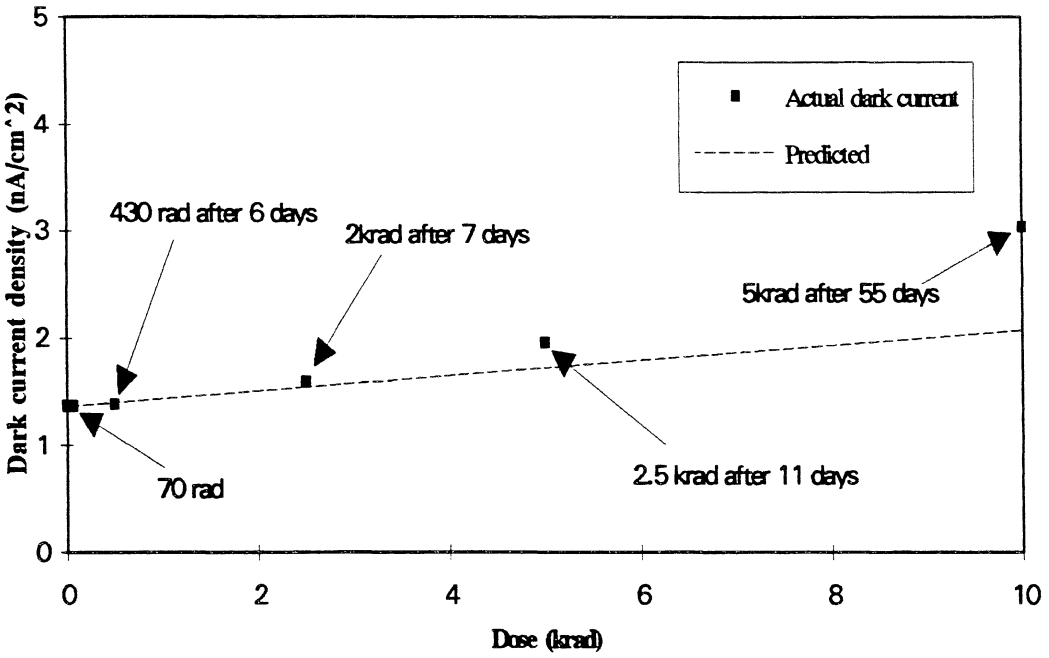


Fig 7.3. The change in clocked dark current (at 300K, and V_{ss}=6V) with dose for a CCD05 device. Also shown are the sizes of the step irradiations, and the time which had lapsed since the first irradiation (device powered during irradiation).

7.2.2. Scintillator Coated Devices

Two scintillator coatings were investigated in this work, CsI(Tl) which was deposited to a thickness of 50μm, and Gadox(Eu) ($Gd_2O_2S(Eu)$) which was deposited to a thickness of 200μm.

The dark current dose dependence of the CsI(Tl) coated device is shown in fig 7.4. The dark current at 300K was found to increase by approximately 0.26nAcm^{-2} per krad. As the flat-band voltage shifts associated with a device of this technology also needed to be investigated, it was necessary to carry out the irradiation in steps. The irradiations and device characterisations were completed within five days so minimising any dark current due to the time dependent process.

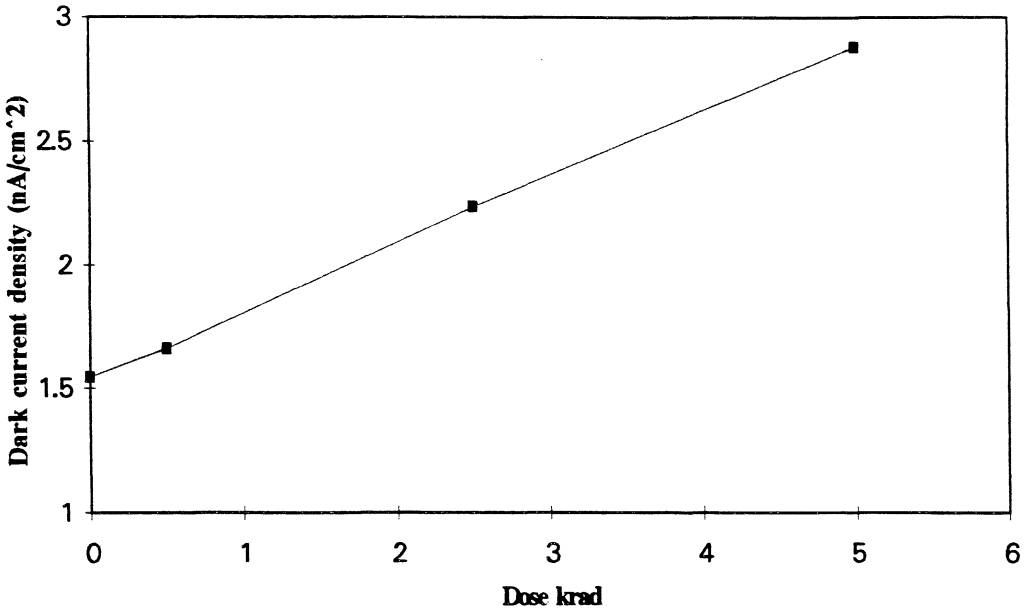


Fig 7.4 The change in clocked dark current (at 300K, V_{SS}=6V) with dose, for a CsI(Tl) coated CCD05 device (device powered during irradiation).

The dark current increase in the Gadox (Eu) coated device was characterised following a 2krad irradiation rather than the 10krad used for the other devices. This did reduce the precision of the measurement, but was necessary in order to allow the device to be used for the work described in section 7.3.

Fig 7.5 shows the dark current measurements taken from the Gadox coated device, with those for a conventional device. The increase per unit dose is similar in both cases, at approximately 0.07nAcm^{-2} per krad.

The most likely cause of the difference in dark current increase seen for the two scintillators, is the polyimide layer ($C_{28}H_{18}N_2O_4$) situated beneath the CsI(Tl). Any hydrogen released from the polyimide into the oxide, would be likely to lead to a buildup in Si/SiO_2 interface states (see section 2.2.2.2.) and a corresponding dark current increase.

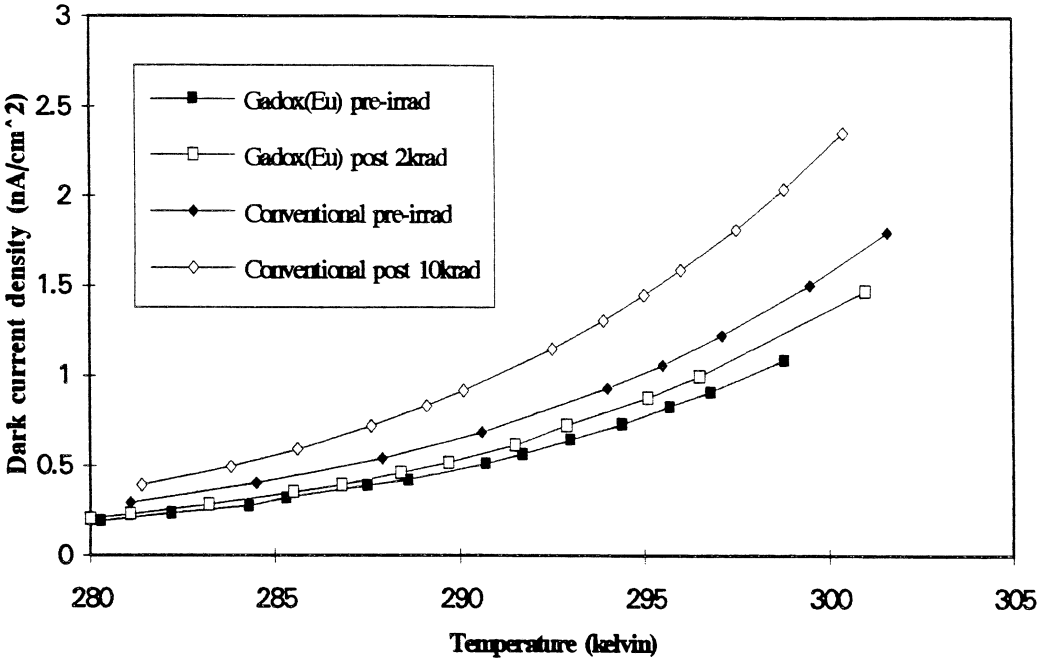


Fig 7.5. The irradiation induced increase in clocked dark current (V_{SS}=6V) (for a Gadox(Eu) coated device, compared with that for a conventional device (devices powered during irradiation).

7.2.3. The Inversion Mode Device (see section 1.3.1)

The dark current from an inversion mode CCD, both before and after a 10krad irradiation, is shown in fig 7.6. For the unirradiated device operated below the inversion thereshold (about 7.5V in fig 7.6) the dark current is similar to that seen for the conventional device, although there is an extra transition region at a substrate bias (V_{ss}) of around 5V. This extra transition is due the n-channel surfaces of the p-doped channel (see section 1.3) coming out of depletion, and accounts for a step of approximately half the size of that seen at 8V. For the unirradiated device operated in inversion, the dark current falls to a few $pAcm^{-2}$.

Irradiation of the device shifts the inversion threshold, as would be expected, but causes a negligible increase in dark current if the device is operated in inversion mode (approximately $2pAcm^{-2}$ after

10krad). If the irradiated device is operated out of inversion mode, then a dark current increase is observed. This increase is significantly smaller than for the conventional mode device, because the clocking scheme used (with all gates held at 0V, during imaging) ensures that the p-stop surfaces are all undepleted, and so any states generated here do not contribute to the dark current. The dark current increase at V_{SS} = 6V was approximately 15pAcm^{-2} per krad for the device investigated. However, because there is transition region positioned close to this substrate bias, the flat-band voltage shift may cause a perceived dark current increase of double this magnitude in other devices.

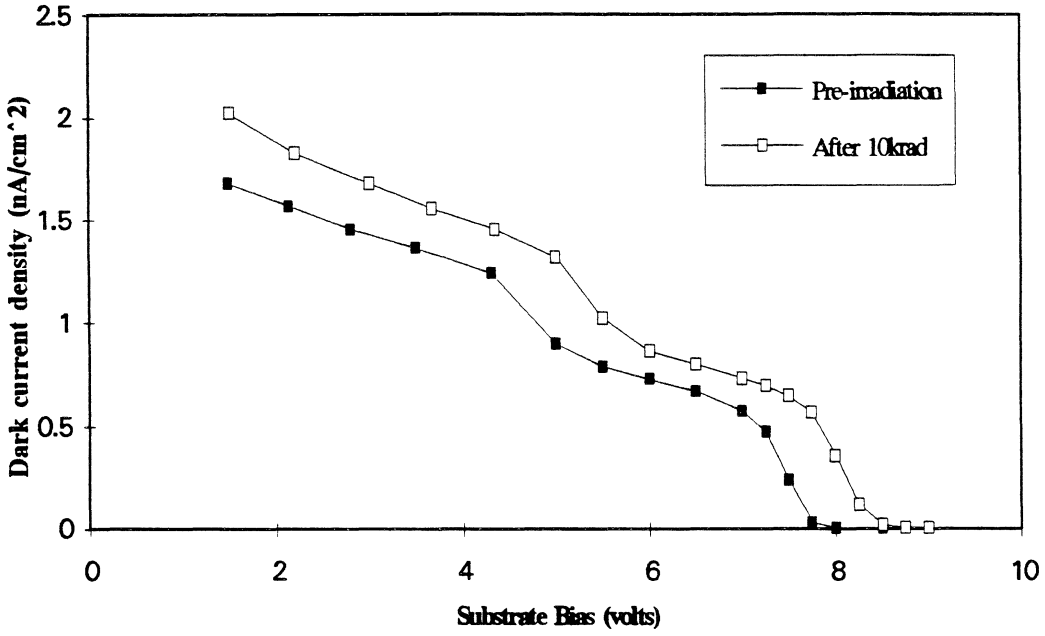


Fig 7.6. The clocked dark current (at 300K) in the inversion mode device CCD02IM-1, before and after irradiation.

7.3 The Time Dependent Increase in Dark current

7.3.1. The Conventional Device

Fig 7.7. shows the time dependent increase in dark current of a CCD05 device CCD05-1, after an initial 10krad irradiation. Between dark current measurements the device was stored at room temperature and was unbiased. After 7 months of storage the time dependent dark current increase had risen to 1.9nAcm^{-2} (measured at 300K, and V_{SS} = 6V), compared to the prompt increase of 0.7nAcm^{-2}.

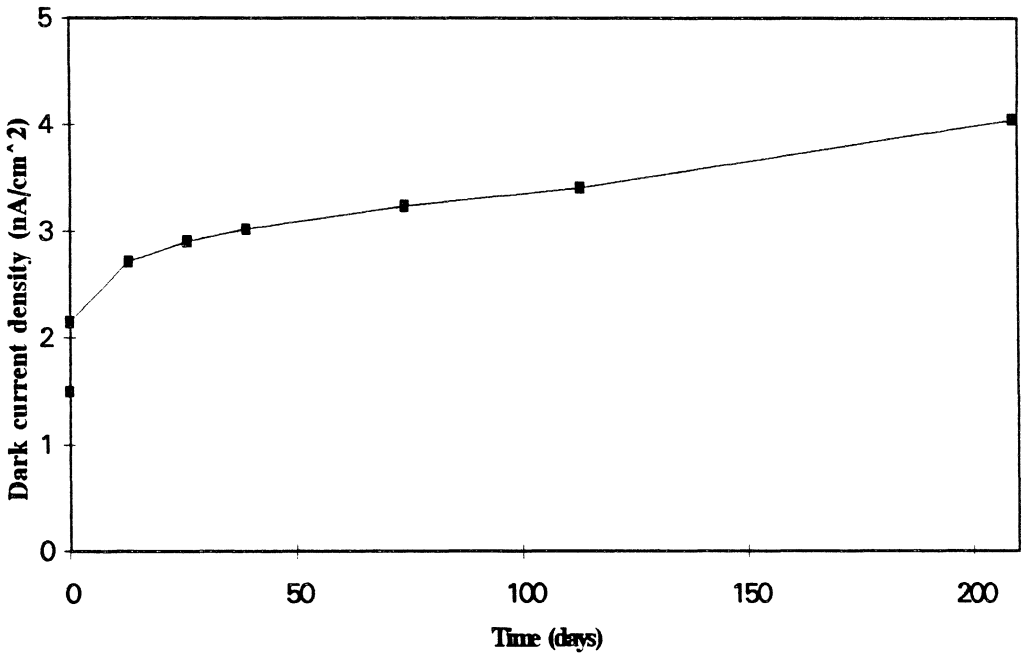


Fig 7.7. The increase in clocked dark current (at 300K and V_{SS} = 6V) of CCD05-1, irradiated to 10krad and then stored at room temperature whilst unbiased. The initial step, at time = 0 days, is the prompt increase in dark current following irradiation

To further characterise the time dependent process high temperature anneals were performed on a

series of devices. Three devices, selected from different production batches, were annealed at 408K for a total of 1000 hours (fig 7.8), in order to investigate batch to batch dependency. It was also the intention to saturate the process, if this was possible, to determine the maximum dark current increase. In addition to this, devices were annealed at 388K and 373K (fig 7.9), to enable the activation energy of the process to be determined. Using this energy barrier it is possible to predict the dark current increase which will be seen in devices stored at room temperature for long periods. (see section 9.3.2.2).

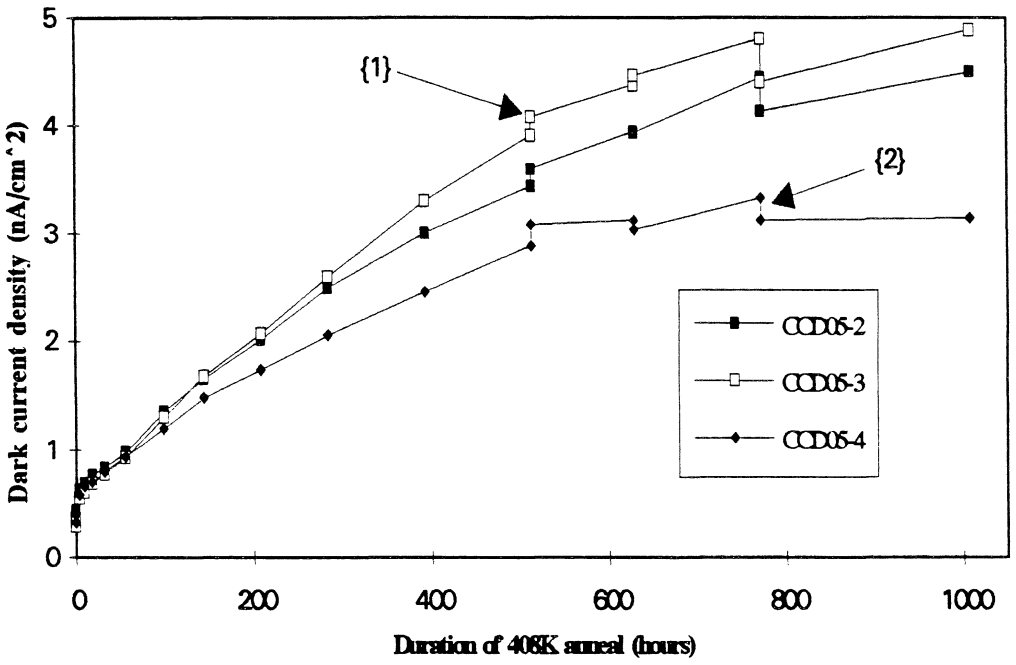


Fig 7.8. The clocked dark current (at 280K, V_{ss}=6V) of devices annealed at 408K, whilst unbiased. The discontinuity at {1} was caused by a 373K anneal which was carried out in an attempt to compare the rates of anneal at the two temperatures. The drop in dark current at {2} occured after a delay of 3 weeks between anneals, which suggests that there is a recovery process competing with the reverse annealing.

For these anneals all dark current measurements are quoted for 280K. This was necessary to restrict the dark current, and so prevent flooding of the potential wells. As can be seen from fig 7.8, the time dependent process has not saturated after 1000 hours at 408K, although the rate of the process has reduced considerably. The relative spread in device performance increases with accumulated

anneal time and it is possible that the process is close to exhaustion in CCD05-4.

Figures 7.9, and 7.10 show the temperature dependency of the time dependent process. It was found that the rate of the process was slowed down by a factor of 8 for anneals at 373K, and by a factor of 2.7 for anneals at 388K, both relative to the process at 408K.

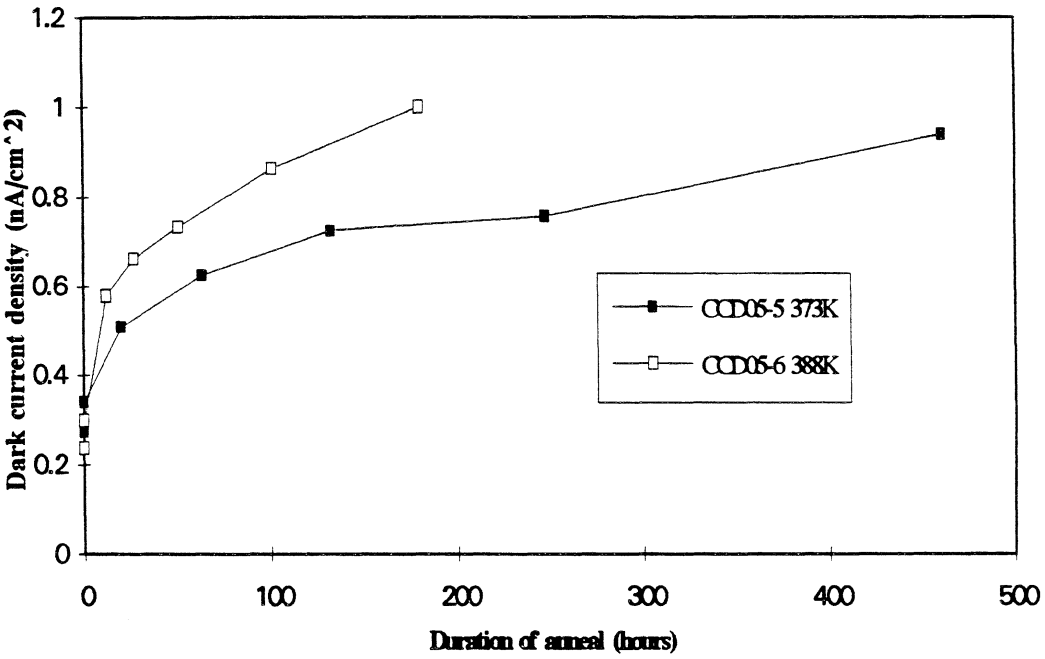


Fig 7.9. The clocked dark current (at 280K) of devices annealed, whilst unbiased, at 373K and 388K.

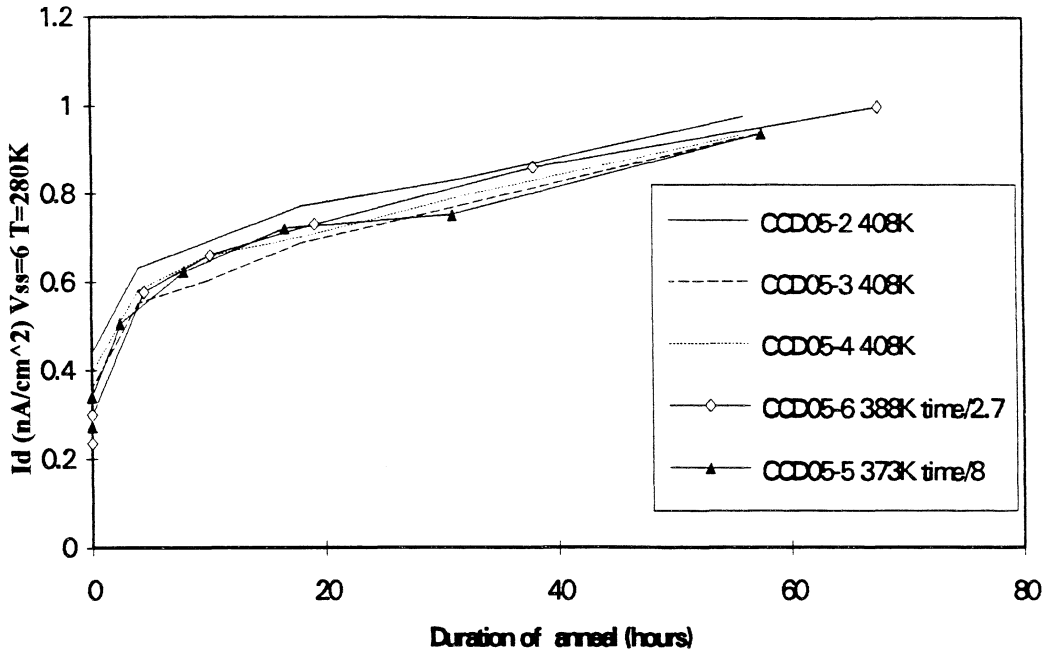


Fig 7.10. this plot shows that the dark current data taken from the devices annealed at 388K and 373K can be overlaid on the data taken from the devices annealed at 408K, if the time axes are changed by the correct factor. The factors are 2.7 and 8, for 388K and 373K respectively (devices were unbiased during anneal).

The effective activation energy of the time dependent process was derived (fig 7.11), and found to be 0.78eV, this compares with the value of 0.82eV quoted by Oldham et al [1], for the transport of H^+ in unbiased SiO_2 (see section 2.2.2.2.),and falls within the range 0.7 to 0.92eV, suggested by Hofstein [2], for H^+ transport in SiO_2 under a variety of conditions.

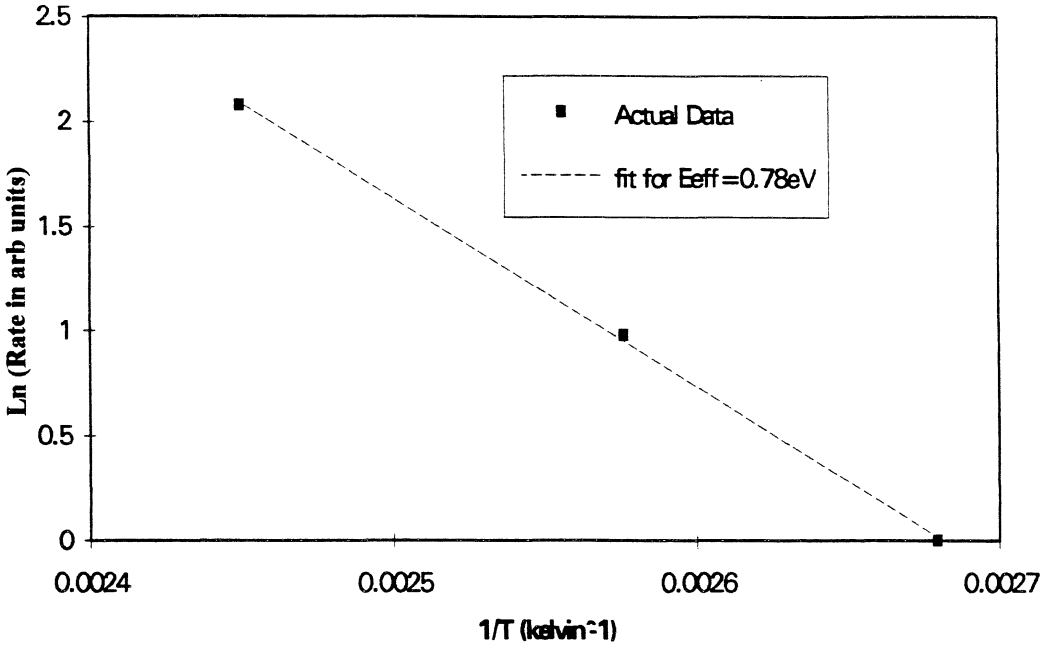


Fig 7.11 Derivation of the effective activation energy of the time dependent process.

7.3.2. Consideration of Scintillator Coatings, and Stepped Irradiations

The results quoted previously all apply to devices with conventional structures, irradiated to a large dose prior to annealing. Further anneals were required in order to test for any dependency of this process, upon scintillator coatings or differing irradiation regimes. To take account of the shorter anneal times, and hence lower dark current, these measurements were made at 290K.

One Gadox coated CCD05 and one conventional CCD05 were irradiated in steps of 2krad, upto a total of 10krad, with 15 hour, 408K anneals performed after each irradiation. In addition the CsI(Tl) coated CCD05, which had previously been irradiated to 5krad and then annealed at 408K to test for scintillator damge, was given further anneals at 408K. As shown in fig 7.12, the two devices initially irradiated to 2krad showed lower levels of dark current than those irradiated to the full 10krad, after 15 hours anneal. However this was due to the smaller prompt increase in dark current, immediately following irradiation. The actual increase in current caused by the anneal is of similar

magnitude. By the time the accumulated dose of these devices had reached 10krad, their dark current levels had reached those of the other devices. This suggests that the time dependent process is not a heavily dependent function of dose, at least for shorter anneal times, provided that the dose is above a certain level, which is less than 2krad. Once radiation produces a pool of hydrogen ions (see sections 2.2.2.2, 8.1, and 9.3.3) the transport to the Si/SiO_2 interface is limited by the interleaving medium. Thus the size of the pool is irrelevant unless the process is allowed to continue until the hydrogen is exhausted.

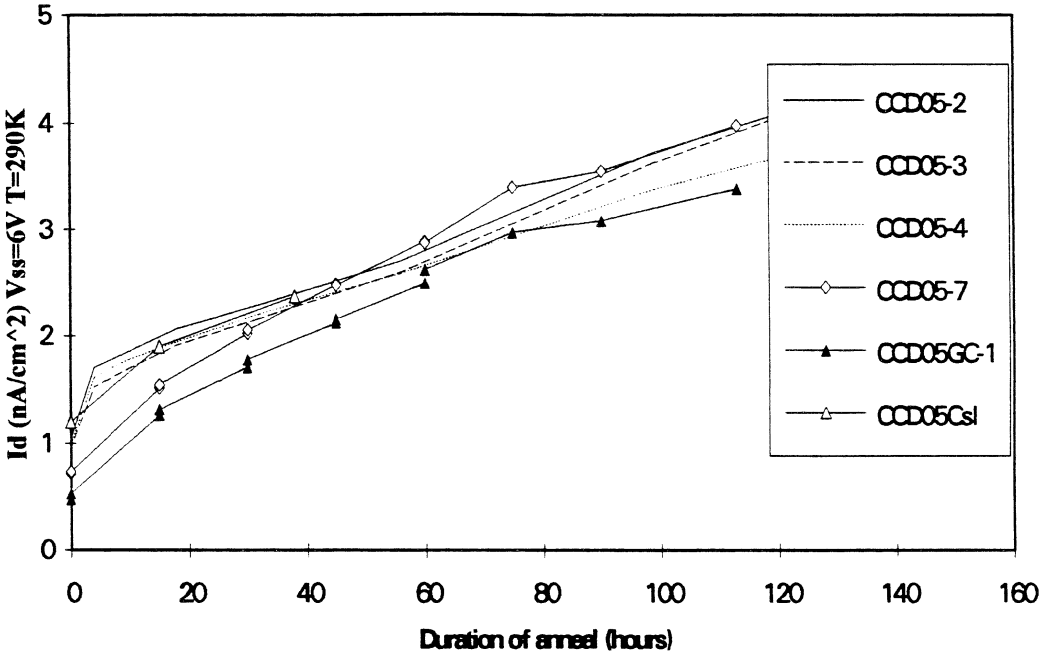


Fig 7.12. A plot comparing the time dependent process in devices irradiated to 10krad prior to annealing at 408K, with devices irradiated in steps. Devices CCD05-1,2, and 3, were irradiated to 10krad prior to annealing. The Gadox(Eu) coated device CCD05GC-1, and the control device CCD05-7, were irradiated in steps of 2krad alternated wuth 15 hour 408K anneals. After an accumulated dose of 10krad the devices were given a further 50 hours anneal. The CsI(Tl) device had previously been irradiated to 5krad and annealed at 408K to test for scintillator damage.

This result also suggests that the scintillator coatings make little or no difference to the time dependent increase in dark current. In the case of the CsI(Tl) coating this seems surprising given the large increase in prompt dark current which was observed. This may also be explained in terms

of the theory outlined above. If there is a large quantity of hydrogen in the oxide, originating from the polyimide layer, then it is plausible that the interaction between the radiation, and hydrogen close to the Si/SiO_2 interface will lead to the generation of many surface states, even with the oxide under a negative field (see chapter 8). However this extra hydrogen does not cause a corresponding enhancement of the time dependent process.

7.3.3. The Inversion Mode Device

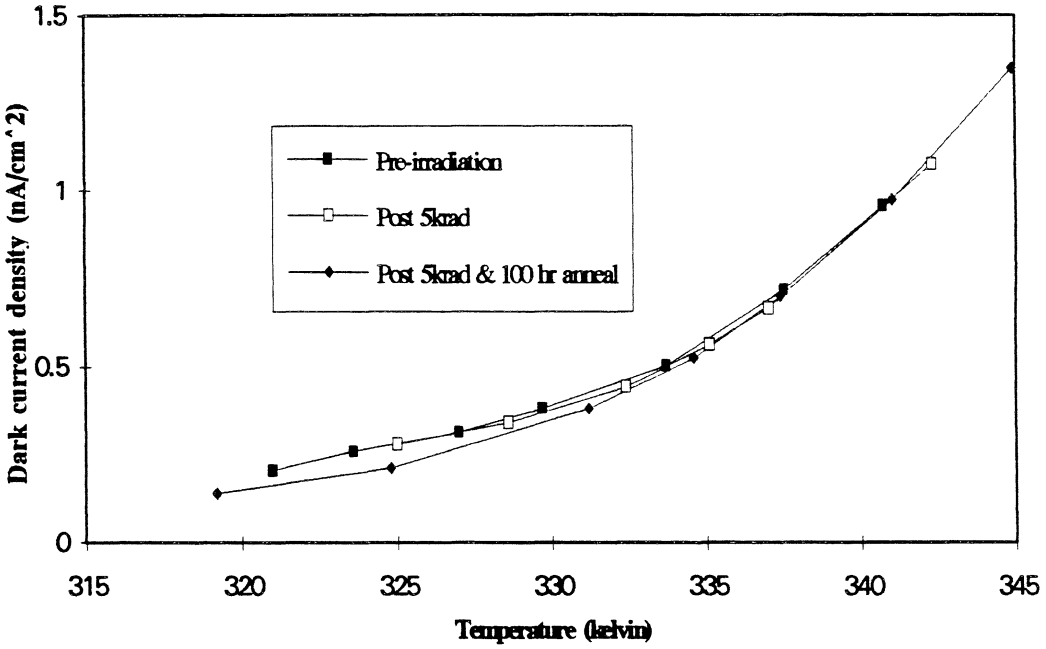


Fig 7.13. The clocked dark current from an inversion mode device CCD02IM-2, when operated in inversion.

The sensitivity of the dark current measurement was improved by operating the inversion mode at temperatures in excess of 320K. After a dose of 5krad, followed by a 100 hour anneal at 408K, no increase in dark current was seen.

References for Chapter 7

[1] T.R. Oldham, F.B. McLean, H.E. Boesch Jr, and J.M. McGarrity, "An Overview of Radiation -induced Interface Traps in MOS Structures", Semicond. Sci. Technol. Vol 4, 986-999, 1989.

[2] S.R. Hofstein, "Proton and Sodium Transport in SiO_2 Films", IEEE Trans. Electron. Dev., Vol 14, 11, 749-759, 1967.

Key to Symbols used in Chapter 8

$I_{d(n)}$	The dark current from depleted n-channel surfaces.
$I_{d(p)}$	The dark current from depleted p-stop surfaces.
$I_{d(n+p)}$	The combined dark current from both surfaces (= $I_{d(n)} + I_{d(p)}$).
$I_{d(p)}cl_{(m)}$	The dark current from the p-stop surfaces during conventionally biased clocking.
$I_{d}cl_{(m)}$	The total dark current during conventionally biased clocking.
$I_{d(n)}cl_{(h)}$	The dark current from the n-channel surfaces during clocking with the substrate bias in the high range (typically greater than 9V).
$I_{d(p)}cl_{(h)}$	The dark current from the p-stop surfaces during clocking with the substrate bias in the high range.
$I_{d}cl_{(h)}$	The total dark current during clocking with the substrate bias in the high range ($=I_{d(n)}cl_{(h)} + I_{d(p)}cl_{(h)}$).
$I_{d}cl_{(h)}(2V)$	The total dark current during clocking with the substrate bias in the high range, and the upper clock bias set at 2V.
σ_{es} and σ_{hs}	The capture cross-sections for electrons and holes at the surface.
$\lambda_{(t)}$	The fraction of steady state charge generation from an intermittently depleted surface, after the surface is depleted for time, t.
$\alpha_{(t)}$	The time average of $\lambda_{(t)}$, representing the dark current to be expected from an intermittently depleted surface as a fraction of the steady state dark current. Subscripts $_n$ and $_p$ denote the n-channel and p-stop surfaces respectively.
σ_{ns} and σ_{ps}	The goemetric mean of the capture cross-sections for both charge carriers, at the n-channel and p-stop surfaces respectively.
$d_{it}*_{(ns)}$	The effective density of states at the n-channel surface.
$d_{it}*_{(ps)}$	The effective density of states at the p-stop surface.

Reverse Annealing in the CCD

8.1 Electric Field Dependence of the Process

It was suspected that the principal cause of the reverse annealing process was the transport of a positively charged particle from the gate oxide layer to the Si/SiO_2 interface (section 2.2.2.2.). In order to test for this, the electric field dependence of the process was investigated. Figure 8.1 shows the direction of the suspected ion transport in the oxide, and the convention for the sign of the oxide field. It can be seen that if the H^+ ion is responsible for the reverse annealing process, then the process will be inhibited by a negative (conventional bias) oxide field, and enhanced by a positive one.

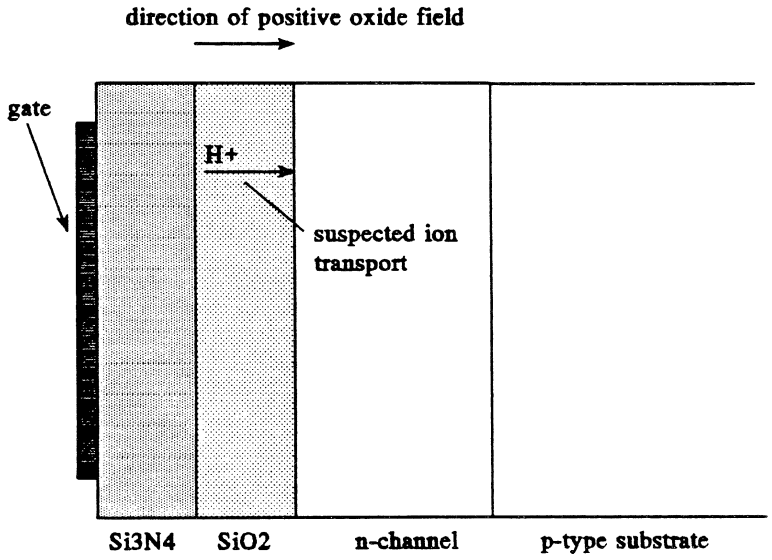


Figure 8.1. This shows the direction of the suspected ion transport, and the convention for a positive oxide field. It can be seen that a negative oxide field will inhibit the process if as suspected, a positively charged particle is responsible.

Figure 8.2 shows the dark current increase with time, of two CCD02s which were irradiated to 5krad and then annealed at 100°C. One device was annealed unbiased, with all connections shorted together. The other device was annealed under conventional bias conditions, where the oxide field is about -3 x $10^5 Vcm^{-1}$.

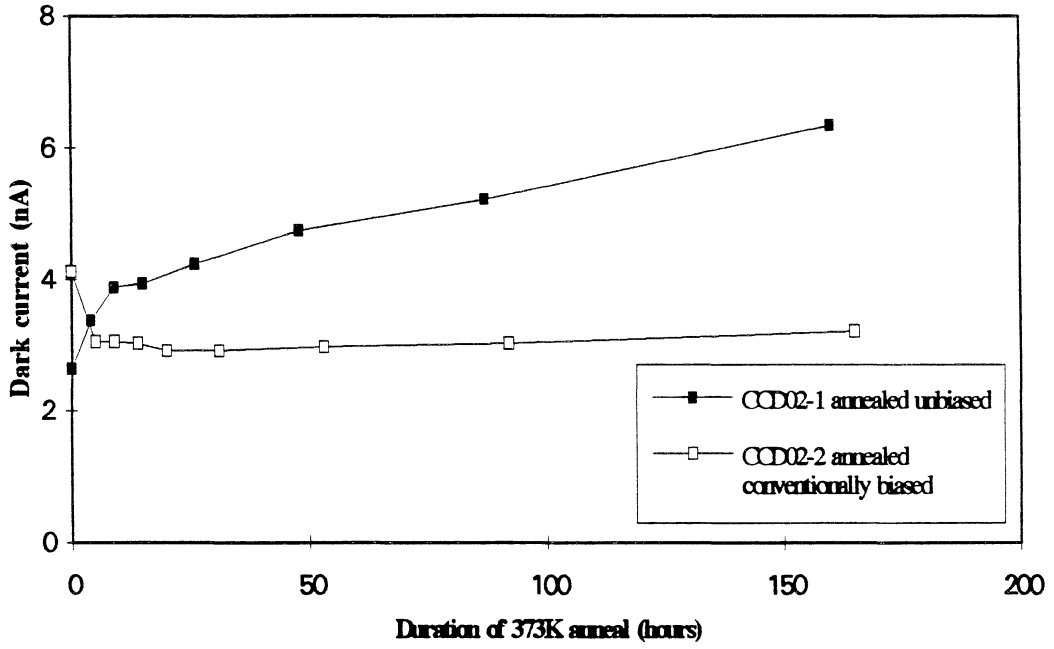


Fig 8.2. The dark current (at 300K, V_{SS}=6V) of CCD02-1, annealed unbiased, and CCD02-2 annealed under conventional bias conditions. Both devices were irradiated to 5krad prior to anneal.

The device annealed whilst unbiased showed a continuous increase in dark current with anneal. The total anneal induced increase reaching about 4nA, after 150 hours. For the device annealed whilst conventionally biased, the dark current actually fell initially, although after about 5 hours it stabilised and little further change was seen. The initial drop in dark current is not understood, and would need to be reproduced in other devices in order to be confirmed as a consequence of the annealing, rather than an artefact of the individual device. It is evident though, that any reverse annealing which takes place is on a far smaller scale than that seen for the device annealed whilst unbiased, and that the negative oxide field does inhibit the process.

Figure 8.3. shows the reverse annealing progress of a CCD02 annealed for 24 hours whilst conventionally biased, then for 24 hours unbiased, and then finally with a positive oxide field of

around 8 x $10^5 Vcm^{-1}$. This device was actually an inversion mode device CCD02IM-1, with the positive oxide field applied to test whether a dark current increase could be induced under any circumstances. However the dark current was also measured with the device operating out of inversion mode where device behaviour is similar to that of a conventional device, and it is these measurements which are shown.

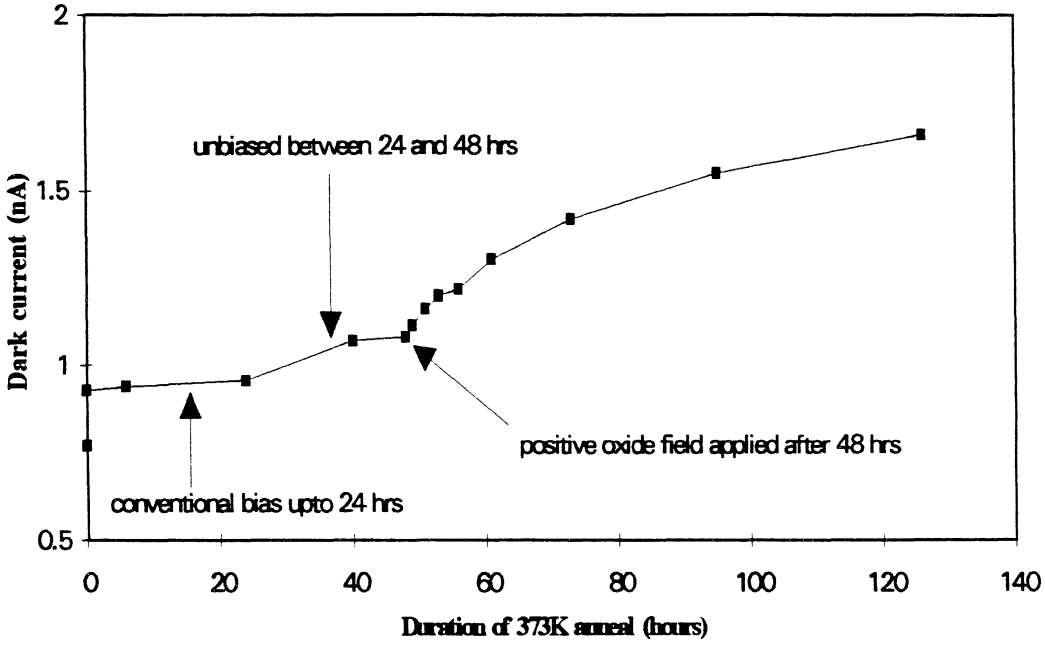


Fig 8.3. The increase in dark current of a CCD02 device annealed at 373K. For the first 24 hours the device was annealed whilst biased conventionally, for the next 24 hours unbiased, and from then on a positive oxide field was contrived. It can be seen that the conventional field inhibits the reverse annealing, whilst the positive oxide field enhances it. The dark current is shown for an operating temperature of 300K, with V_{ss}=6V.

8.2. Reverse Annealing in Unirradiated Devices

Two CCD02s were annealed unirradiated in order to determine whether device irradiation is a pre-requisite for the reverse annealing process. One was annealed unbiased, and the other was annealed

with a positive oxide field in order to accelerate any reverse annealing which may take place.

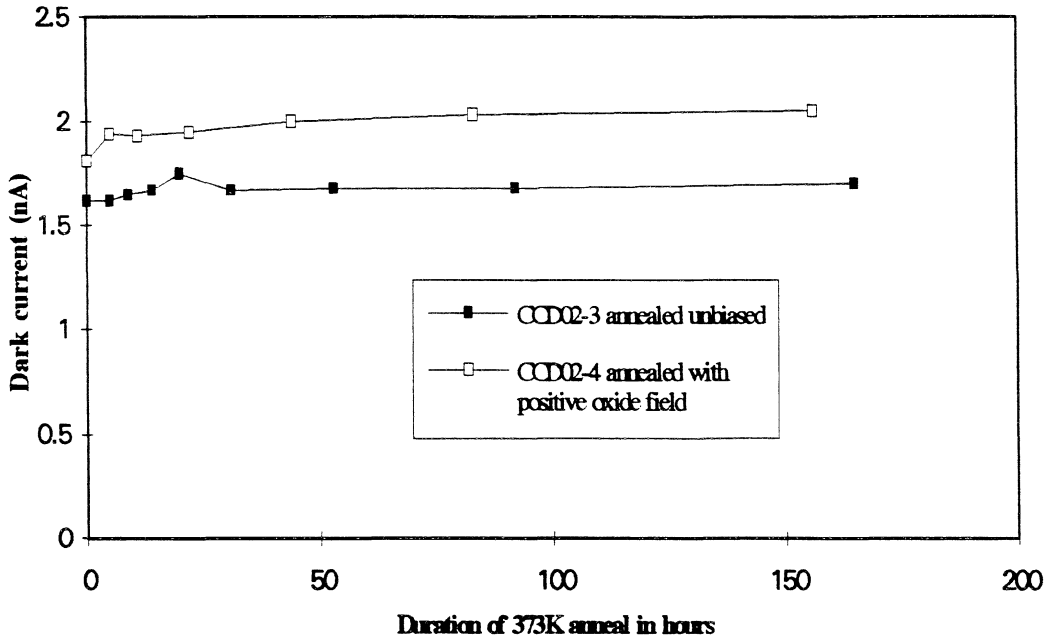


Fig 8.4. Annealing of unirradiated devices (dark current measured at 300K, with V_{SS}=6V).

As shown in fig 8.4, there was no significant reverse annealing in either of the unirradiated devices. This supports the hypothesis (see section 7.3.2.) that radiation is necessary to free hydrogen in the oxide layer before the process can begin.

8.3. The Source of the Anneal Induced Dark Current

The operation of the inversion mode CCD02s (section 1.3), and the very low dark current levels observed, show that almost all of the dark current in an unirradiated conventional CCD02 or CCD05 is generated by states at the Si/SiO_2 interfaces. Also it is known that 70kVp x-rays do not carry sufficient energy to cause bulk defects in the silicon lattice (section 2.1.2.2.). Therefore, for the irradiations and anneals described here, all dark current increases are caused by these interface states. There are however two Si/SiO_2 interfaces to be considered, the interface between the n-channel and the gate oxide, and the interface between the p-stop and the gate oxide. (see fig 5.2)

In order to discriminate between charge generation from the p-stop surface, and charge generation from the n-channel surface it is necessary to measure the dark current from the device as a function of substrate bias [1].

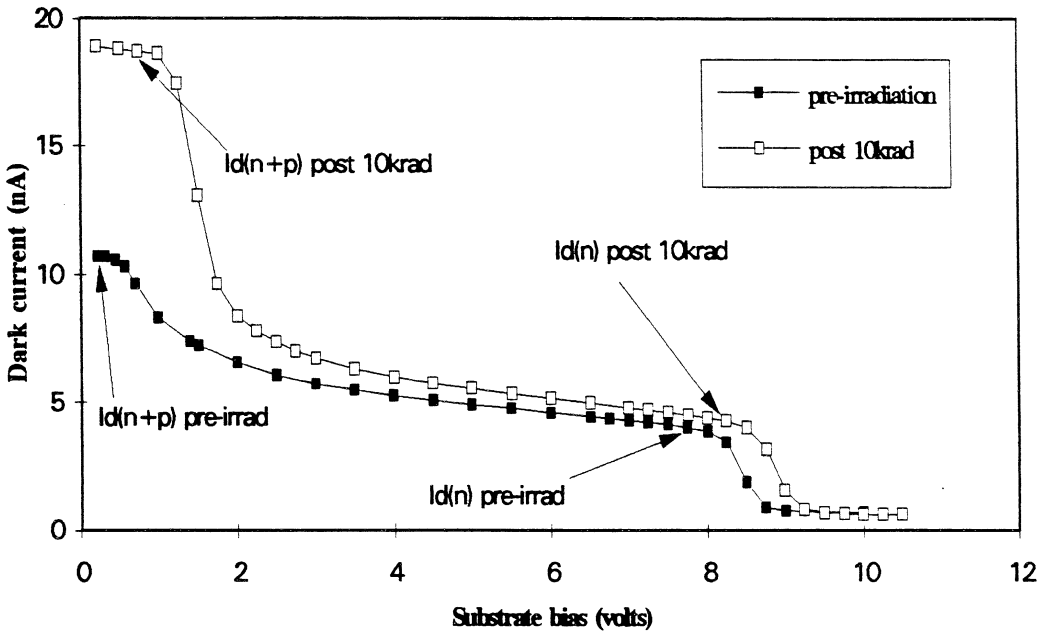


Fig 8.5 The static dark current (at 300K) from a CCD05, before and after 10krad irradiation. Where $I_{d(n)}$ is the dark current from the n-channel surfaces, and $I_{d(n+p)}$ is the combined dark current from the n-channel and p-stop surfaces (device powered during irradiation).

Fig 8.5 shows the static dark current from a CCD05 as a function of substrate bias. $I_{d(n)}$ is the dark current from the device when the n-channel surface is depleted, but the p-stop surface is accumulated, and so corresponds to dark current generation by states at the n-channel surface. $I_{d(n+p)}$ is the dark current from the device when both the n-channel and p-stop surfaces are depleted and so corresponds to dark current generation by the states at both surfaces.

8.3.1. $I_{d(n)}$ and $I_{d(p)}$ as a function of Annealing

Measurement of $I_{d(n)}$ and $I_{d(n+p)}$ allows the relative dark current contributions from the n-channel and p-stop surfaces to be determined for the case where they are depleted. Although the precise

implications for an operational device depend upon the electrical state of the device, in terms of depleted and undepleted surfaces (see section 8.3.2), monitoring of these values at each anneal stage gives information regarding the locality of the interface state buildup. Figure 8.6 shows the increase in $I_{d(n)}$ and $I_{d(p)}$ (where $I_{d(p)} = I_{d(p+n)} - I_{d(n)}$), of device CCD05-8, annealed at 373K.

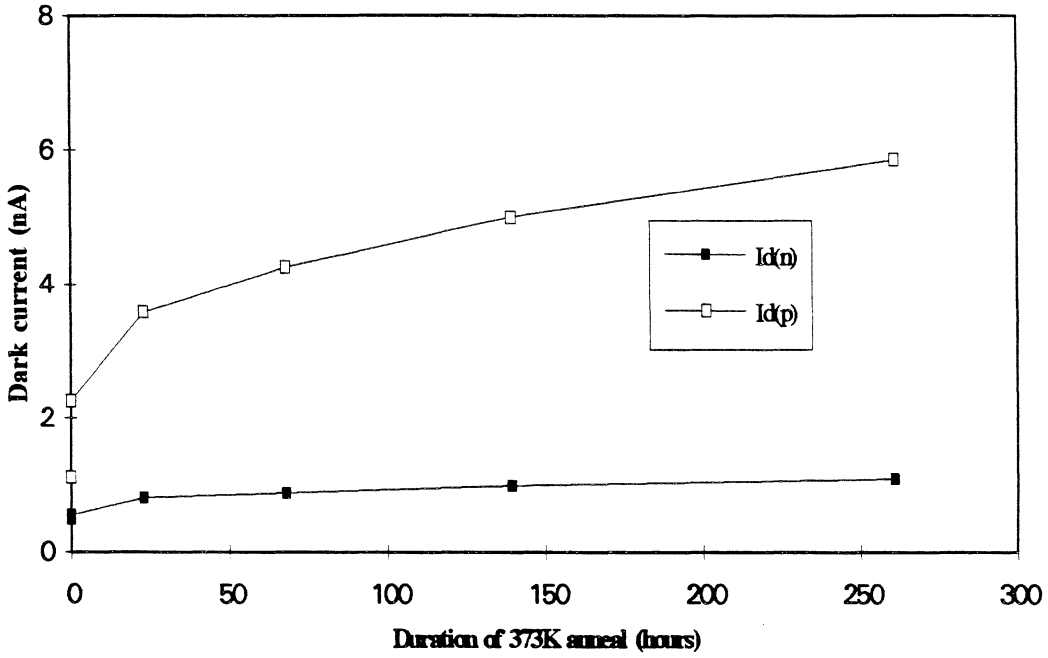


Fig 8.6 This shows the increase in $I_{d(n)}$ and $I_{d(p)}$ for device CCD05-8, annealed at 373K. Current measurements are for 280K.

As can be seen, whilst the n-type surfaces account for a significant proportion, (around 30%) of the dark current generation from the unirradiated device, almost all of the irradiation and anneal induced dark current originates from the p-stop surfaces.

Previous to the measurements taken for CCD05-8, a similar treatment was performed on device CCD05-6 (except for the anneal temperature of 388K). At this time the CCD05 board was was not prepared for static biasing of devices, so the static scenario was simulated by reducing the upper clock gate bias to 2V, rather than the 10V used conventionally (see fig 8.7).

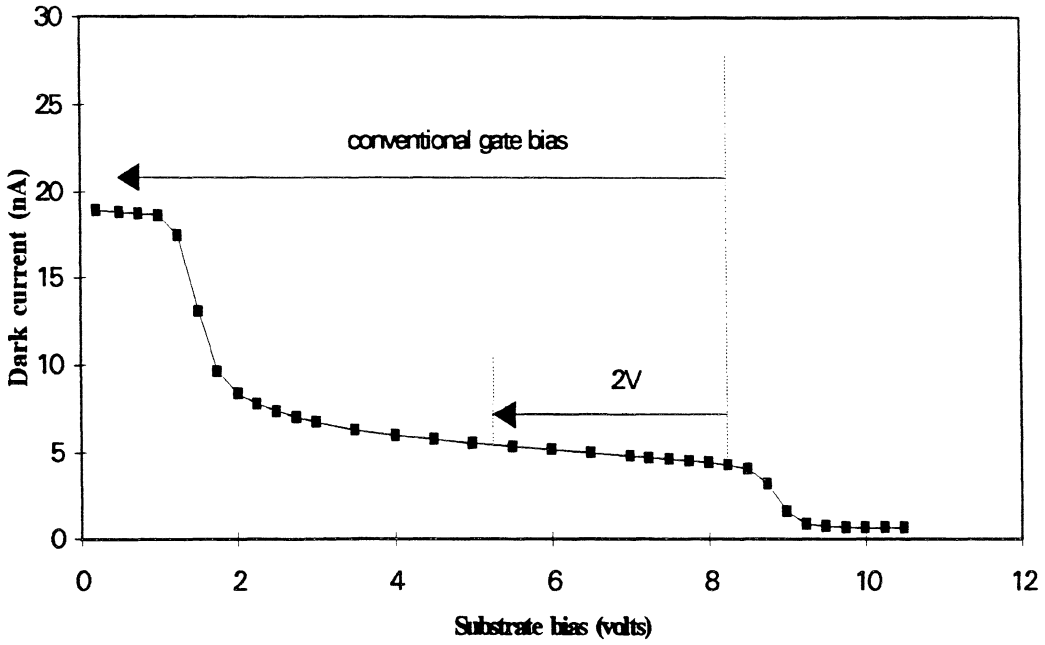


Fig 8.7. This plot shows how reducing the gate bias sufficiently, approximates to the static case. In a conventionally clocked device the gate bias effectively shifts the operation of a capacitor from the medium voltage case where the p-stop surfaces are accumultaed, to the low voltage case where they are depleted. With the upper clock gate bias set at 2V, only a small fraction of the p-stop surface is depleted (see chapter 5) and this can be corrected for.

Using a gate voltage of this size ensures that at no time do any of the p-stop surfaces become fully depleted, as would happen for the conventional gate bias (see fig 8.7, and discussion in section 8.3.2.) This does significantly reduce the charge carrying capacity of the pixel potential wells, so care was taken to ensure to see that this capacity was not exceeded. It was not possible to eliminate the leakage current with the measurements taken for this device, but from the measurements made for CCD05-8, leakage is thought to be less than 0.5nA at 300K. Because of the approximations used for this device, the dark current levels are likely to be overestimated by a few percent. However the findings do support the observations made from device CCD05-8, in the respect that nearly all the radiation and anneal induced dark current originates from the p-stop surfaces, as shown in fig 8.8.

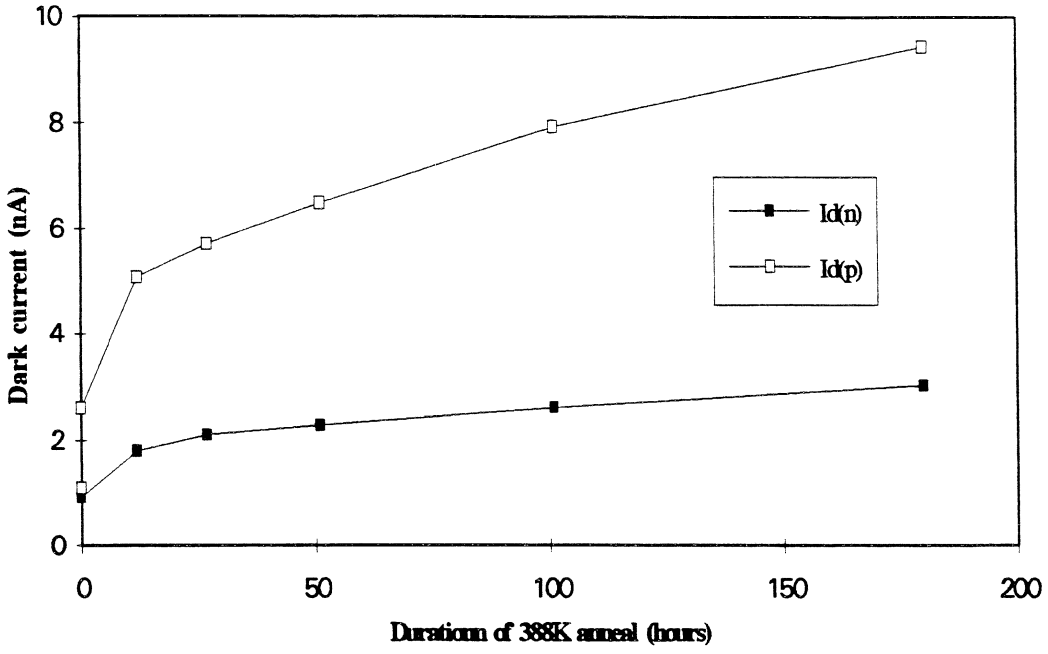


Fig 8.8. This shows the increase in $I_{d(n)}$ and $I_{d(p)}$ for CCD05-6, annealed at 388K. Current measurements are for 280K..

8.3.2 Relating the Increase in $I_{d(n)}$ and $I_{d(p)}$ to the Operation of a Clocked Device

$I_{d(n)}$ and $I_{d(p)}$ are the levels of dark current from the n-channel and p-stop surfaces respectively, for the case where they are depleted. When a device is clocked, however, depending upon the biasing conditions, and the clocking sequence used, the surfaces may be depleted, undepleted, or intermittently depleted [1].

8.3.2.1 Conventional Clocking

Typical biasing conditions for the conventional mode CCD02 and CCD05, are a substrate bias in the medium range (3-8V in fig 8.7), a lower clock gate bias of 0V, and an upper clock gate bias of

10V. The clocking sequence used for these devices means that during imaging time one third of the pixel capacitors have the gate held at the high bias, and two thirds have the gate held at the low bias. (fig 8.9)

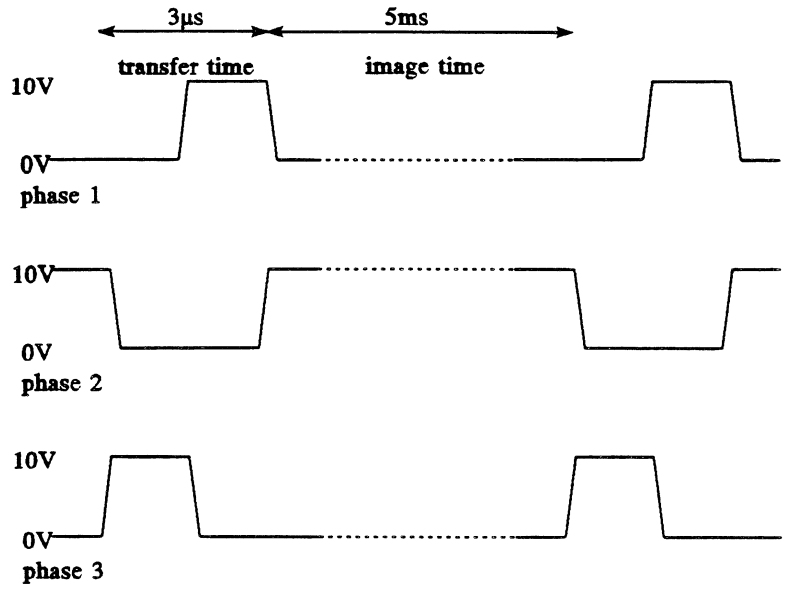


Fig 8.9. A typical clocking sequence for the conventional device, with phase 2 gates held high throughout the imaging time.

The n-channel surfaces are all permanently depleted due to the substrate bias, and therefore $I_{d(n)}$ will be the contribution from this source. As far as the p-stop surfaces are concerned, there will be depletion edges at the p-stop surface close to the n-channel caused by the reverse biased p-n junction between regions (as described in chapter 5), causing a small fraction of the area to be depleted. In addition to this those p-stop surfaces under phase 2 gates will be intermittently depleted for 5ms at a time. The dark current from the p-stop surfaces is therefore given by;

$$I_{d(p)}cl_{(m)} = (1-\gamma)\times\alpha_{p(T)}\times\frac{I_{d(p)}}{3}+\gamma\times I_{d(p)}$$

where $I_{d(p)}cl_{(m)}$ is the dark current from the p-stop surfaces during conventionally biased clocking (i.e. in the medium range of substrate bias), and α_p is a temperature dependent fraction between 0 and 1, relating the dark current from an intermittently depleted surface with the equilibrium dark current from a permanently depleted surface (see sections 2.3.2.2. & 8.3.3.). γ is the fraction of the

p-stop surface falling within the depletion edges, and is a function of the substrate bias. Although it would be possible to estimate this value if the means to carry out a 3-dimensional solution of Poisson's equation were available, generally it will be necessary to determine this value experimentally as shown in fig 8.11.

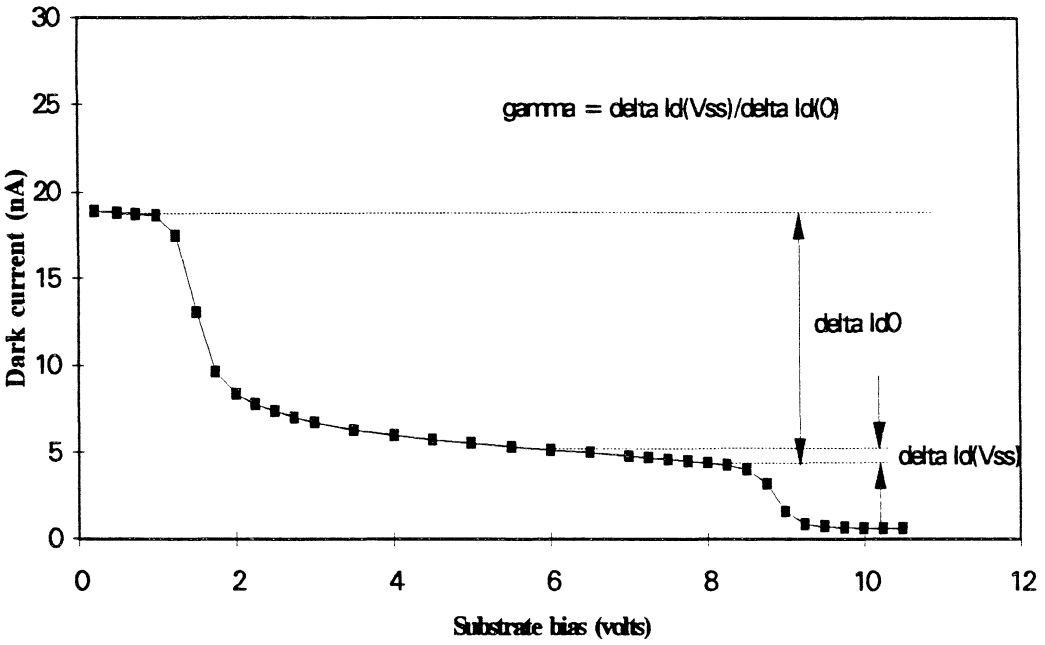


Fig 8.11. Experimental determination of γ is for a given substrate bias.

the total dark current $I_dcl_{(m)}$, is therefore given by;

$$I_dcl_{(m)} = I_{d(n)} + (1-\gamma)\times \alpha_{p(T)} \times \frac{I_{d(p)}}{3} + \gamma \times I_{d(p)}$$

If the device is operated close to the threshold of inversion of the n-channel surface (around 8V in fig 8.11) then γ approaches zero and so the total dark current, as in [1], is given by;

$$I_dcl_{(m)} \approx I_{d(n)} + \alpha_{p(T)} \times \frac{I_{d(p)}}{3} \qquad (8.1)$$

8.3.2.2. Conventional Device Operated in Inversion

If the device is operated at a high substrate bias (>9V for fig 8.7) such that the n-channel surfaces are inverted for a gate bias of 0V, then there will be no contribution from either of the surfaces under the phase 1 and phase 3 gates. The dark current will all originate from the surfaces under the phase 2 gates, as a result of the intermittent depletion caused by the gate bias. The dark current from the n-channel surface is therefore given by;

$$I_{d(n)}cl_{(h)} = \alpha_{n(T)} \times \frac{I_{d(n)}}{3}$$

where α_n is n-channel surface equivalent of α_p.

with the dark current from the p-stop surfaces given by;

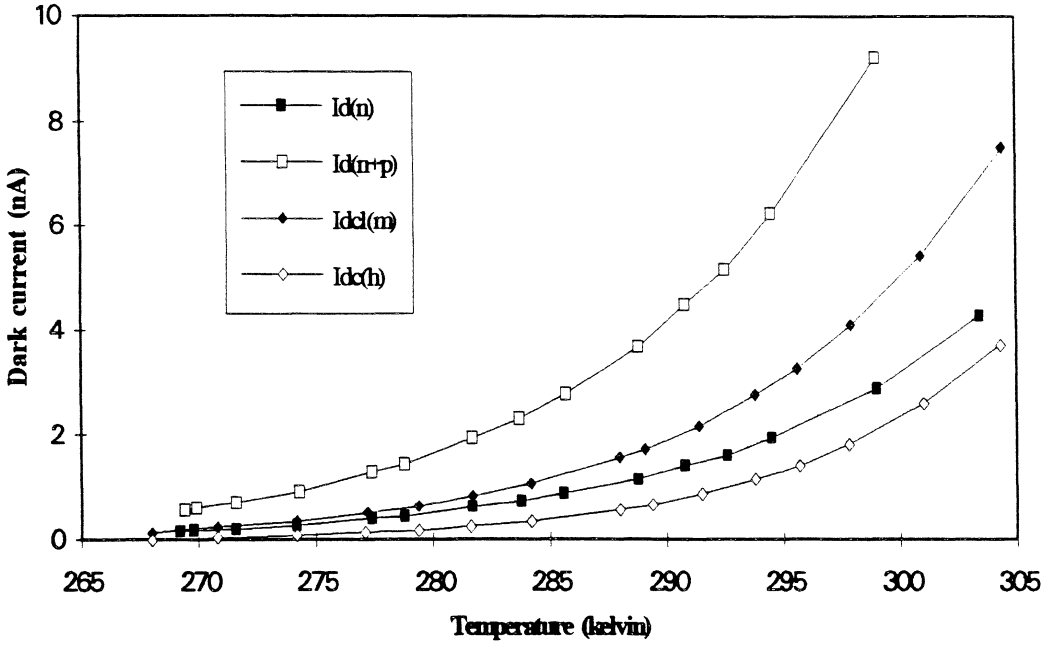
$$I_{d(p)}cl_{(h)} = \alpha_{p(T)} \times \frac{I_{d(p)}}{3}$$

and the total clocked dark current, $I_d cl_{(h)}$,is given by [1];

$$I_d cl_{(h)} = \alpha_{n(T)} \frac{I_{d(n)}}{3} + \alpha_{p(T)} \frac{I_{d(p)}}{3} \qquad (8.2)$$

8.3.2.3. Comparison Between Measured Clocked Dark Current, and Static Dark Current

Fig 8.12 shows the clocked and static dark currents of the CCD05 as a function of temperature, both for the case of an unirradiated device, and for the case of a device irradiated to 10krad (whilst powered) and then annealed (whilst unbiased) at 373K for 570 hours.



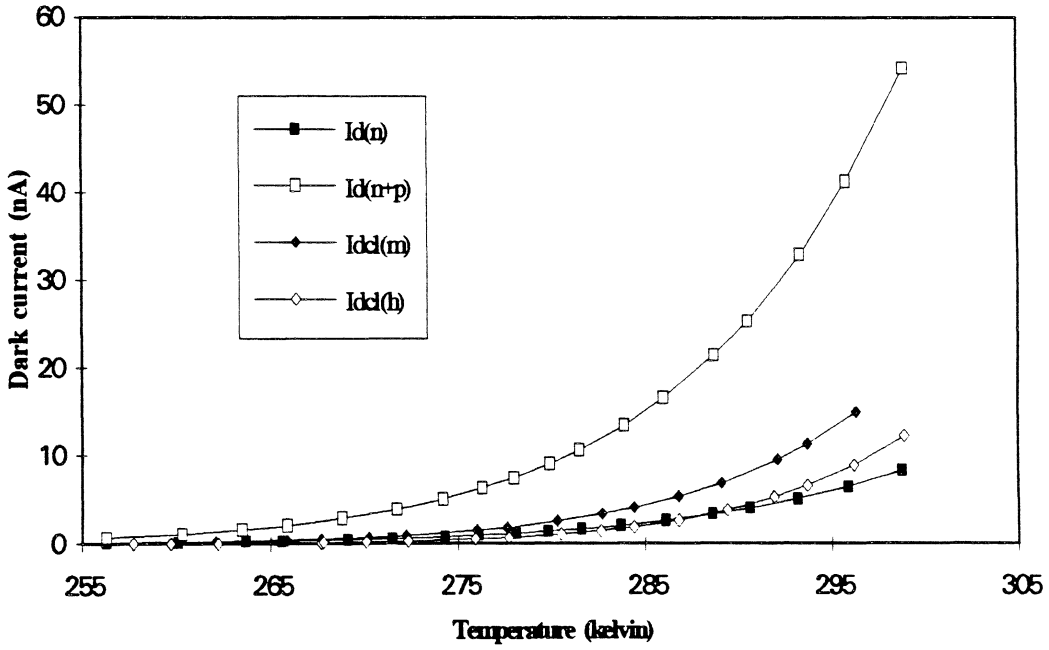


Fig 8.12. Comparison between the clocked dark current and the static dark current for CCD05-8, a) when unirradiated , and b) when irradiated to 10krad (whilst powered), and then annealed for 570 hours at 373K, whilst unbiased).

For conventional device operation, the contribution from the p-stop surfaces increases as a fraction of the total dark current, following irradiation (0.37 to 0.5 at 290K). This fraction, which is dependent upon operating temperature, remains approximately constant throughout the anneals at around 0.5 (see fig 8.13). Thus although the increase in $I_{d(p)}$ is far greater than the increase in $I_{d(n)}$, because of the permanent depletion of all the n-channel surfaces, the dark current contribution here remains a similar size to that from the p-stop surfaces.

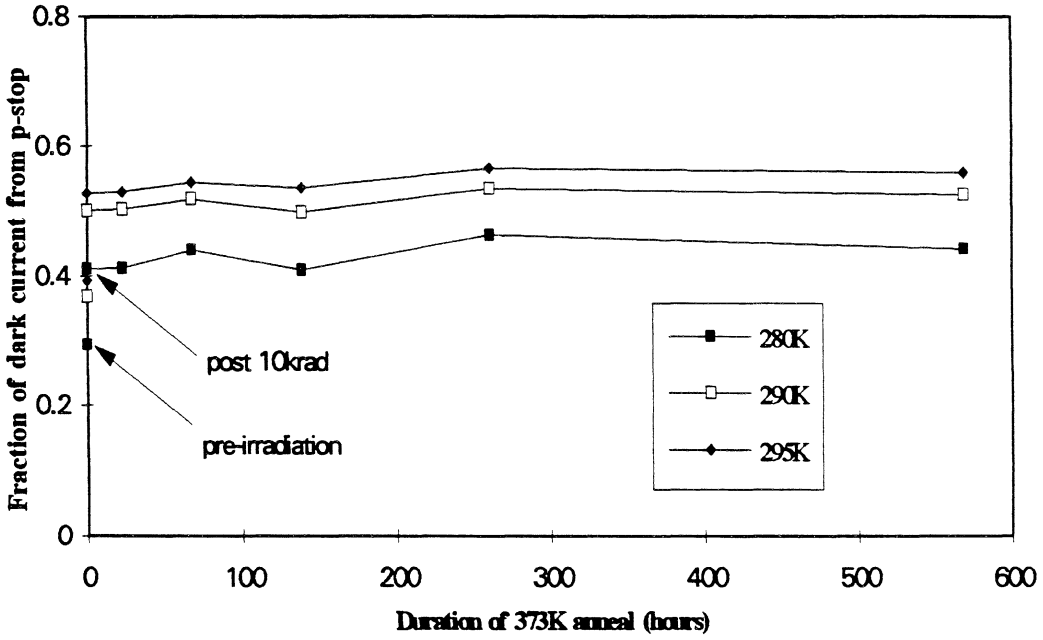


Fig 8.13. This plot shows the fraction of dark current originating from the p-stop surfaces for CCD05-8, operated with conventional bias and clocking. Three operating temperatures are shown.

8.4. Buildup of Interface States

The dark current from a depleted surface is related to the density of states as [1,2];

$$J_{DS}=0.5\times q\pi KTn_i v_{th}\sqrt{(\sigma_{es}\sigma_{hs})}D_{it}^{*} \qquad (8.3)$$

where J_{DS} is the dark current density, (A/cm^2),

q is the electronic charge = $1.602 \times 10^{-19}C$,

K is Boltzmann's constant = 8.617×10^{-5} eV/K

T is the temperature in kelvin,

n_i is the intrinsic carrier concentration, $(3.1\text{-}3.88) \times 10^{16} \times T^{1.5} \times \exp(-7000/T)$ cm^{-3}. [3,4]

v_{th} is the thermal velocity $\approx 1 \times 10^7 \times (T/300)^{0.5}$ cms^{-1} [1,2],

σ_{es} and σ_{hs} are the capture cross-sections for electrons and holes at the surface in cm^2,

D_{it}^* is the average interface state density close to E_m (see section 2.3.2.2.) in $cm^{-2}eV^{-1}$

All of the terms in equation 8.3 are known, except for the capture cross-sections of the two surfaces, and the interface state densities. Therefore, if the temperature dependence of $I_{d(n)}$ and $I_{d(p)}$ are known, the product of $(\sigma_{es}\sigma_{hs})^{0.5}$ and D_{it}^* be determined. This product will be referred to as σD_{it}^*.

8.4.1. Determination of σD_{it}^* for the n-channel Surface.

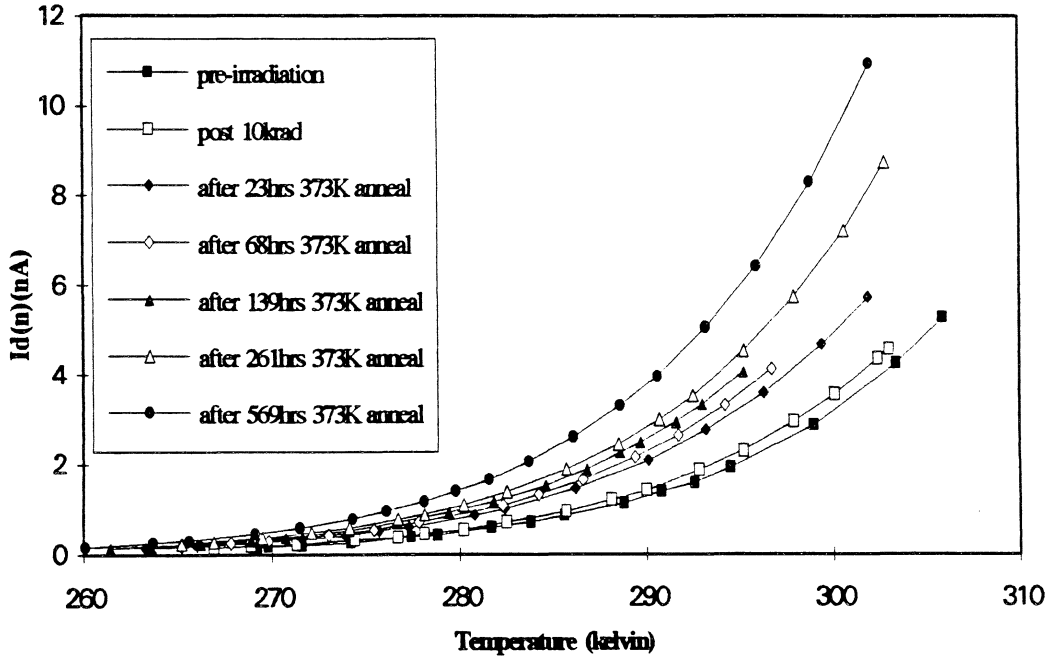


Fig 8.14. This shows the temperature dependence of $I_{d(n)}$ for CCD05-8, at various anneal stages (all anneals with device unbiased).

The temperature dependence of $I_{d(n)}$ at each stage of anneal is shown in fig 8.14. In order to ascertain the value of σD_{it}^{*} at each stage, the measured data was fitted to equation 8.3. The results which are subject to a systematic error of 11% due to the uncertainty in intrinsic carrier concentration, are shown along with statistical error below.

Irradiation and anneal history	$\sigma D_{it\ (ns)}^{*}$ (eV^{-1})
	systematic error = ± 11%
pre-irradiation	(1.268 ± 0.005) x 10^{-6}
post 10krad	(1.413 ± 0.004) x 10^{-6}
after 23hrs 373K anneal	(1.956 ± 0.013) x 10^{-6}
after 68hrs 373K anneal	(2.222 ± 0.009) x 10^{-6}
after 139hrs 373K anneal	(2.503 ± 0.008) x 10^{-6}
after 261hrs 373K anneal	(2.745 ± 0.007) x 10^{-6}
after 569hrs 373K anneal	(3.693 ± 0.007) x 10^{-6}

8.4.2. Determination of σD_{it}^{*} for the p-stop Surface

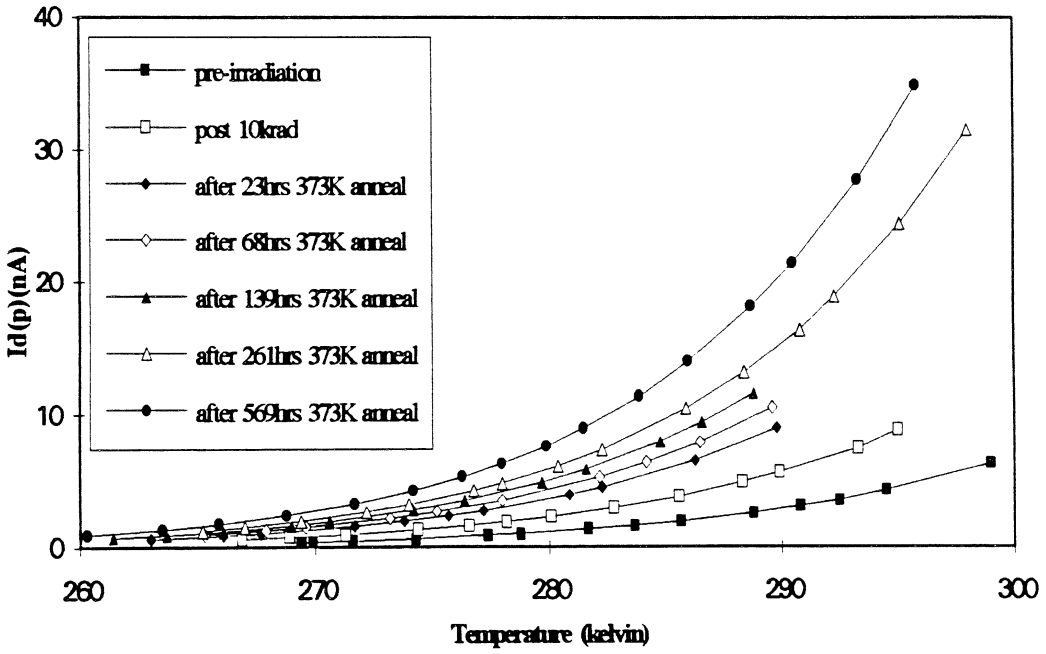


Fig 8.15. This shows the temperature dependence of $I_{d(p)}$ for CCD05-8, at various stages of anneal (all anneals with device unbiased).

The temperature dependence of $I_{d(p)}$ at each anneal stage is shown in fig 8.15. $I_{d(p)}$ could not be measured directly, but was calculated by subtracting $I_{d(n)}$ from $I_{d(n+p)}$. As for $I_{d(n)}$ the data was fitted to equation 8.3, in order to calculate the values of σD_{it}^{*} at each anneal stage. These are shown in the table below.

Irradiation and anneal history	$\sigma D_{it}^{*}{}_{(ps)}$ (eV^{-1})
	systematic error = ± 11%
pre-irradiation	$(4.980 \pm 0.03) \times 10^{-6}$
post 10krad	$(9.885 \pm 0.08) \times 10^{-6}$
after 23hrs 373K anneal	$(1.637 \pm 0.006) \times 10^{-5}$
after 68hrs 373K anneal	$(1.957 \pm 0.006) \times 10^{-5}$
after 139hrs 373K anneal	$(2.332 \pm 0.005) \times 10^{-5}$
after 261hrs 373K anneal	$(2.718 \pm 0.004) \times 10^{-5}$
after 569hrs 373K anneal	$(3.672 \pm 0.004) \times 10^{-5}$

Table 1. σD_{it}^{*} as a function of anneal for CCD05-8 (all anneals with device unbiased).

8.4.3. Determination of the Capture Cross-sections

As can be seen from equation 8.3, before the density of interface states can be determined it is first necessary to calculate the geometric mean of the appropriate capture cross-sections (σ). Roy [1] showed that this could be done by comparison of the clocked and static dark currents from a device.

The time dependent dark current from a surface which changes from the undepleted state to the depleted state, as occurs during clocking, is related to the equilibrium dark current by equation 8.4 (see section 2.3.2.2).

$$\lambda_{(T)} \equiv \frac{J_{DS}(t)}{J_{DS}(\infty)} = \frac{2}{\pi}\int_0^{\infty} \exp[-(X+X^{-1})\frac{t}{\tau}]\frac{dX}{(1+X^2)} \qquad (8.4)$$

where t is the time which has lapsed since surface depletion, and τ is given by;

$$\tau = (n_i v_{th} \sqrt{\sigma_{es} \sigma_{hs}})^{-1}$$

by solving this integral numerically for different values of $\sigma (= (\sigma_{es}\sigma_{hs})^{0.5})$, and then comparing the predicted clocked dark currents with those actually observed for CCD05-8, the geometric mean of the capture cross-sections is estimated.

From 8.3.2. we have that $I_d cl_{(m)}$, the clocked dark current for the medium range of substrate bias (close to the onset of inversion) is given by;

$$I_d cl_{(m)} = I_{d(n)} + \alpha_{p(T)} \times \frac{I_{d(p)}}{3} \qquad [(8.1) see\ p143]$$

which allows experimental determination of α_p as a function of temperature.

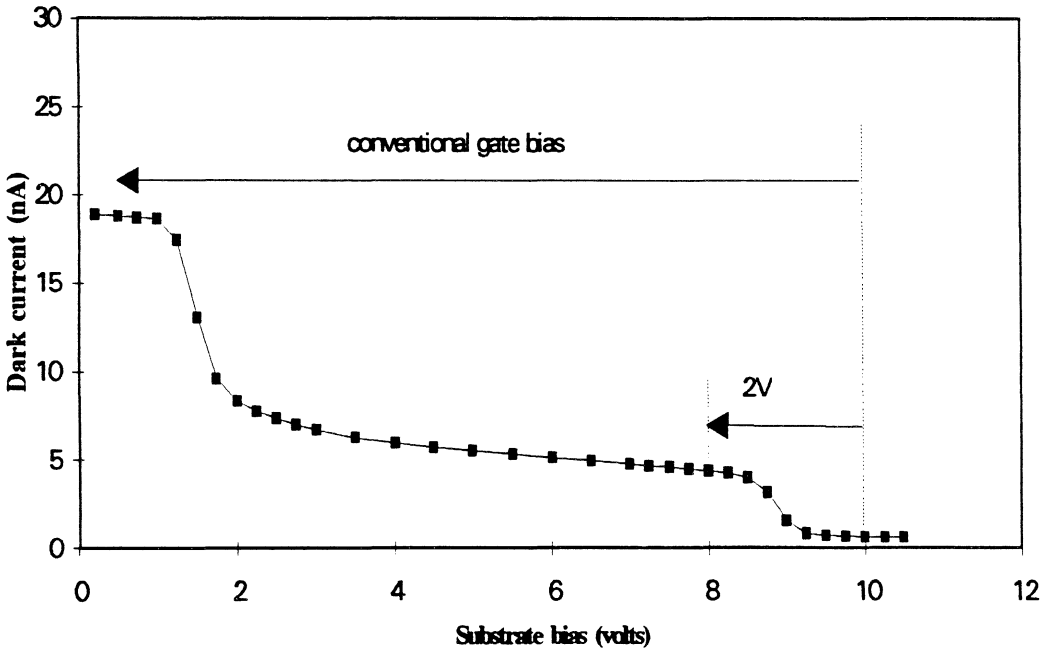


Fig 8.16. This shows that if the upper clock gate bias is reduced sufficiently, then only the n-channel surfaces are intermittently depleted by the high gate bias.

$I_d cl_{(h)}$, the clocked dark current for the high range of substrate bias is a function of both $\alpha_{n(T)}$ and $\alpha_{p(T)}$ (see equation 8.2), so use of this parameter to calculate $\alpha_{n(T)}$ would subject the measurement to an unnecessarily large error. Instead the dark current was measured with the substrate bias in the high range, but the high gate bias set at only 2V. (see fig 8.16) Operating the device in this way ensures that only the the n-channel surfaces are depleted by application of the high gate bias, and allows $\alpha_{n(T)}$ to be experimentally determined. The dark current now measured, $I_d cl_{(h)}(2V)$, is given by;

$$I_d cl_{(h)}(2V) = \alpha_{n(T)} \times \frac{I_{d(n)}}{3} \qquad (8.5)$$

8.4.3.1. Theoretical Calculation of α

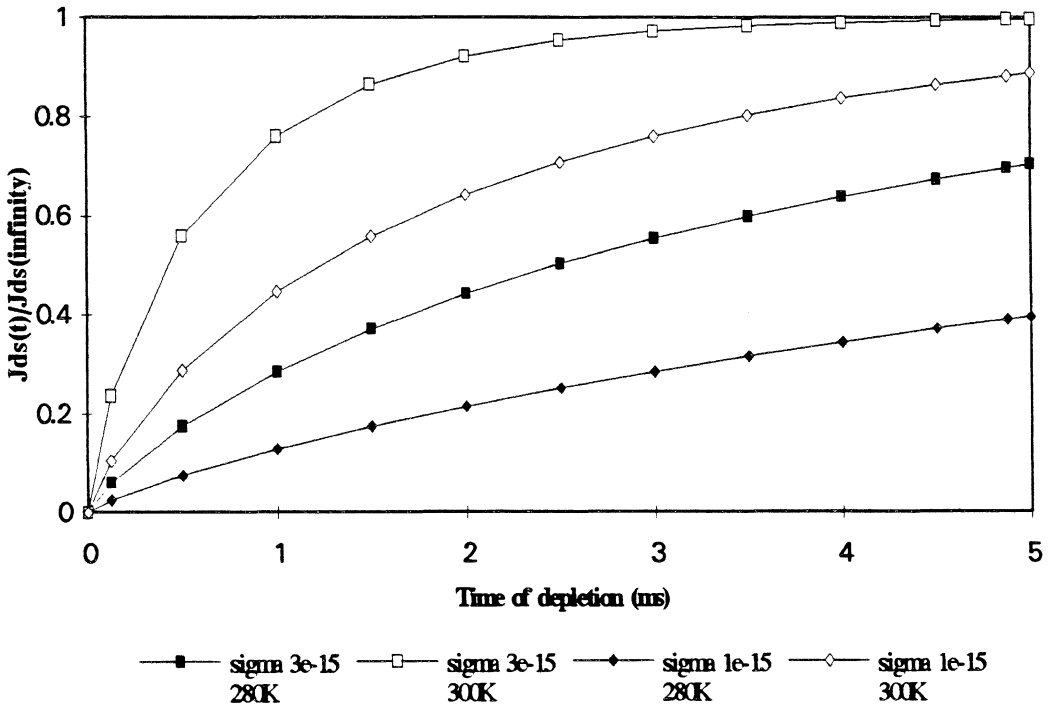


Fig 8.17. This shows λ as a function of time, for two values of temperature, and σ. The data was obtained by numerical solution of equation 8.4. The units of σ are cm^2

For an intermittently depleted surface the dark current generation is periodically quenched as the

surface goes out of depletion. Each time the surface is re-depleted the generation begins again. To predict the value of α for any given combination of temperature and σ, the average value of $\lambda_{(t)}$ (the fraction of steady state charge generation from a surface, at time, t) during the period of depletion must be determined. For the purposes of this work the period of depletion is 5ms (see fig 8.9).

Fig 8.17 shows the dependence of λ upon time for a selection of temperatures and values of σ, as calculated by solution of equation 8.4. α is the average value of $\lambda_{(t)}$ during the period of depletion, and so is given by;

$$\alpha = \frac{1}{t_0}\int_0^{t_0} \lambda_{(t)} dt$$

where t_0 is the period of depletion.

As for fig 8.17, λ was calculated for a range of temperatures and values of σ. The values of α corresponding to each combination were then calculated numerically from plots such as those shown in fig 8.17, and are themselves shown in fig 8.18.

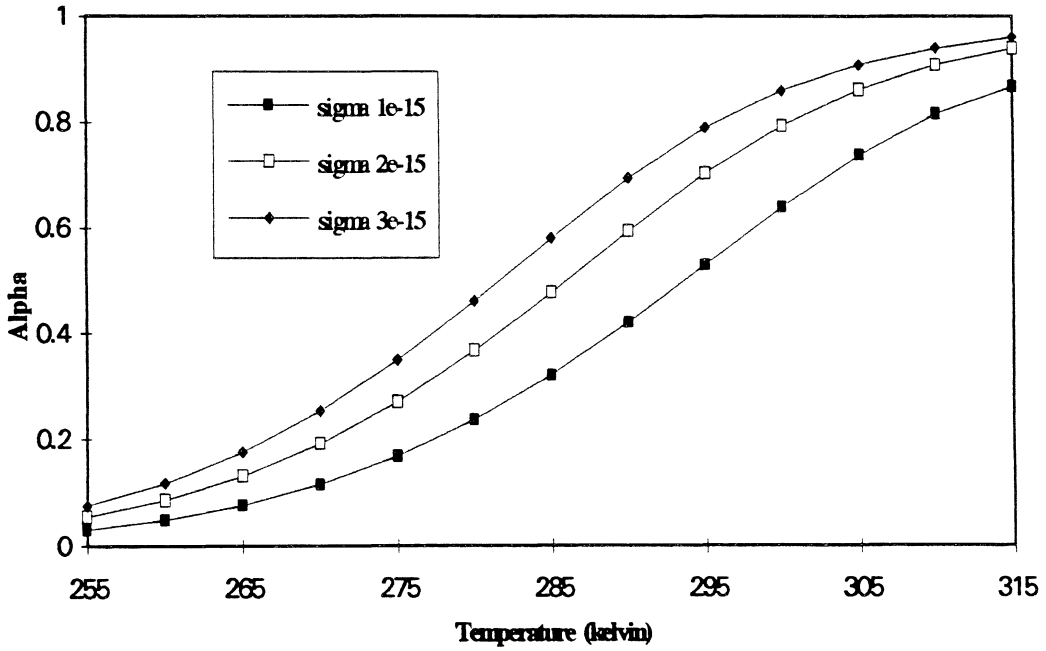


Fig 8.18. α as a function of temperature for a range of values of σ. The units of σ are cm^2.

8.4.3.2. Fitting the Theoretically Derived values of α to the Measured Dark Current.

Fig 8.19. refers to CCD05-8, prior to irradiation. It shows a comparison between the measured clocked dark current $I_dcl_{(m)}$, and the dark current predicted by inserting into equation 8.1, values of $\alpha_{p(T)}$ taken from fig 8.18 for four different assumed values of σ_{ps}, (where σ_{ps} is the geometric mean of the capture cross-sections at the p-stop surface). The closest fit is found for the case where σ_{ps} is approximately 2 x $10^{-15}cm^2$.

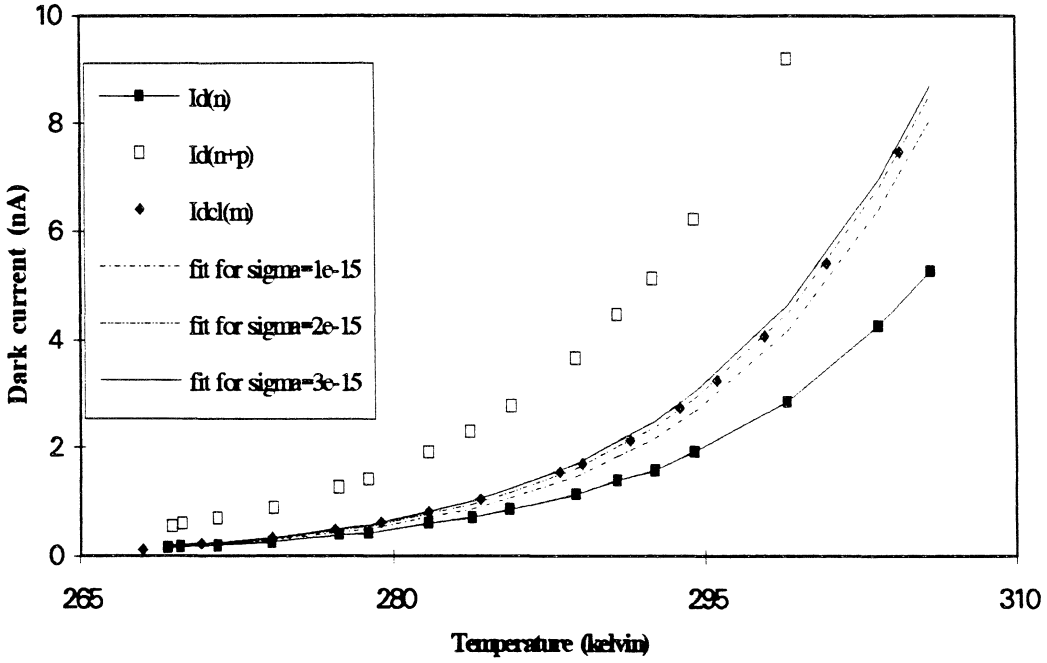


Fig 8.19. This shows the measured $I_dcl_{(m)}$ of CCD05-8, before irradiation, and that predicted by various values of σ_{ps}. Units of σ are cm^2

Fig 8.20 shows a similar treatment of CCD05-8 after it had been irradiated to 10krad, and then annealed at 373K for a total of 569 hours. Here the closest fit can be identified with a little more precision, at an assumed value for σ_{ps} of around 1.7 x $10^{-15}cm^2$. These results imply that there is little change in the capture cross-sections at the p-stop surface as a result of irradiation or annealing.

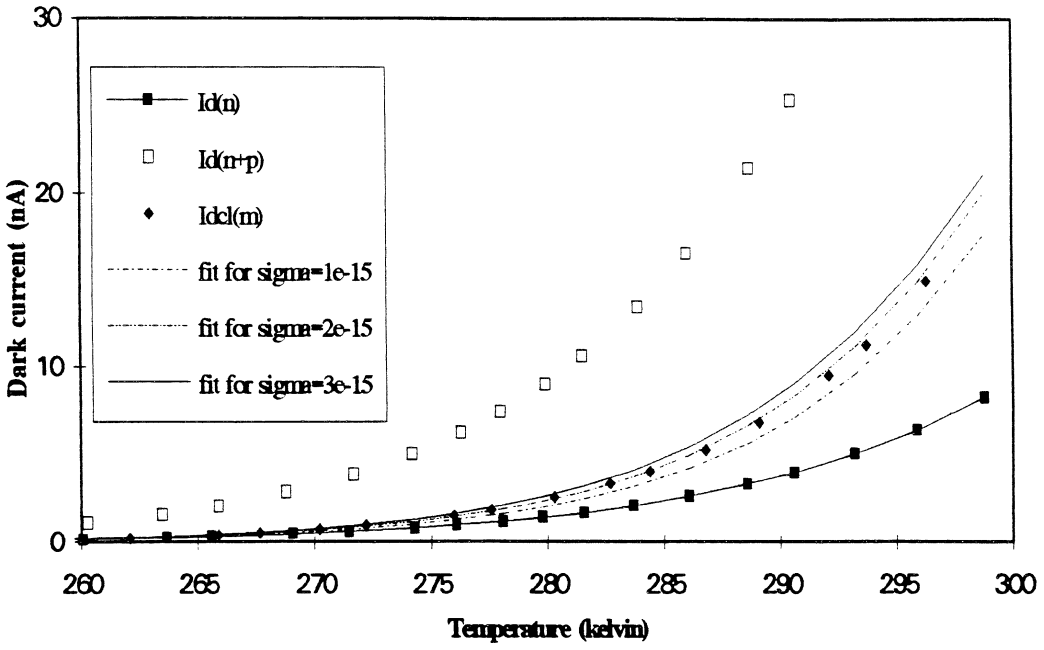


Fig 8.20. The measured $I_dcl_{(m)}$ of CCD05-8, after 10krad irradiation, and 570hours anneal at 373K, and that predicted by various values of σ_{ps}. Units of σ are cm^2.

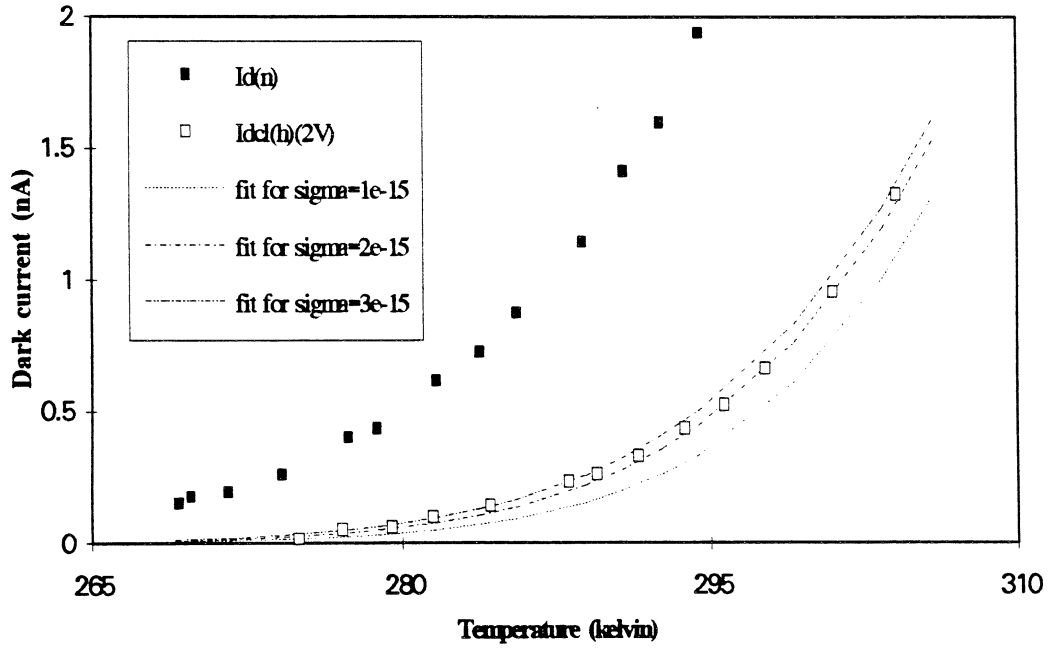


Fig 8.21. CCD05-8 prior to irradiation. Measured $I_dcl_{(h)}(2V)$ and that predicted by assumed values of σ_{ns}. Units of σ are cm^2.

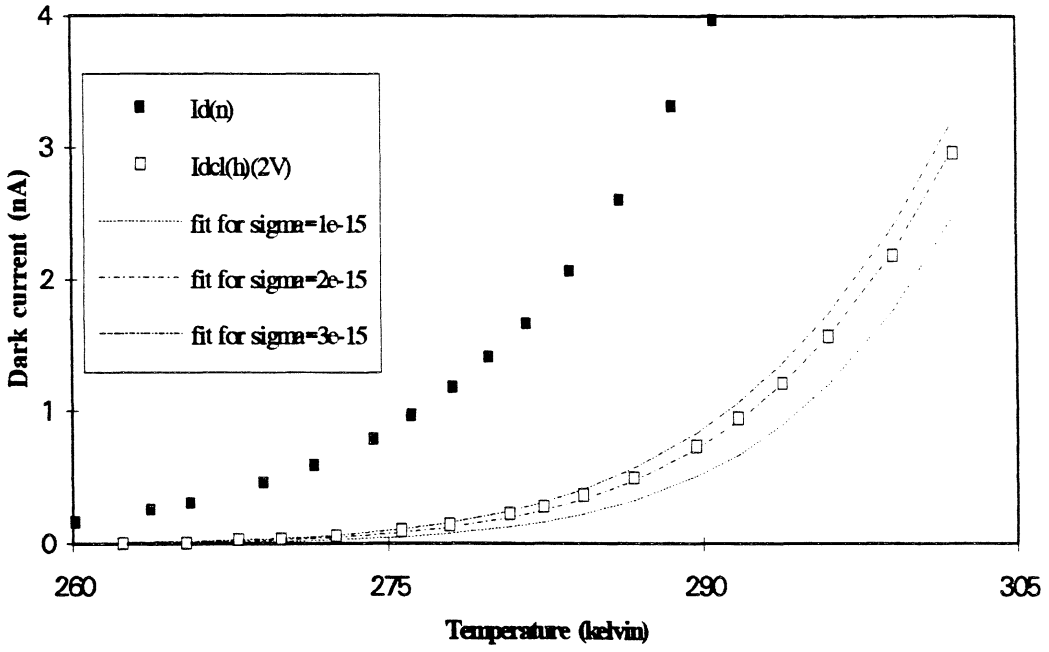


Fig 8.22. CCD05-8 after 10krad irradiation, and 569 hours anneal at 373K. Measured $I_dcl_{(h)}(2V)$ and that predicted by assumed values of σ_{ns}. Units of σ are cm^2.

Fig 8.21 and 8.22, show the measured $I_dcl_{(h)}(2V)$ for CCD05-8 compared with that predicted by equation 8.5, for a range of assumed values of σ_{ns}. The best fits are found for an assumed σ_{ns} of approximately $2 \times 10^{-15} cm^2$.

8.4.4. Calculation of the Effective Interface State Densities

Taking into account the the approximations used during the numerical determination of the dependence of λ, and subsequently α, upon σ_{ns} or σ_{ps}, and the nature of the plots used to derive σ_{ns} and σ_{ps}, it is not believed that they can be quoted with an accuracy of greater than $\pm$ $0.5 \times 10^{-15} cm^2$ (approx $\pm$ 25%). This, along with the error in the calculated values of the product, σD_{it}^* suggests a systematic error in the calculations of $D_{it}^*{}_{(ns)}$ and $D_{it}^*{}_{(ps)}$, of around $\pm$ 35%.

The calculated surface state densities for CCD05-8, taking σ_n to be $2 \times 10^{-15} cm^2$ and σ_p, to be $1.7 \times 10^{-15} cm^2$, are shown in the table 2, and in figs 8.23 and 8.24.

Irradiation and anneal history	$D_{it}^{*}{}_{(ps)}$ ($cm^{-2}eV^{-1}$)	$D_{it}^{*}{}_{(ns)}$ ($cm^{-2}eV^{-1}$)
	$\sigma_{ps} = (1.7 \pm 0.5) \times 10^{-15} cm^2$	$\sigma_{ns} = (2 \pm 0.5) \times 10^{-15} cm^2$
	systematic error $\approx \pm 35\%$	systematic error $\approx \pm 35\%$
pre-irradiation	$(2.93 \pm 0.02) \times 10^9$	$(6.34 \pm 0.03) \times 10^8$
post 10krad	$(5.81 \pm 0.05) \times 10^9$	$(7.07 \pm 0.02) \times 10^8$
after 23 hrs 373K anneal	$(9.63 \pm 0.04) \times 10^9$	$(9.78 \pm 0.07) \times 10^8$
after 68hrs 373K anneal	$(1.151 \pm 0.004) \times 10^{10}$	$(1.111 \pm 0.005) \times 10^9$
after 139hrs 373K anneal	$(1.372 \pm 0.003) \times 10^{10}$	$(1.252 \pm 0.004) \times 10^9$
after 261hrs 373K anneal	$(1.599 \pm 0.003) \times 10^{10}$	$(1.373 \pm 0.004) \times 10^9$
after 569 hrs 373K anneal	$(2.160 \pm 0.003) \times 10^{10}$	$(1.847 \pm 0.004) \times 10^9$

Table 2. Density of surface states in CCD05-8, as function of anneal time (all anneals with device unbiased).

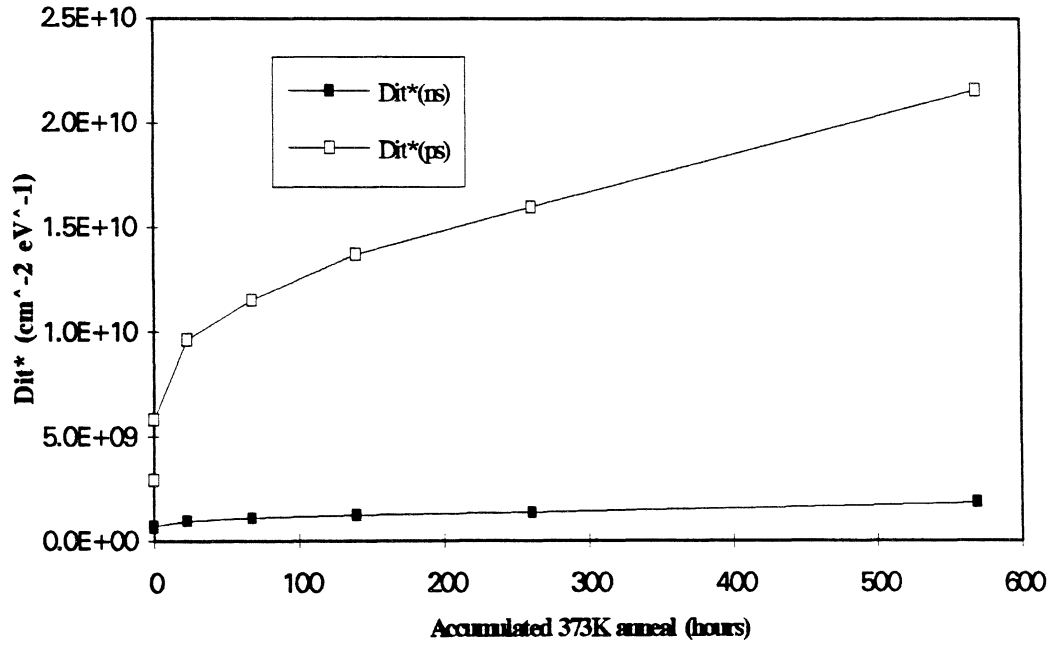


Fig 8.23. The density of surface states in CCD05-8, as a function of accumulated anneal (all anneals with device unbiased).

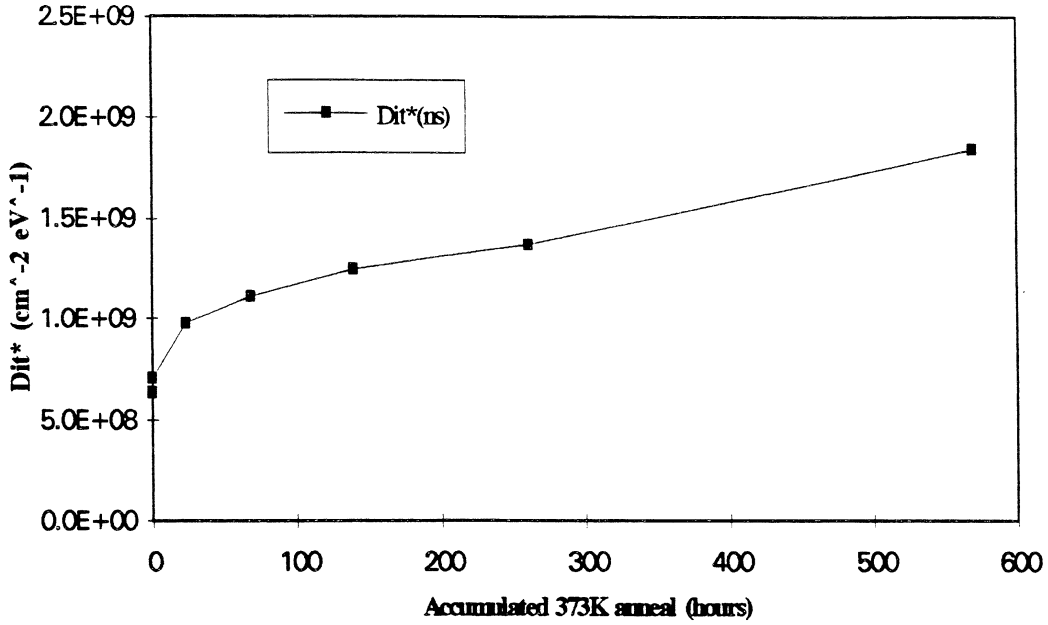


Fig 8.24. An expanded plot of the density of states at the n-channel surface, for CCD05-8 (all anneals with device unbiased).

As mentioned in section 8.3.1, the dark current contribution from the n-channel and p-stop surfaces at various stages of anneal, was also measured for a second device, CCD05-6. For this device the only geniune static dark current measurements were made following the final anneal, all other static measurements were simulated by reducing the applied gate bias (also see section 8.3.1.). Because of this no account was taken of leakage current. Also the measurements necessary to determine σ_{ns} and σ_{ps} were not made prior to irradiation, so it has to be assumed that there was no change as a result of irradiation and annealing. This does seem legitimate given the findings from CCD05-8. The calculated values of σD_{it}^{*} and D_{it}^{*} for CCD05-6, are shown in tables 3 and 4, and in fig 8.25.

Irradiation and anneal history	$\sigma_{ns}D_{it}^{*}(eV^{-1})$	$D_{it}^{*}{}_{(ns)}$ $(cm^{-2}eV^{-1})$
		$\sigma_{ns} = (1.7\pm0.5) \times 10^{-15}cm^{2}$
pre-irradiation	1.94×10^{-6}	1.14×10^{9}
post 10krad	2.16×10^{-6}	1.27×10^{9}
after 12 hrs 388K anneal	4.32×10^{-6}	2.54×10^{9}
after 27hrs 388K anneal	4.92×10^{-6}	2.89×10^{9}
after 51hrs 388K anneal	5.40×10^{-6}	3.18×10^{9}
after 101hrs 388K anneal	6.49×10^{-6}	3.82×10^{9}
after 180 hrs 388Kanneal	7.65×10^{-6}	4.50×10^{9}

Table 3. Density of states at the n-channel surface of CCD05-6 (all anneals with device unbiased).

Irradiation and anneal history	$\sigma_{ps}D_{it}^{*}(eV^{-1})$	$D_{it}^{*}{}_{(ps)}$ $(cm^{-2}eV^{-1})$
		$\sigma_{ps} = (1.7\pm0.5) \times 10^{-15}cm^{2}$
pre-irradiation	4.93×10^{-6}	2.90×10^{9}
post 10krad	1.09×10^{-5}	6.39×10^{9}
after 12 hrs 388K anneal	2.35×10^{-5}	1.38×10^{10}
after 27hrs 388K anneal	2.66×10^{-5}	1.57×10^{10}
after 51hrs 388K anneal	3.02×10^{-5}	1.78×10^{10}
after 101hrs 388K anneal	3.70×10^{-5}	2.18×10^{10}
after 180 hrs 388Kanneal	4.40×10^{-5}	2.59×10^{10}

Table 4. Density of states at the p-stop surface for CCD05-6 (all anneals with device unbiased).

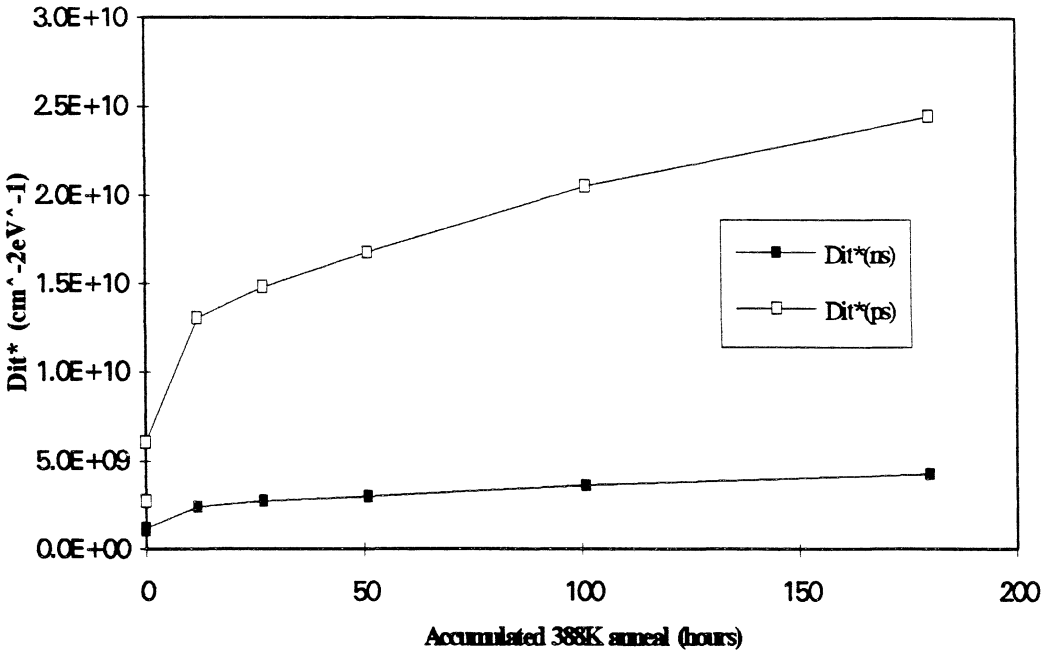


Fig 8.25. The effective density of surface states in device CCD05-6, as a function of accumulated anneal (all anneals with device unbiased).

8.4.5. Discussion of Findings

The values derived for the geometric mean of the electron and hole capture cross-sections at the Si/SiO_2 surfaces (~2 x $10^{-15}cm^2$) are of the order expected. Pierret [2] quotes the results of earlier authors who determined the capture cross-sections (close to the centre of the silicon bandgap) in the range of 10^{-14} - $10^{-15}cm^2$ in the case of electrons, and 10^{-15} - $10^{-16}cm^2$, for holes.

The density of interface states calculated from the above capture cross-sections are lower than expected, especially in the case of device CCD05-8 where the pre-irradiation density at the n-channel surface was found to be (6.3 ± 2.2) x 10^8 $cm^{-2}eV^{-1}$. Pierret suggests that a typical interface state density is around 1 x 10^{10} $cm^{-2}eV^{-1}$, but that densities closer 10^9 $cm^{-2}eV^{-1}$ have been measured.

Roy [1] also found the pre-irradiation n-channel interface state density of these devices to be low, at 1.1 x 10^9 $cm^{-2}eV^{-1}$ for EEV's CCD01 device. Roy had estimated σ_{ns} to be 1.4 x 10^{-15} cm^2, as

opposed to 2 x 10^{-15} cm^2 estimated for device CCD05-8, which suggests that the difference between his estimate, and that for CCD05-8, is a consequence of the imprecision with which σ_{ns} is measured, rather than any significant discrepancy between the initial surface states of the two devices.

Any underestimation of the surface state density due to an error of calculation seems unlikely, given the close agreement between the figures quoted here, and by Roy. However it is possible that an invalid assumption may have been made in the calculation of σ_{ns}. The method used to estimate σ_{ns} and σ_{ps} involves the assumption that for an intermittently depleted surface, charge generation is periodically quenched, as the surface goes out of depletion, and that the charge generation restarts upon the surface being re-depleted (see 2.3.2.2 & 8.4.3). Roy [1 p96] demonstrated that the p-stop surface need only be biased out of depletion for the order nanoseconds (compared to the transfer time of μs, see fig 8.9) in order to achieve full quenching of charge generation. The situation at the n-channel surface though, is less clear. Quenching of the charge generation process here entails the injection of holes from the p-stop, and so is likely be a more prolonged process. If incomplete quenching occurs in the time for which the surface is biased out of depletion, the consequences will be an increased level of dark current, and so an overestimation of σ_{ns}. This inturn would explain an underestimation in the density of states, $D_{it}{}^{*}{}_{(ns)}$.

Annealing measurements made with MOS structures are generally carried out with the devices in a biased state. Fleetwood et al [5] found that an unhardened MOS transistor with 45nm oxide (irradiated to 90krad(SiO_2), and biased at +6V during anneal) showed an increase in interface density of about 4 x 10^9 $cm^{-2}eV^{-1}$ after 11 hours at room temperature, and a further increase of about 3.5 x 10^{10} $cm^{-2}eV^{-1}$ after 170hrs at 100°C. As expected this increase is significantly greater than that seen for CCD05-8, which was unbiased during annealing. Other measurements of interface state buildup in biased MOS devices have been carried out by Schwank et al [6], and Saks and Brown [7]. Further references are given in chapter 2.

References for Chapter 8

[1] T. Roy, "Ionising Radiation Induced Surface Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1993.

[2] R.F. Pierret, "Advanced Semiconductor Fundamentals", Volume VI of "Modular Series on Solid State Devices", Published by Addison Wesley, 1987.

[3] R.M. Warner, and B.L. Grung, "Transistors: Fundamentals for the Integrated-Circuit Engineer", Published by Wiley Interscience, 1983.

[4] P.D. Ankram, "Semiconductor Electronics", Published by Prentice Hall, 1971.

[5] D.M. Fleetwood et al, "The Role of Border Traps in MOS High-Temperature Post=Irradiation Annealing Response", IEEE Trans. Nucl. Sci. Vol 40, 6, 1323-1334, 1993.

[6] J.R. Scwank et al, "Latent Interface-Trap Buildup and Its Implications for Hardness Assurance", IEEE Trans. Nucl. Sci., Vol 39, 6, 1953-1963, 1992.

[7] N.S. Saks, and D.B. Brown, "Interface Trap Formation Via the Two Stage H^+ Process", IEEE Trans. Nucl. Sci., Vol 36, 6, 1989.

Summary and Conclusions

This chapter is intended to serve as an independent summary of the areas investigated in this work, and of the findings. Consequently there is some repetition of text and figures from earlier chapters.

9.1. Overview

The main body of work undertaken was the characterisation of the damage mechanisms, both short term and long term, in EEV CCDs used in dentistry for medical x-ray imaging.

Initially irradiations were carried out on a number of conventional devices to establish flat band voltage shifts, and allow comparison with gamma induced damage. The work was then extended to measure the dark current increases shown by these devices and to characterise the x-ray induced effects in some technological variants. These include the inversion mode device, and two types of scintillator coatings, CsI(Tl), and Gadox(Eu) ($Gd_2O_2S(Eu)$).

The program was concluded by an investigation into the "reverse annealing" effect which has been blamed for the appearance, in some devices, of latent images of objects viewed previously. In order that the cause of this effect could be identified, and quantified, a series of anneals was carried out in which devices were irradiated and then annealed under various conditions.

In addition to the radiation work, further studies into the bias dependence of the CCD were performed. This work expands on device characterisation by Roy [1].(see chapter 5)

9.2. Flat-Band Voltage Shifts

For the initial measurements, made with CCD02 devices, the anti-blooming drain versus dark current profile, (V_{abd} v I_d), and the reset-drain bias versus dark current profile, (V_{rd} v I_d), were used to determine the voltage shifts (see sections 6.1 & 6.2). The CCD05 device does not have an antiblooming drain, and their multiple output nodes make measurent of the (V_{rd} v I_d) profile

Device type	V_{abd} v I_d	V_{rd} v I_d	V_{ss} v I_d	Reset turn-on
unbiased during irradiation				
Conventional CCD02	~10mV per krad	~10mV per krad		
Powered during irradiation				
Conventional CCD02	40-50mV per krad	40-50mV per krad		
Conventional CCD05			40-50mV per krad	40-50mV per krad
CsI(Tl) coated CCD05			90-100mV per krad	90-110mV per krad
Gadox coated CCD05 (GC1)				160mV per krad[1]
Gadox coated CCD05 (GC2)			90-100mV per krad	43mV per krad[2] 190mV per krad[1]
Associated Measurements				
RadFET biased at +20V		40μA threshold bias		
Thick oxide (0.85μm)		3V per krad		
Thin oxide (0.25μm)		0.27V per krad		

Notes; 1) reset transistor not covered by full thickness of Gadox(Eu) layer, due to layer thinning at the edge of the device, 2) reset transistor not covered by Gadox(Eu) layer at all.(see section 6.3.2.)

Table 1 The voltage shift measurements from EEV's CCD02 and CCD05 devices. The measurements are described in section 6.1.

impractical. Because of this voltage shifts in the CCD05s were determined using the substrate bias versus dark current profile, (V_{SS} v I_d), and reset transistor gate threshold bias (see sections 6.3 & 6.4). The results are summarised in table 1.

For 1MeV gamma irradiation, the shifts obtained from the CCD01 were 14mV per krad when unpowered during irradiation, and 120mV per krad when powered [2].

The dose profiles seen by the devices were modelled using the PHOTCOEF program [3] (see chapter 3 and appendix1) and it was found that for x-ray irradiation the silicon dioxide layer would be expected to receive only 67% of the dose received by the PIN diode dosimeter. This is primarily a result of electron transport from the device during irradiation, and affects the layers close to the surface. The epitaxial silicon layer being of much greater thickness only suffers dose reduction close to the oxide interface. This "dose factor" corresponds to the difference between the response of unpowered devices to x-rays and gamma rays.

This dose factor only partly explains the response of powered devices to x-rays as opposed to gammas. In addition the recombination of generated holes and electrons must be considered. The absorption of x-rays causes photoelectrons to be generated which have a much shorter range than the compton electrons scattered by Cobalt 60 gammas. As a result of this, a much more concentrated ball of charge is created. This increases the probability of recombination, and so reduces the yield of holes. This reduced yield is consistent with the reduced voltage shift observed for x-rays. Dozier and Brown [3] (see fig 2.4).

So for conventional devices, unpowered during irradiation, we have that;

$$\Delta V_{(70kVp)} = \Delta V_{(1MeV)} \times Dose\ Factor$$

where $\Delta V_{(70kVp)}$ is the voltage shift induced by 70kVp x-rays, and $\Delta V_{(1MeV)}$ is the voltage shift induced by 1MeV gammas.

and for conventional devices powered during irradiation, we have that:

$$\Delta V_{(70kVp)} = \Delta V_{(1MeV)} \times \textit{Dose Factor} \times \textit{Recombination Factor}$$

The irradiation degradation of the scintillator coated devices were significantly more than that of the conventional devices. However both types of scintillator caused the photocurrent induced during irradiation (and hence signal) to be enhanced to five times that seen in a conventional device. In order that these observations could be better understood, the device structures were modelled using PHOTCOEF (see appendix 1).

PHOTCOEF predicted that the CsI(Tl) coating would cause a 5-fold dose enhancement in the oxide and a 1.5-fold dose enhancement in the epitaxial silicon (see appendix 1 c&d).. The extra signal enhancement observed in practice is due to scintillated light, whilst the voltage shift is smaller than would be expected because much of the extra dose in the oxide is caused by low energy photoelectrons from the scintillator, and so the hole yield is low.

PHOTCOEF predicted a 5-fold dose enhancement in the oxide and a 1.4-fold dose reduction in the silicon, for the Gadox(Eu) coating (see appendix 1 e&f). It was found that towards the middle of the device the voltage shift was similar to that seen for the CsI(Tl) coated device, but close to the edges different voltage shifts were observed due to thinning of the layer (see section 6.3.2).

9.3. Dark Current Effects

Two types of dark current increase were observed in irradiated devices, a prompt increase seen immediately following irradiation, and a time dependent increase which occurs gradually.

9.3.1. The Prompt Increase in dark current.

These measurements were made with CCD05 devices, powered during irradiation. Dark current increases were as follows.

Device structure	Dark Current Increase per krad per device (pA)at 300K	Dark Current Increase per krad cm^2 (pA) at 300K
Conventional (V_{SS}=6V)	310	68
Gadox(Eu) coated (V_{SS}=6V)	320	71
CsI(Tl) coated (V_{SS}=6V)	1150	260
Inversion mode device operated in inversion (V_{SS}=9V)	less than 1pA	less than 1pA

The two scintillator coatings caused different device responses. Whilst the Gadox(Eu) coated device showed a similar dark current increase to the conventional device, the CsI(Tl) showed a far greater increase. This difference is probably explained by the presence of a polyimide layer under the CsI(Tl) but not under the Gadox(Eu). The polyimide layer may be acting as a source of hydrogen which is released by radiation and leads to to the generation of surface states at the Si/SiO_2 interface as described for the reverse annealing process,(see below and section 2.2.2.2).

9.3.2. The Time Dependent Increase in Dark Current

This work was instigated by EEV in response to the observation of time dependent effects in devices which were irradiated and then left in storage at room temperature. On inspection, several months after irradiation, some devices were found to show latent images of objects viewed during previous exposures.

It is known that the density of defect states at Si/SiO_2 interface increases with time in MOS devices following irradiation, in a process referred to as "reverse annealing" [4]. As this would explain the presence of localised regions of high dark current in a device, and hence a latent image, it was considered most likely to be the cause of the problem. As described in [4], by far the largest of the effects contributing to "reverse annealing", is the transport of hydrogen ions, liberated by radiation generated electrons/holes in the oxide, towards the Si/SiO_2 interface (see section 2.2.2.2). On reaching the interface the ion is able to combine with a hydrogen atom which is acting as passivation to an interface state, thus exposing the state. This increase in interface state then causes a corresponding increase in dark current.

In order to determine that this process was the cause of the latent images, an annealing programme was carried out in three stages. The first series of anneals, using CCD02 devices, was intended to determine whether irradiation triggers reverse annealing, and also to reveal the charge state of the agent causing the interface states. A second series was then undertaken using CCD05 devices in order to quantify both the time and temperature dependence of the process. In addition to this work, further anneals were carried out to test for dependence of the reverse anneal process upon other factors such as scintillator coatings, and consecutive irradiation/anneal cycles

9.3.2.1. Electric Field, and Irradiation Dependence of the Reverse Annealing Process

The first series of anneals was carried out at 373K in order to speed up the process. The dark current increases quoted are for devices operated at 300K after 50 hours anneal.

Device and conditions of anneal	Dark Current Increase (pA) Devices clocked with V_{ss}=6V
CCD02-3 unirradiated, and pins shorted during anneal	100
CCD02-4 unirradiated, 10V +ve oxide field during anneal	200
CCD02-1 irradiated to 5krad, pins shorted during anneal	1800
CCD02-2 irradiated to 5krad, conventional bias during anneal	Decrease of 800*
Inversion Mode CCD02IM-1, irradiated to 10krad, then operated in inversion (V_{ss}=9V)	No measurable increase, whatever bias during anneal
As above operated out of inversion	see fig 1

* A drop was observed after five hours, the dark current then seemed to stabilise, showing a slight recovery in dark current level after 50 hours

From this table and fig 1 it can be seen that a conventional oxide field (field direction towards gate) inhibits the process whilst a positive oxide field enhances it. This is consistent with the hypothesis that the migration of H^+ ions to the Si/SiO_2 interface is responsible for the reverse annealing process.

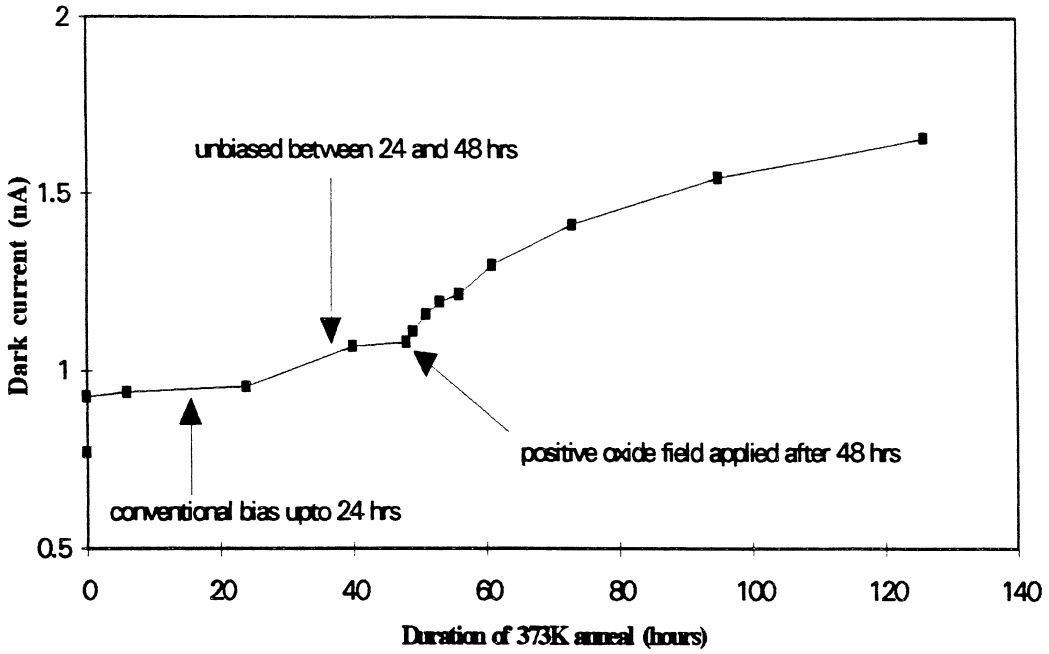


Fig 9.1. The response of the inversion mode device to 373K annealing, when operated out of inversion mode. For the first 24 hours the device was annealed whilst biased conventionally, for the next 24 hours unbiased, and from then on a positive oxide field was contrived. It can be seen that the conventional field inhibits the reverse annealing, whilst the positive oxide field enhances it. The dark current was measured at 300K, and V_{SS}=6V.

9.3.2.2. Time and Temperature Dependence of the Reverse Anneal Process

For this work seven CCD05 devices were used, all were irradiated to 10krad, and were annealed unbiased, to simulate storage conditions for commercial devices. Three of the devices selected from different production batches were annealed at 408K. This meant that batch to batch dependency could be investigated, and also simulated the temperature of the autoclave, which could possibly be used to sterilise devices in the field. It was also hoped that the use of such a high temperature would allow the process to saturate, revealing the maximum interface state buildup. Devices were also annealed at 388K, 373K and room temperature. It was then possible to use the high temperature anneals to calculate an effective energy barrier to the process, and then cross-check the predicted temperature dependence, against the dark current increase seen in the device held at room temperature. The dark current at each anneal stage was measured as a function of temperature for

each device, to ensure greater accuracy. Extra measurements were carried out on CCD05-6 (annealed at 388K), and CCD05-8 (annealed at 373K) to allow discrimination between dark current contribution from n-channel surfaces and dark current contribution from p-stop surfaces, and also to allow the respective interface state densities to be calculated.

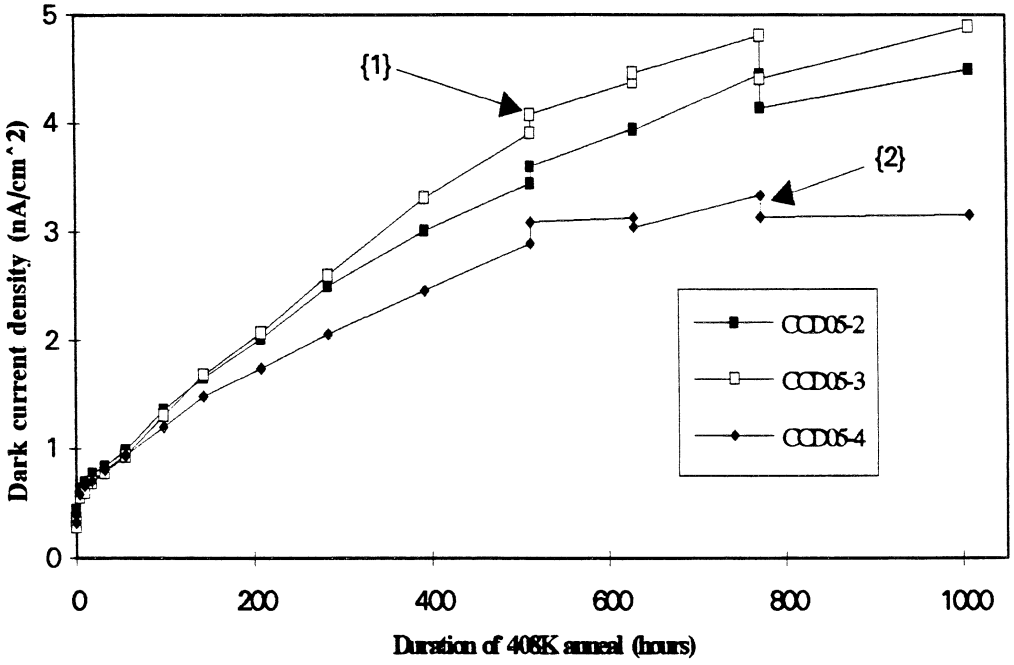


Fig 9.2. The reverse annealing of devices exposed to 408K whilst unbiased. The discontinuity at {1} was caused by a 373K anneal which was carried out in an attempt to compare the rates of anneal at the two temperatures. The drop in dark current at {2} occured after a delay of 3 weeks between anneals, which suggests that there is a recovery process competing with the reverse annealing. Dark current was measured at 280K with V_{ss}=6V.

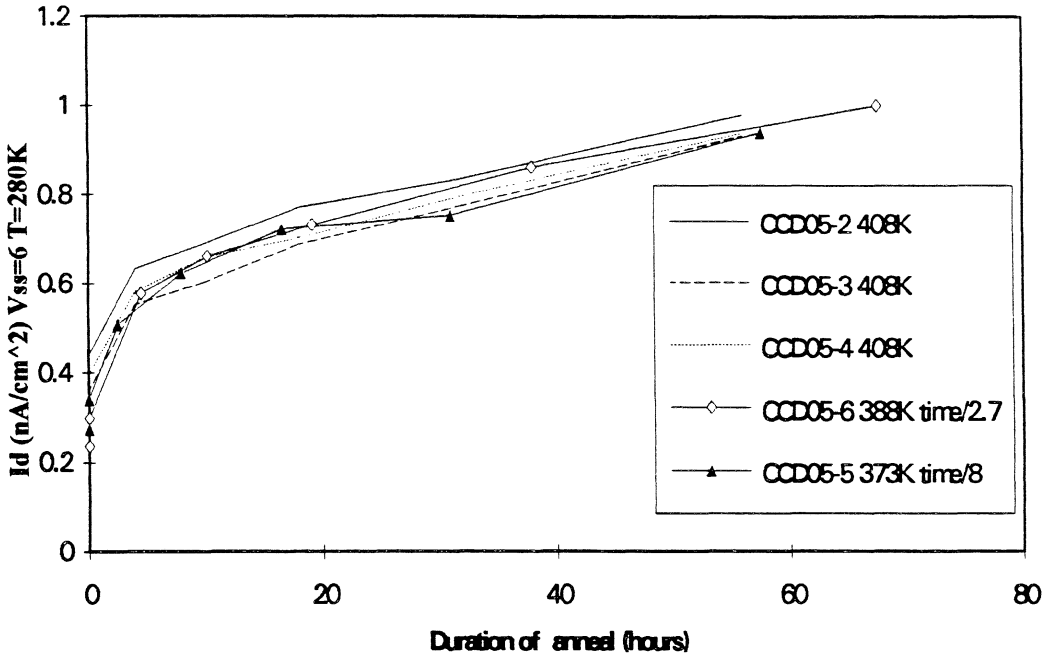


Fig 9.3. This plot shows that the dark current data taken from the devices annealed at 388K and 373K can be overlaid on the data taken from the devices annealed at 408K, if the time axes are changed by the correct factor. The factors are 2.7 and 8 for 388K and 373K respectively. All devices annealed unbiased.

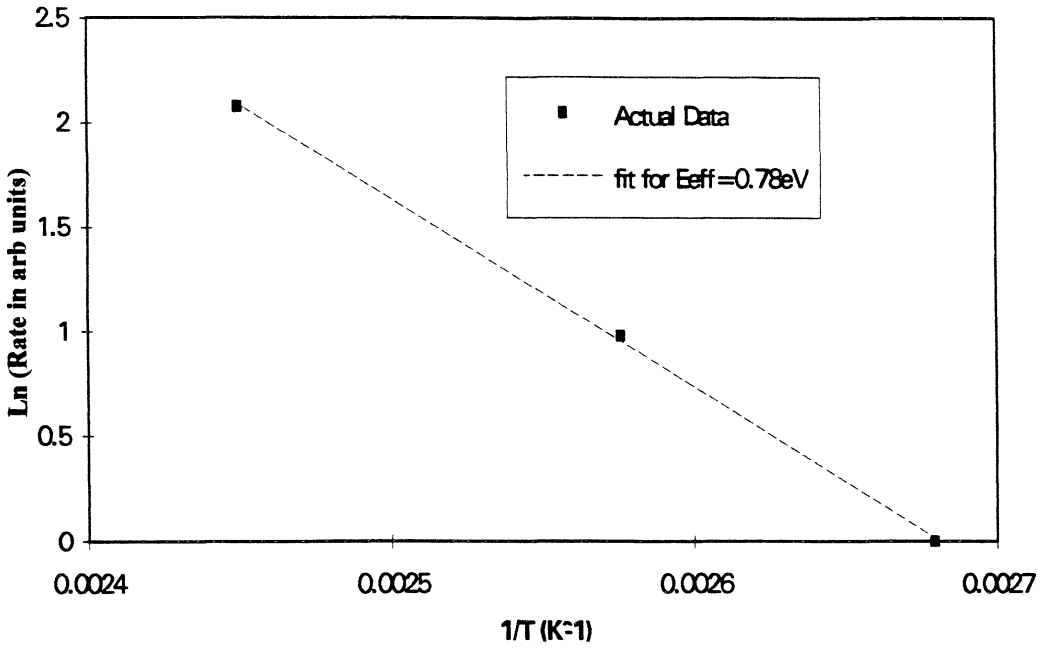


Fig 9.4. The derivation of the effective energy barrier to the reverse annealing.

It was found that the rate of dark current increase at 408K is 8 times that at 373K, and 2.7 times that at 388K (fig 9.3). Using these ratios figure 9.4 was plotted in order to determine the effective energy barrier (E_{eff}) resisting the process. This barrier was found to be 0.78eV. Using figs 9.3 and 9.4, the following relationship between time, temperature and dark current was derived

The dark current for a CCD05 or CCD02 device at T=280K and Vss=6V, rises by approximately $0.18nAcm^{-2}$, ($I_{Danneal(1)}$) after a time "t_1" given by

$$t_1(hours)=6\times10^{-10}\times\exp(\frac{E_{eff}}{KT})$$

Further increase in dark current $I_{Danneal(2)}$, approximates to a saturating exponential where t_{eff} < ~600 hours (see below), and is given by;

$$I_{Danneal2}(nA\,cm^{-2}) = A(1-\exp(-\frac{t_{eff}}{900})$$

where

$$t_{eff} = Duration\ of\ anneal\ (hours) \times 4.19 \times 10^{9} \times \exp(-\frac{E_{eff}}{KT})$$

$A \approx (5.7 \pm 1.3)$ nAcm^{-2}, and E_{eff} is taken as 0.776eV

Taking into account the accuracy of the calculation of E_{eff} and the variability of room temperature, it was calculated that one day's anneal at 373K is equivalent to between one and two years' anneal at room temperature. In this time a dark current increase of around 0.8nA could be expected for a CCD05 device, for T=280K, and Vss=6. This compares with the measurement taken to date, of 0.66 nA after 7 months of room temperature annealing. The corresponding increase at 300K was 8.6nA (1.9nAcm^{-2}).

9.3.2.3 Buildup of Interface States

In order to quantify the buildup of interface states at the p-stop and n-channel surfaces extra measurements were carried out on devices CCD05-6 (annealed at 388K) and CCD05-8 (annealed at 373K). At each anneal stage the dark current was measured with V_{SS} in the high range (p-stops depleted) and in the medium range (n-surface depleted, p-stop surface accumulated)(see fig 8.5). This enabled the dark current contributions from the two regions to be determined. Also the geometric means of the capture cross-sections in the two regions was determined by comparison of dark currents in different operating regimes (see section 8.4.3, and[1]). The cross-sections were found to be $(1.7 \pm 0.5) \times 10^{-15}$ cm^2 for both surfaces of CCD05-6, and the p-stop surface of device A3067-10-10, and $(2 \pm 0.5) \times 10^{-15}$ cm^2 for the n-channel surface of CCD05-8, although it is possible that these values are overestimated in the case of the n-channel surfaces (see section 8.4.5). This suggests that although the dark current contributions from the two regions are different, indicating a different density of surface states in the two regions, chemically the behaviour of the

two interfaces is similar.

The density of states at the two surfaces was calculated from the following [1,5];

$$D_{it}^{*} \approx \frac{2J_D}{q\pi kTn_i v_{th}\sqrt{\sigma_{ns}\sigma_{ps}}}$$

where D_{it}^{*} is the effective density of interface states ($cm^{-2}ev^{-1}$), J_D is the dark current density form the device (Acm^{-2}), v_{th} is the average thermal velocity of the carriers (cms^{-1}), n_i is the intrinsic carrier concentration (cm^{-3}), and σ_{ns} and σ_{ps} are electron and hole capture cross-sections at the surface (cm^2).

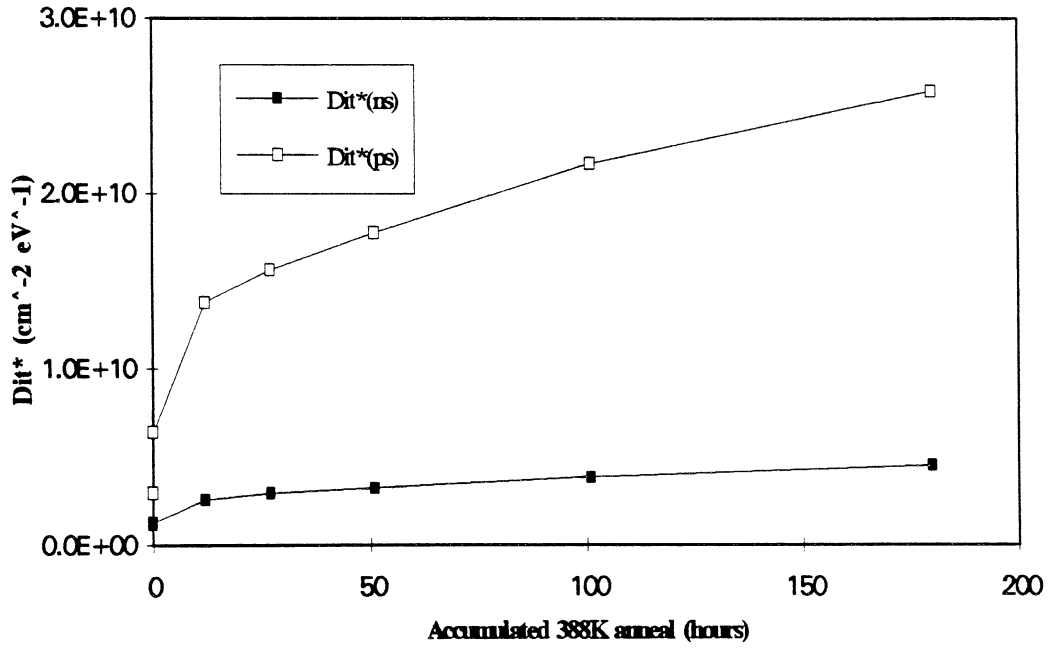


Fig 9.5.. Buildup of interface states at p-stop ($D_{it}^{*}{}_{(ps)}$), and n-channel ($D_{it}^{*}{}_{(ns)}$) interfaces during 388K anneal for device CCD05-6. (device annealed unbiased).

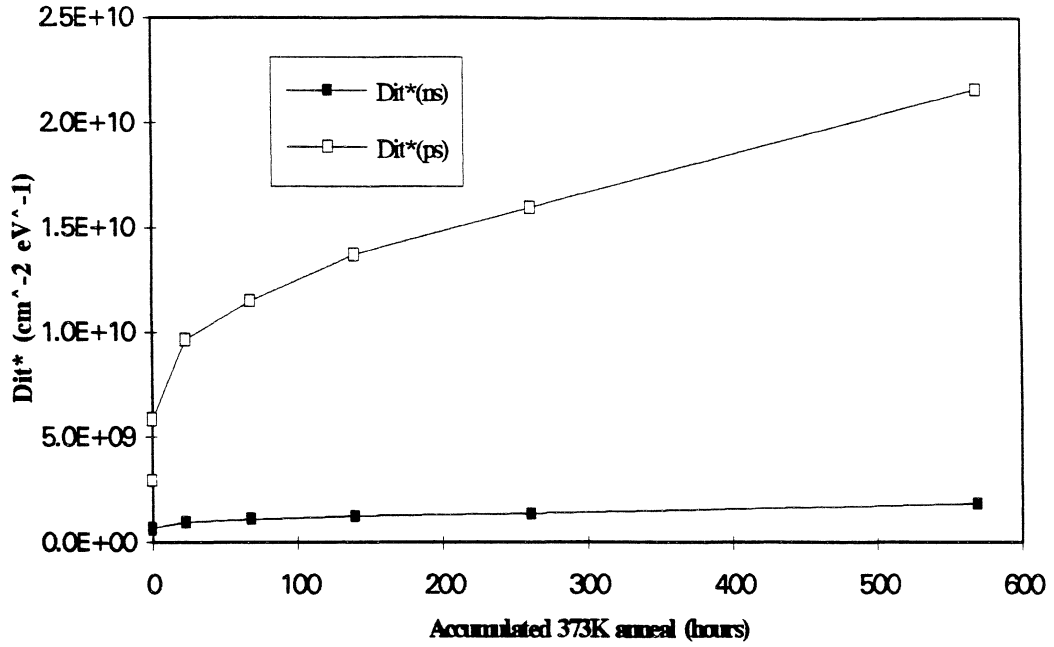


Fig 9.6. Buildup of interface states at p-stop and n-channel interfaces during 373K anneal for device CCD05-8. (device annealed unbiased).

For CCD05-6 the interface state density at the p-stop surface was calculated to be approximately 2.90 x 10^9 $cm^{-2}eV^{-1}$ prior to irradiation, rising to 6.39 x 10^9 $cm^{-2}eV^{-1}$ after 10krad, for CCD05-8 the initial interface state density was calculated at 2.93 x 10^9 $cm^{-2}eV^{-1}$, rising to 5.81 x 10^9 $cm^{-2}eV^{-1}$ after 10krad. This compares with Roy's calculation [1] of an interface state density, at the p-stop surface, of 1.6 x 10^{10} $cm^{-2}eV^{-1}$ prior to irradiation, rising to 1.7 x 10^{11} $cm^{-2}eV^{-1}$ after 30krad of Sr^{90} betas. However Roy had calculated the geometric mean of the capture cross-sections to be approximately 4 x 10^{-16} cm^2. This difference in derived capture cross-section largely explains the difference in calculated interface state densities. If a value of 1.7 x 10^{-15} cm^2 is assumed, then Roy's work indicates a rate of interface state generation with dose, of 1.2 x 10^9 $cm^{-2}eV^{-1}krad^{-1}$. This compares to (3-3.5) x 10^8 $cm^{-2}eV^{-1}krad^{-1}$ calculated from the findings of this work.

From figs 9.5 and 9.6, it can be seen that most of the interface state buildup occurs at the p-stop surface. However if the device is to be operated such that the n-channel surface is permanently depleted, with the p-stops predominantly accumulated, then the device will still be sensitive to the buildup of states at the n-channel surface (see section 8.3.2.3).

9.3.3. Consideration of Scintillator Coatings and Stepped Irradiations

The results quoted above all apply to devices with conventional structures, irradiated to a large dose prior to annealing. In order to test the validity of these results for devices of differing architecture, and for devices facing differing irradiation regimes, the following anneals were carried out;

One Gadox(Eu) coated device and one conventional device were irradiated in steps of 2krad, upto a total of 10krad, with 15 hour, 408K anneals carried out after each irradiation. In addition the CsI(Tl) coated CCD05 which had previously been irradiated to 5krad and then annealed at 408K to test for scintillator damage, was given further anneals at 408K.

As can be seen from fig 9.7, the two devices initially irradiated to 2krad showed lower levels of dark current than those irradiated to the full 10krad, after 15 hours anneal. However this was mainly due to the smaller prompt dark current increase. The actual increase in current seen during the anneal is of similar magnitude. By the time the accumulated dose of these devices reached 10krad their dark current levels had reached those of the other devices. This suggests that the reverse anneal process is not a heavily dependent function of dose, at least for shorter anneal times, provided that the dose is above a certain trigger level, which is less than 2krad. Once radiation produces a pool of hydrogen ions the transport to the interface is limited by the interleaving medium; i.e. the size of the pool is irrelevant. This principle would be invalid if the process was allowed to continue to saturation, however, this would appear to take many hundreds of years at room temperature.

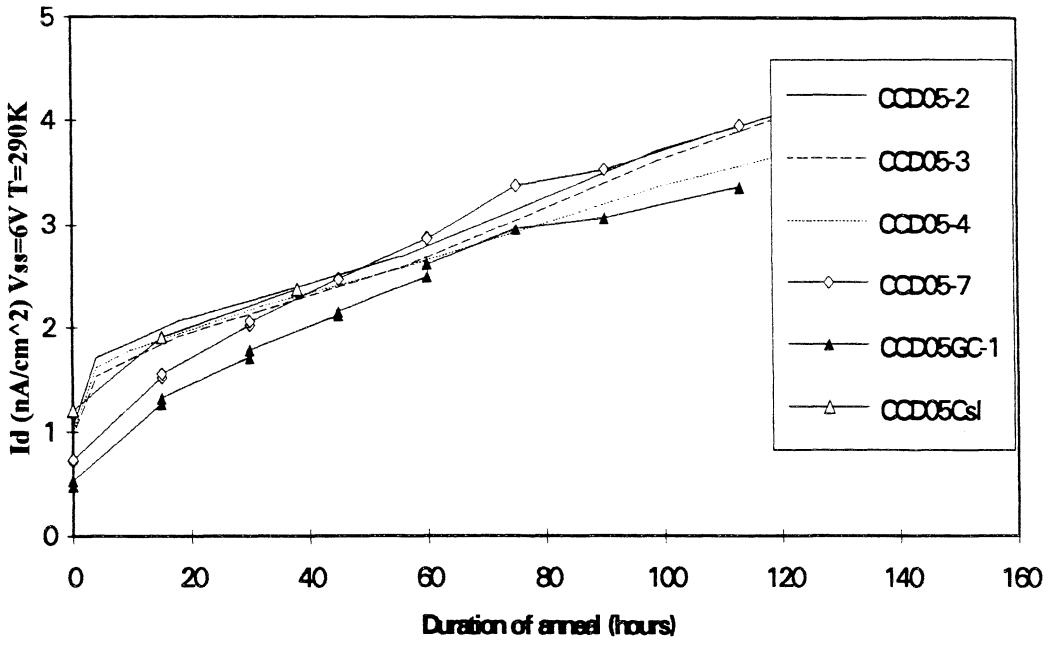


Fig 9.7. A plot comparing the reverse annealing of devices irradiated to 10krad prior to annealing at 408K, with devices irradiated in steps. Devices CCD05-2,3 and 4 were irradiated to 10krad prior to annealing. The Gadox(Eu) coated device, CCD05GC-1, and the control device, CCD05-7, were irradiated in steps of 2krad alternated with 15 hour 408K anneals untill an accumulated dose of 10krad had been reached, and then were given a further 50 hours anneal.

9.4. Annealing out of Flat-band Voltage Shifts

Whilst these anneals were being performed, the flat band voltage of the devices was monitored by checking the reset turn-on threshold. As shown in fig 9.8, at high temperatures a significant proportion of the voltage shift can be recovered (see section 6.4).

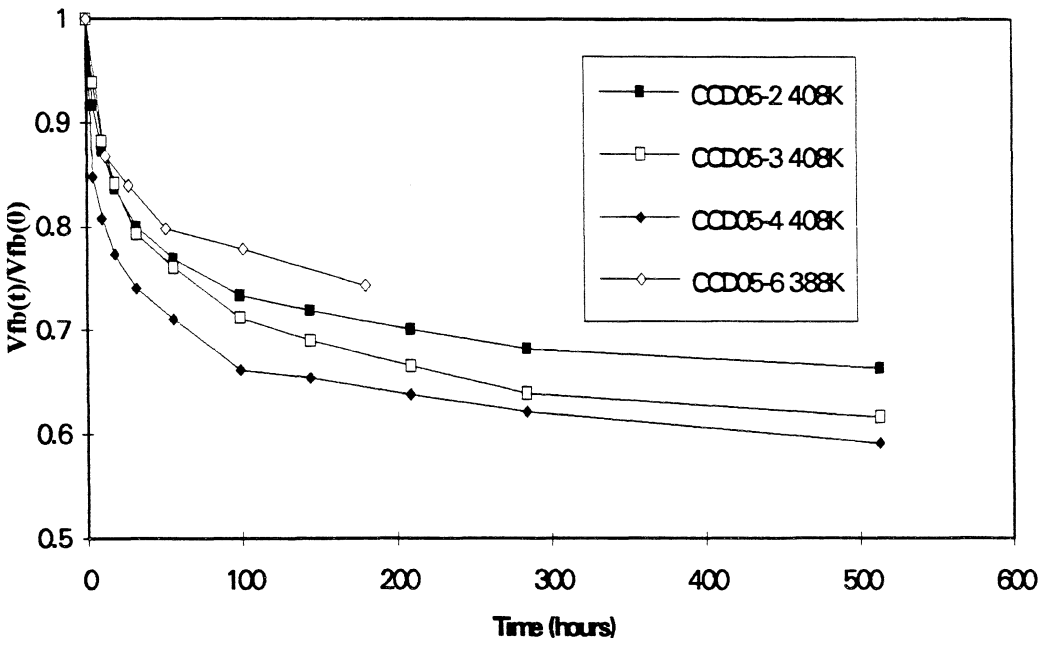


Fig 9.8.. Recovery of flat band voltage shift in CCD05 devices irradiated to 10krad, with nominal shift of 450mV.

9.5 Conclusions

X-rays induce smaller shifts per unit dose than gamma rays. This is understood in terms of dose deposition and charge recombination.

Degradation of scintillator coated devices (voltage shifts) is greater than for the conventional structure. However the signal enhancement more than compensates for this.

Defining a figure of merit, F, as;

$$F = \frac{signal\ enhancement}{increase\ in\ rate\ of\ degradation}$$

For the CsI coated device the figure of merit $F_{(CsI(TL))}$ is;

$$F_{(CsI(Tl))} \approx \frac{5}{2} \equiv 2.5$$

For the Gadox coated device the situation is more complicated. As the layer is deposited at present, it thins towards the edge of the device so causing a non-uniform voltage shift. For regions of the device under the thin part of the layer the voltage shift is actually enhanced, up to 190mV in the worst case. Taking this worst case scenario, the figure of merit $F_{(Gadox(Eu))}$ is;

$$F_{(Gadox(Eu))} \approx \frac{5}{4} \equiv 1.25$$

It is probable that this figure could be increased to 2.5, by extending the Gadox(Eu) layer a few mm further at the device edges, and so ensuring uniformity of layer thickness over the whole device area.

PHOTCOEF provides a good basis for calculating the effects of scintillator coatings.

Reverse annealing of dark current has been observed. It is very small compared with the results from other manufacturers' devices [7] (see fig 9.9).

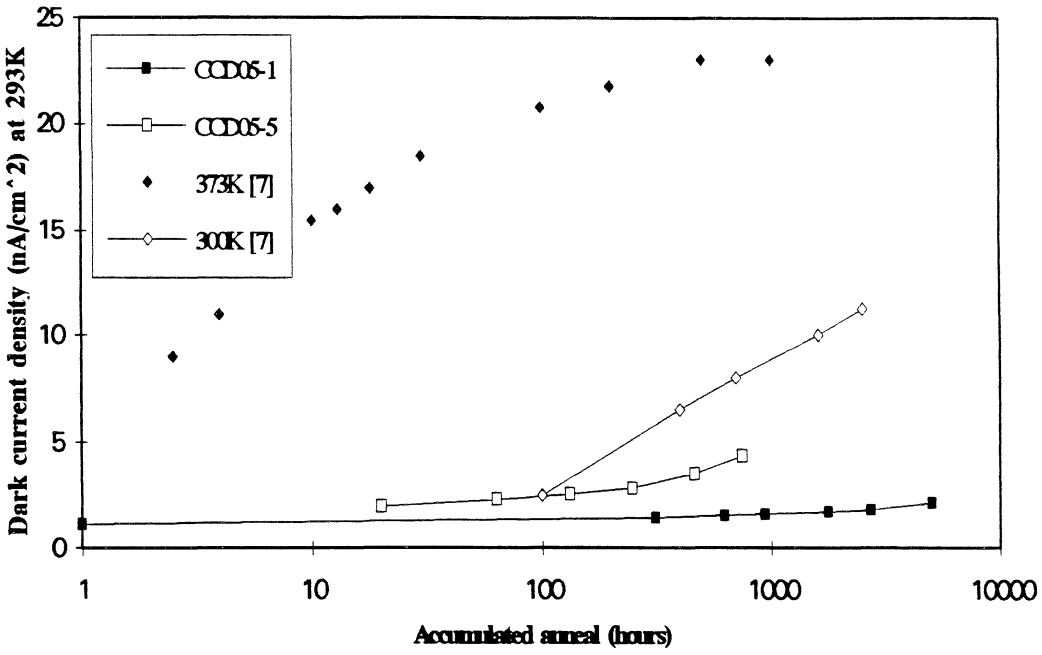


Fig 9.9. The annealing of CCD05-1 (room temperature), and CCD05-5 (373K) compared to annealing measurements made by Herve et al [7]. CCD05-1 and CCD05-5, were both irradiated to 10krad prior to annealing, whereas the devices used by Herve were irradiated to 3krad (SiO_2) with Sr^{90} betas.

The annealing effect is inhibited by a conventional oxide bias, and enhanced by a positive bias. This field dependence implies that a migration of hydrogen ions to the Si/SiO_2 interface is responsible. It is clear that most of the hydrogen originates in the p-stop region. There is evidence that polyimide provides a source of hydrogen for this process.

The effective energy barrier for the reverse annealing process is 0.78eV (cf 0.82eV [4], and 0.85eV [7])

The total increase in dark current I_{Dinc}, is given by;

$$I_{Dinc} = I_{Dprompt} + I_{Danneal(1)} + I_{Danneal(2)}$$

where $I_{Dprompt}$ is the increase in dark current seen immediately following irradiation, and $I_{Danneal(1)}$ and $I_{Danneal(2)}$ are the fast and slow components of the reverse anneal induced dark current increase (see sections 9.3.1, and 9.3.2).

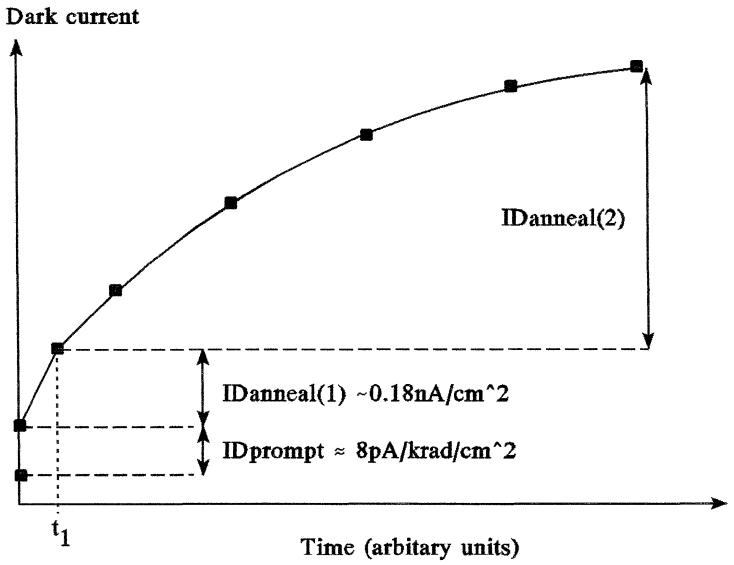


Fig 9.10. A schematic showing the three components of radiation induced dark current for a device operating temperature of 280K. For an operating temperature of 300K the anneal induced dark current increases are approximately 13 times greater, with $I_{Dprompt}$ increasing to 70pAcm^{-2} per krad.

Using this energy barrier, and the annealing measurements taken at high temperatures, it is predicted that conventional CCD02 and CCD05 devices which are left at room temperature following irradiation, will see an increase in dark current of 0.18nAcm^{-2} (for T=280K, Vss=6V) after between one and two years. For a CCD05 with an active area of 4.5cm^2 this implies a rise of 0.8nA for the whole device, which compares with an observed increase of 0.66nA after 7 months to date. The corresponding increase at 300K was 8.6nA (1.9nAcm^{-2}).

Although more work is needed, this process is triggered by radiation. It is believed that for the doses received by these samples, the reverse annealing is due to a supply of hydrogen released by the radiation. Once this source of hydrogen is produced the reverse annealing is largely independent of the total dose.

Dark current increases are caused by surface states only[1]. Changes in dark current caused by irradiation, both initially and after reverse annealing, are eliminated by use of inverted mode operation. With conventional CCDs, the effect can be reduced by powering the devices during storage. If it proves necessary to autoclave devices (which involves heating to 408K), then it would be beneficial to power them during the process.

[1] X-rays used in dentistry do not have photons of sufficient energy to cause bulk defects

References for Chapter 9

[1] T. Roy, "Ionising Radiation Induced Surface Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1993.

[2] M.S. Robbins, "Radiation Damage Effects in Charge Coupled Devices", PhD Thesis. Dept of Physics, Brunel University, UK, 1992.

[3] C.M. Dozier, and D.B. Brown, "Effect of Photon Energy on the Response of MOS Devices", IEEE Trans. Nucl. Sci., NS-28, 6, 1981.

[4] T.R Oldham, F.B. McLean, H.E. Boesch Jr, and J.M. McGarrity, "An Overview of Radiation Induced Interface Traps in MOS Structures", Semicond. Sci. Technol. Vol 4, 986-999, 1989.

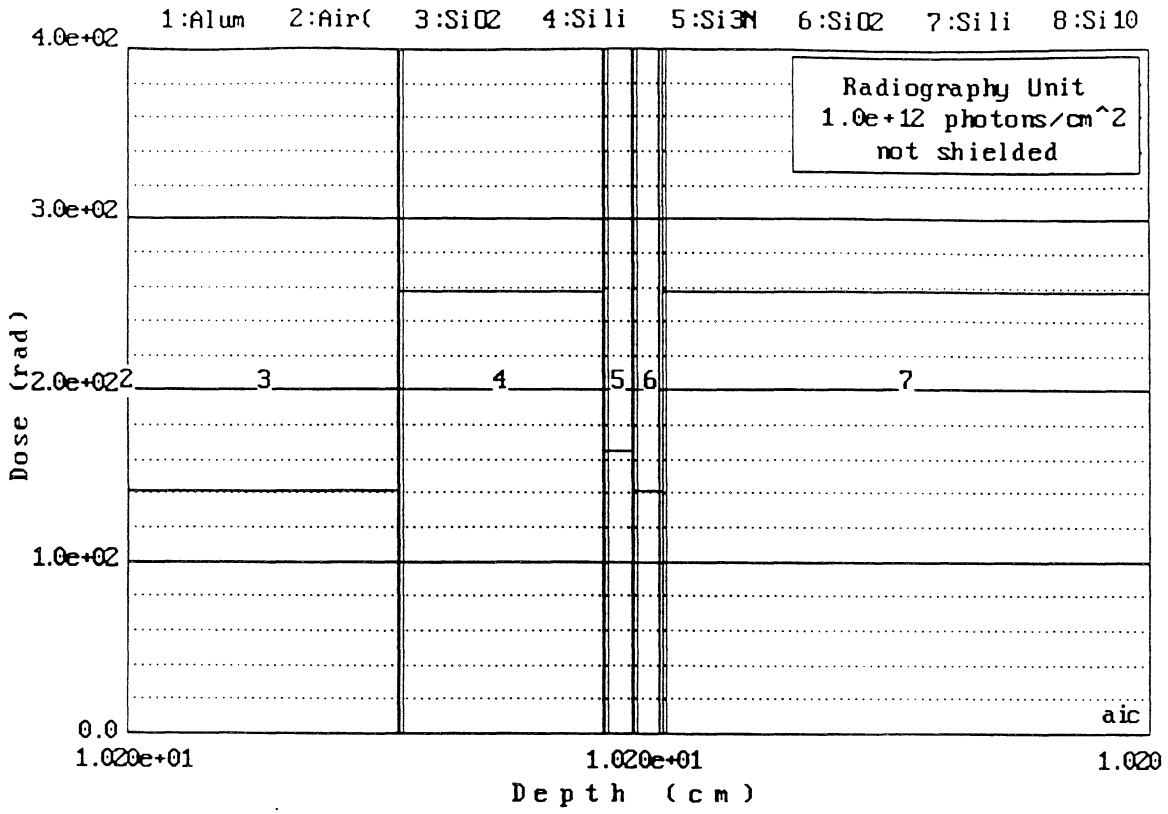
[5] R.F. Pierret, "Advanced Semiconductor Fundamentals, Volume VI of Modular Series on Solid State Devices", Published by Addison-Wesley, 1987.

[6] PHOTCOEF, AIC Software, PO Bx 544, Grafton, Mass 01519, USA.

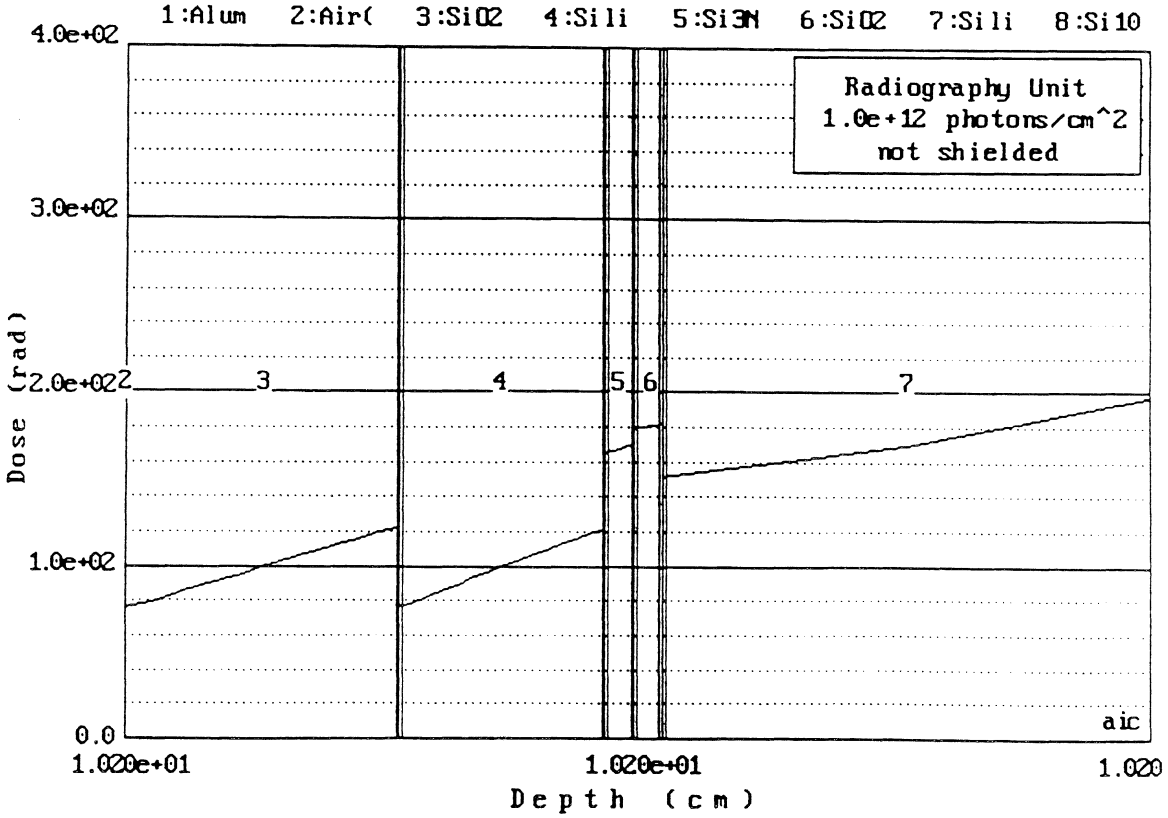
[7] D. Herve, et al "Cumulated Dose Long Term Effects in Charge Coupled Devices", CEA, BP 12, 91680 Bruyeres-le-Chatel, France. Presneted at RADECS '91 343-347, 1991.

Appendix 1. PHOTCOEF Simulations

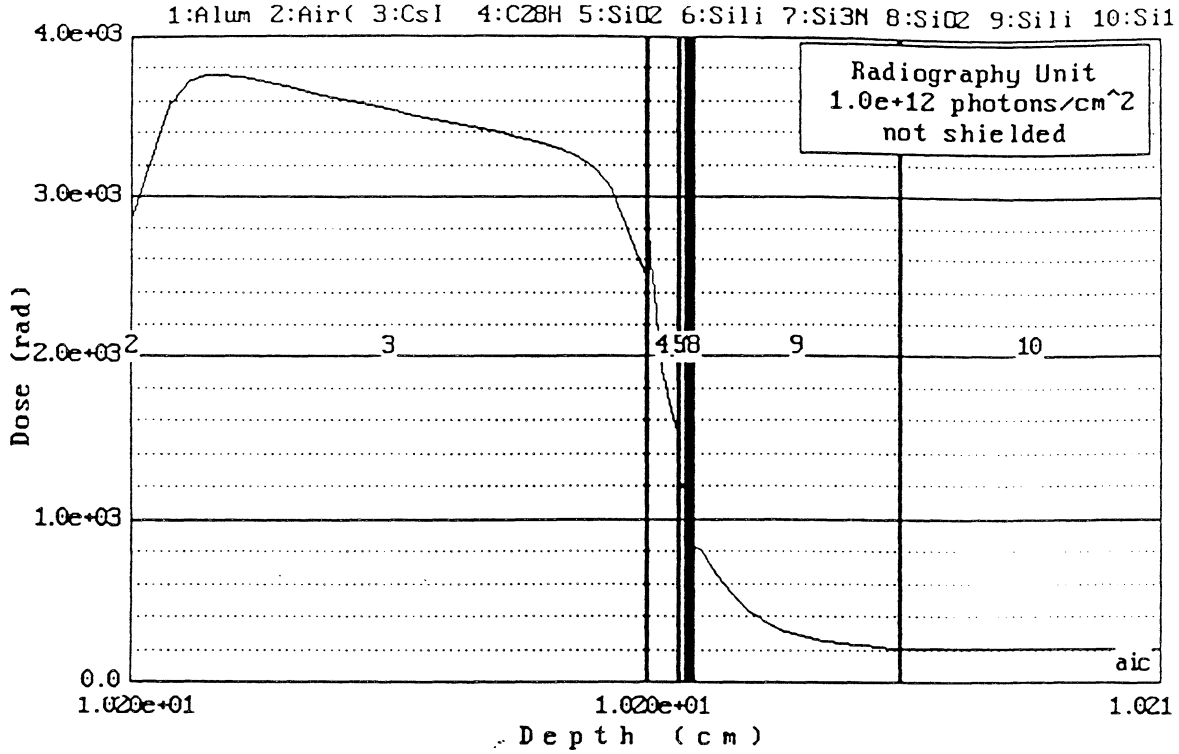
a) Irradiation by 70kVp x-rays. Equilibrium dose (neglecting electron transport between layers) through conventional device. Layer 5 is the gate nitride, 6 is the gate oxide, and 7 is the epitaxial layers.



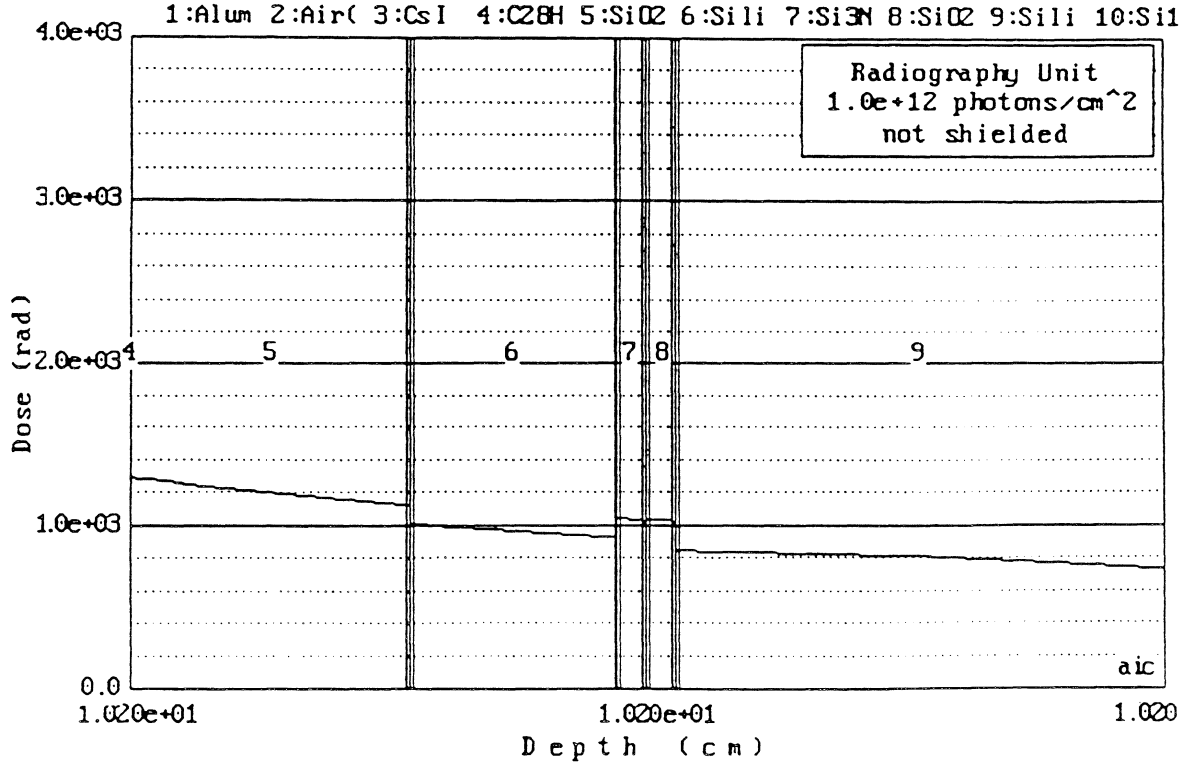
b) As above, but taking into account electron transport between layers.



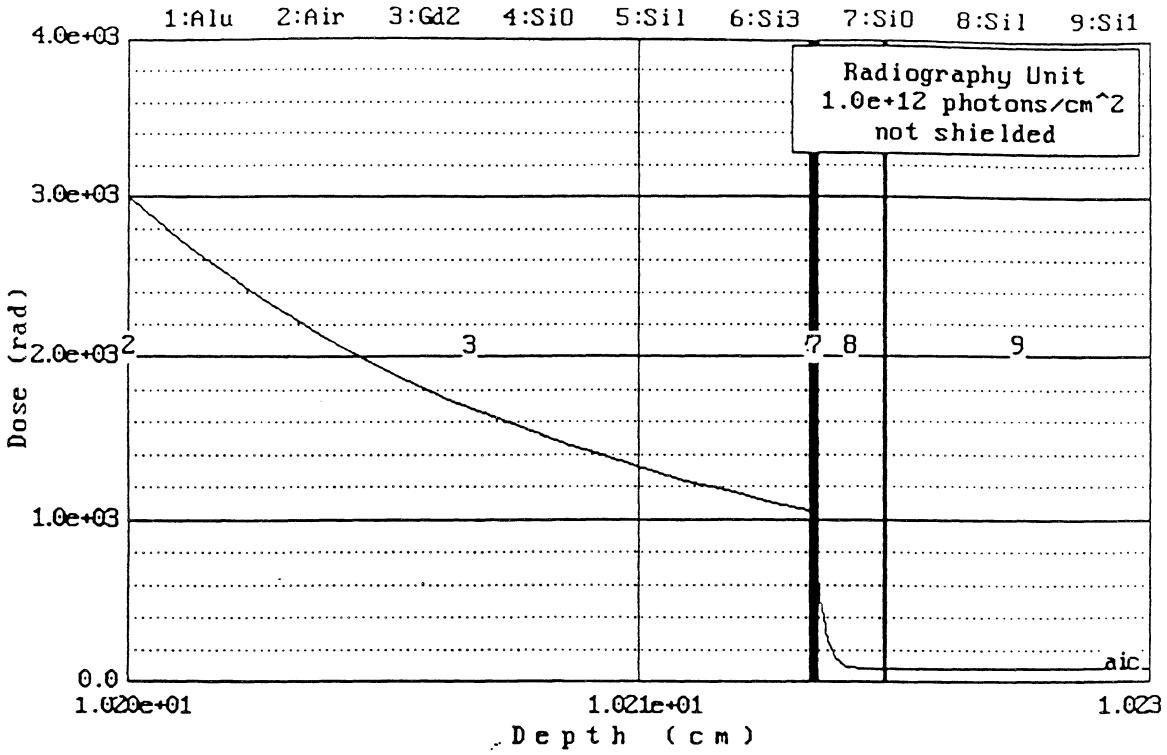
c) Irradiation by 70kVp x-rays. Relative dose through CsI(Tl) (layer 3), and epitaxial silicon (layer 9) of CsI(Tl) coated device



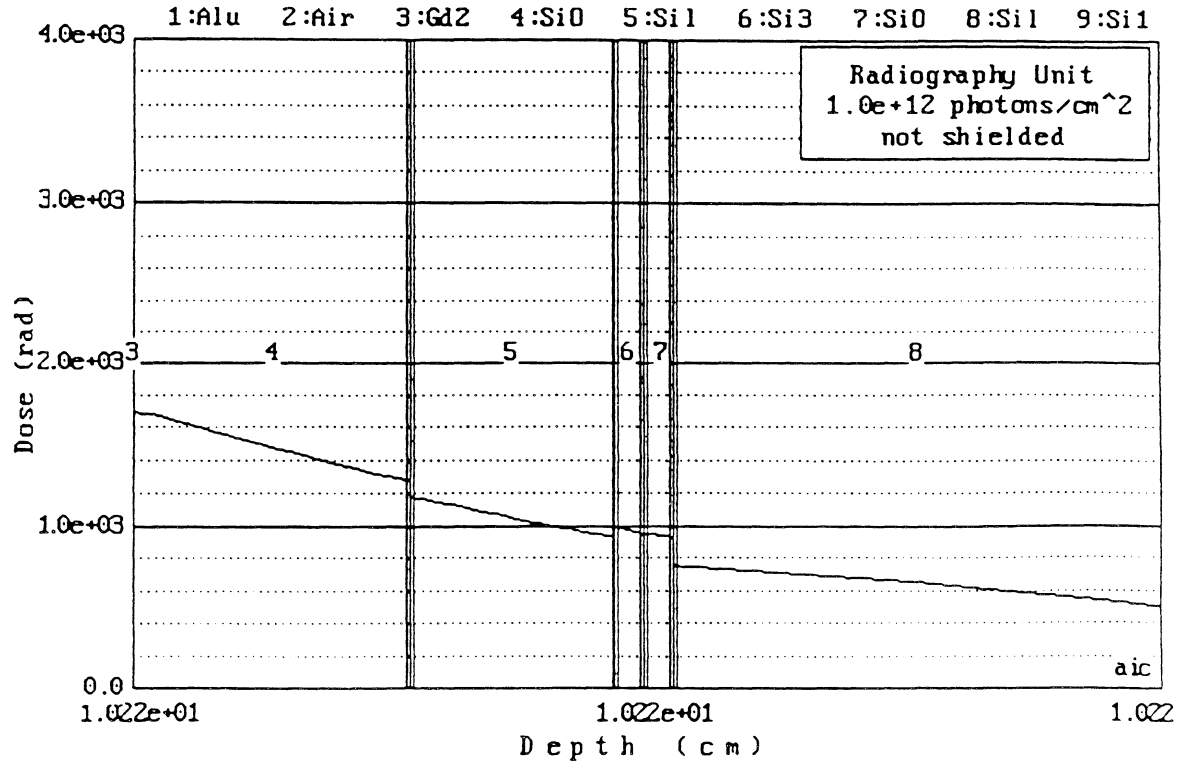
d) Expanded plot of above showing gate nitride (layer 7), gate oxide (layer 8), and epitaxial silicon (layer 9).



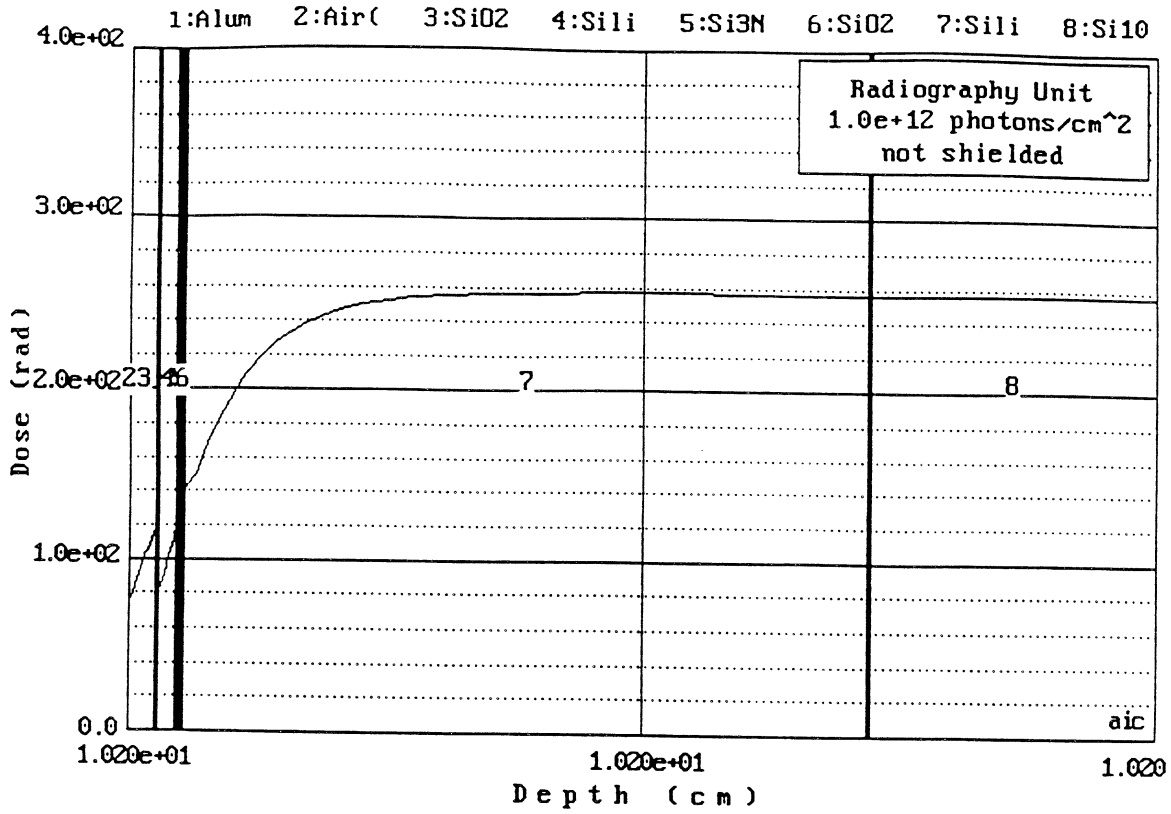
e) Irradiation by 70kVp x-rays. Relative dose through Gadox(Eu) (layer 3), and epitaxial silicon (layer 8) of Gadox(Eu) coated device.



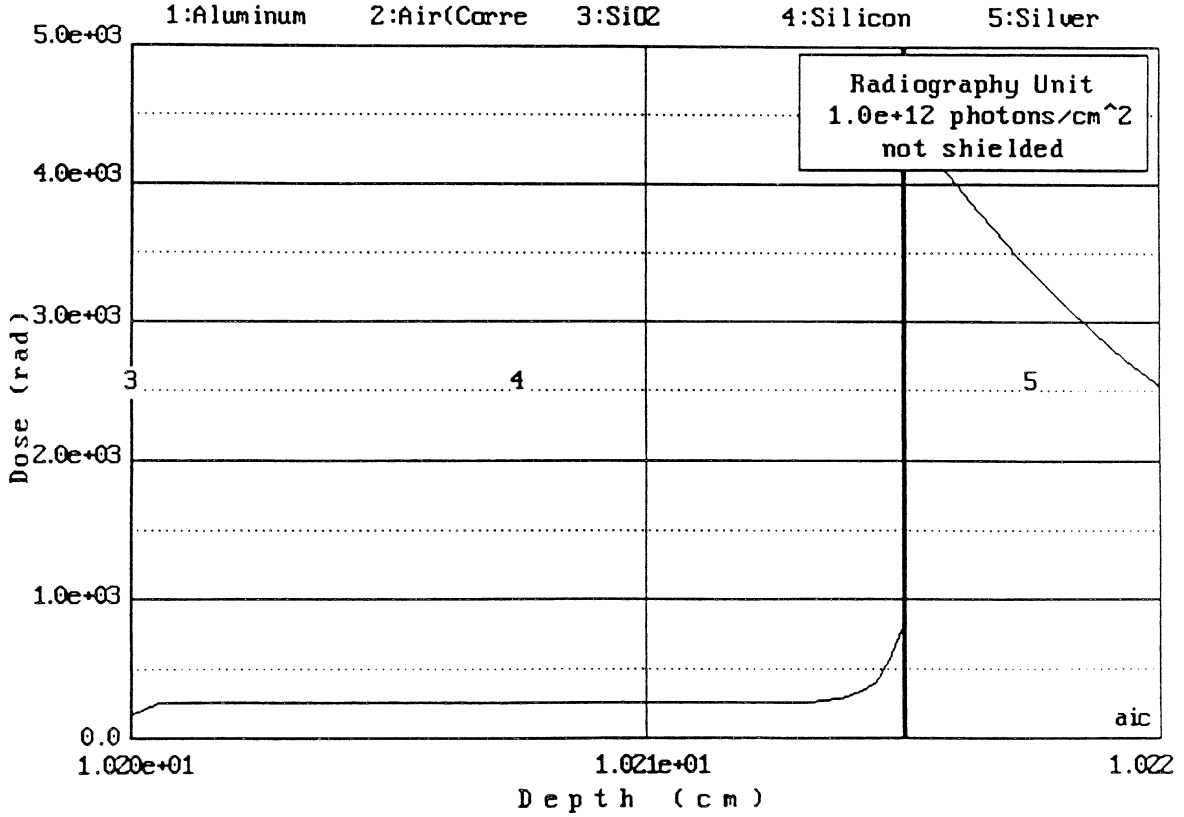
f) Expanded plot of above showing gate nitride (layer 6), gate oxide (layer 7), and epitaxial silicon (layer 8).



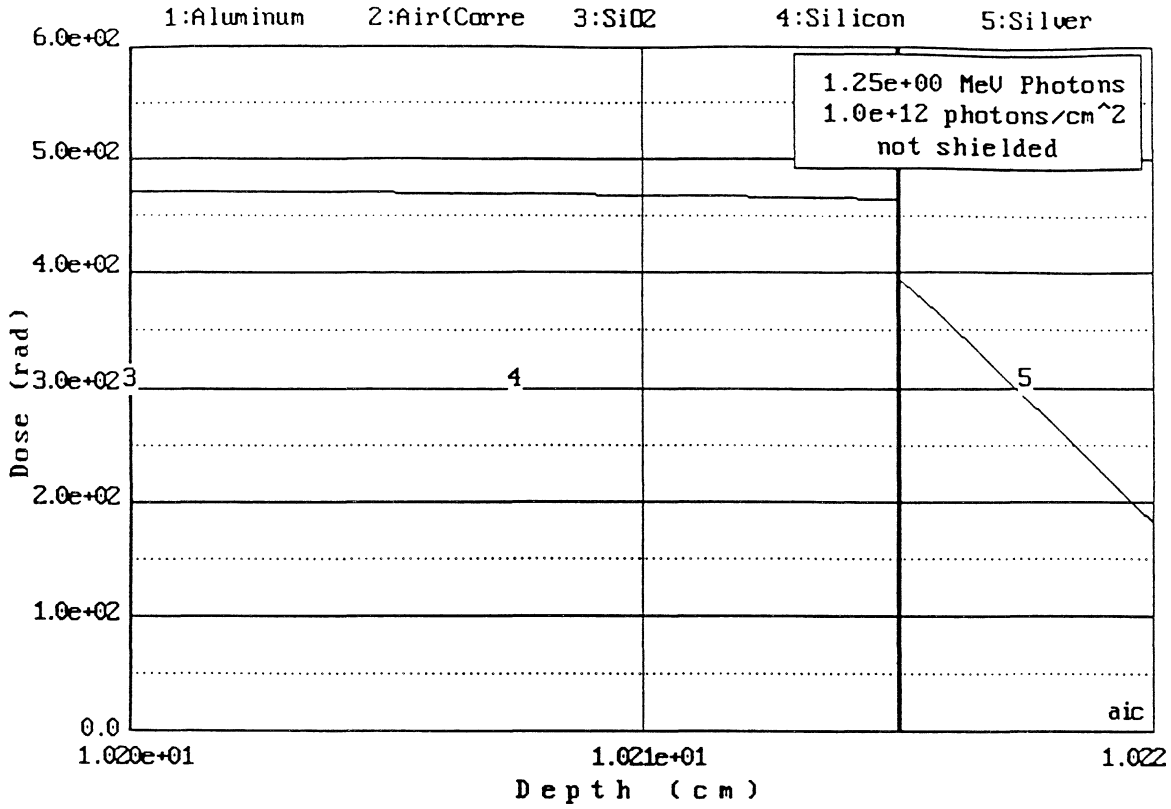
g) Irradiation by 70kVp x-rays. Relative dose through epitaxial silicon (layer 7) of conventional device.



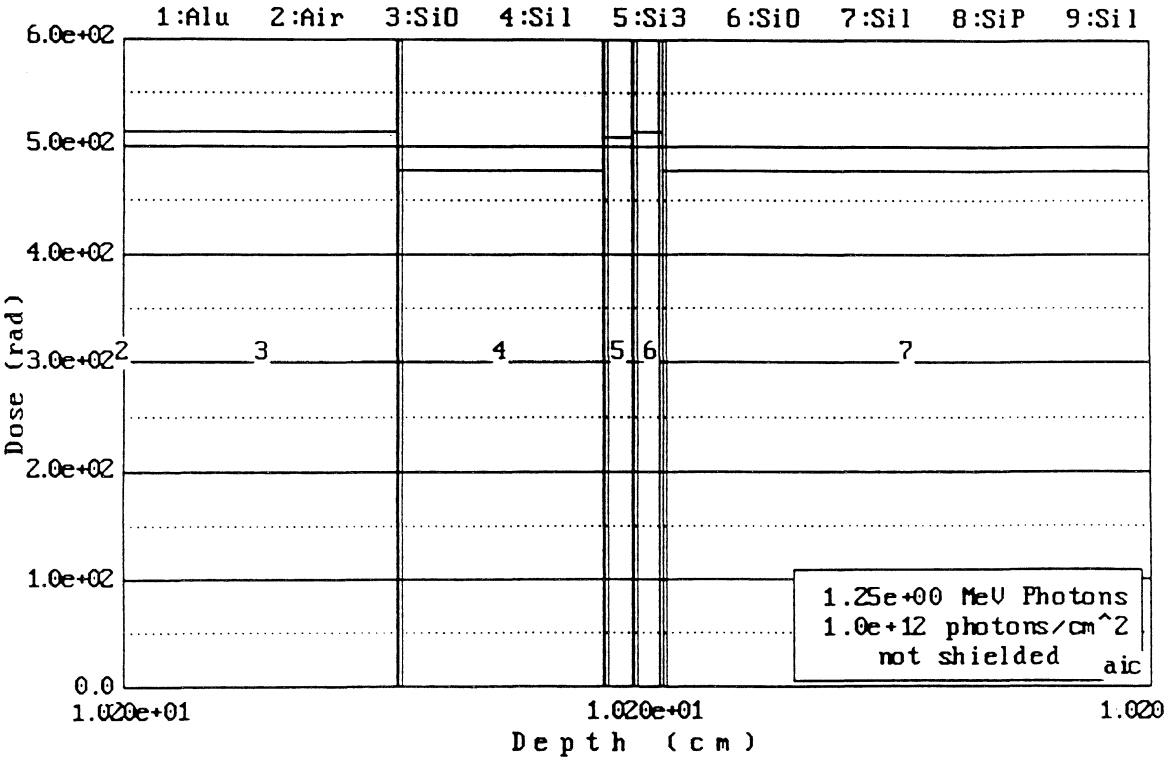
h) Irradiation by 70kVp x-rays. Relative dose through depletion region of PIN diode (layer 4)



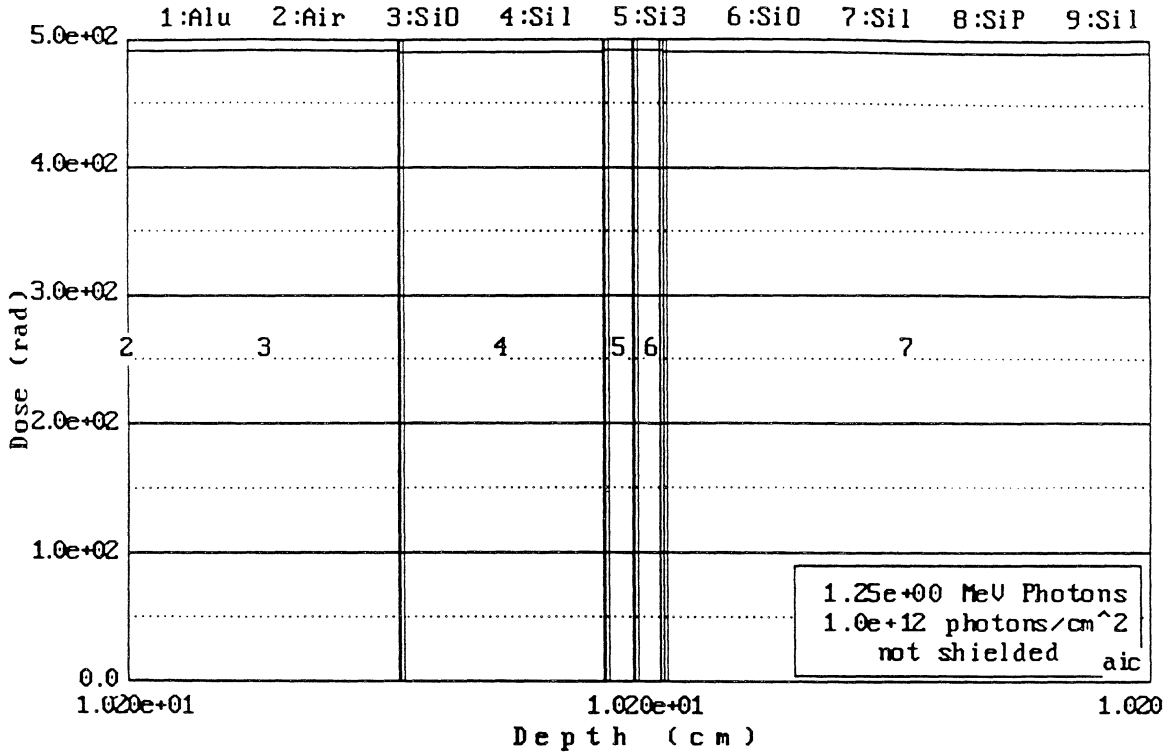
i) Irradiation by 1.25MeV gammas. Relative dose through depletion region of PIN diode (layer 4)



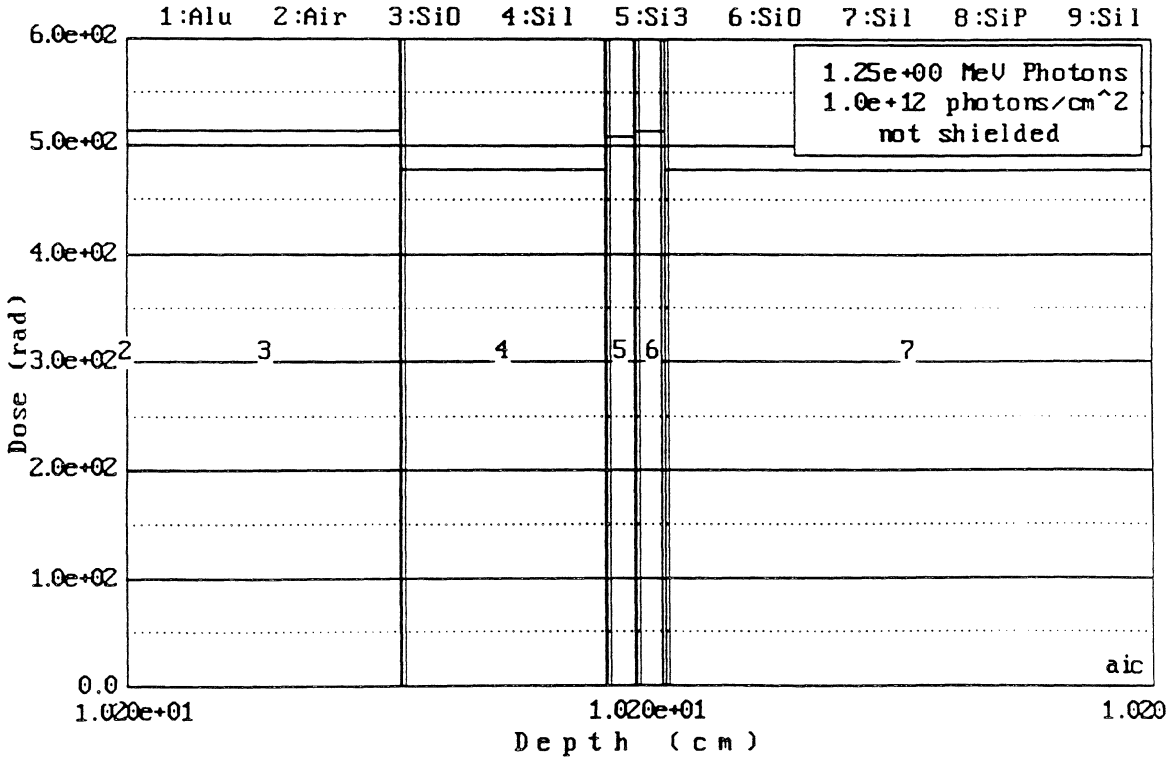
j) Irradiation by 1.25MeV gammas. Relative dose through gate nitride (layer 5), gate oxide (layer 6), and epitaxial silicon (layer 7) of a conventional CCD.



k) Irradiation by 1.25MeV gammas. Equilibrium dose (neglecting electron transport between layers) through conventional device. Layer 5 is the gate nitride, 6 is the gate oxide, and 7 is the epitaxial layers.



l) As above, but taking into account electron transport between layers.



Appendix 2. Analysis of Potential at Accumulated p-stop Surface.

1) Calculation of Surface Potential as Function of Gate Bias

For the case where the surface is accumulated, this calculation is complicated by the mutual interdependence of carrier density and potential. The expression which implicitly relates the gate bias to the surface potential is [1 p25];

$$Q_{sc}=\pm C_0\times(\frac{kT}{q})\times F(u_s,u_b) \qquad (1)$$

where Q_{sc} is the charge density per unit area (Cm^{-2}), k is Boltzmann's constant (Jk^{-1}), T is the temperature (K), C_0 is an effective semiconductor surface capacitance given by;

$$C_0=\sqrt{\frac{2q^2\epsilon_s n_i}{kT}}$$

where q is the electronic charge (C), ϵ_s is the dielectric permittivity of silicon ($C^2N^{-1}m^{-2}$), n_i is the intrinsic carrier concentration (m^{-3}),

and $F(u_s,u_b)$ is a function given by;

$$F(u_s,u_b)\equiv\sqrt{2}\times[(u_b-u_s)\sinh u_b-(\cosh u_b-\cosh u_s)]^{0.5} \qquad (2)$$

where u_s and u_b are dimensionless potentials defined by;

$$u_b\equiv\frac{q\phi_b}{kT} \quad , \quad u_s\equiv\frac{q\phi_s}{kT}$$

ϕ_b, and ϕ_s are the potential of the Fermi level with respect to the midgap, for the bulk and surface

respectively (see fig 1).

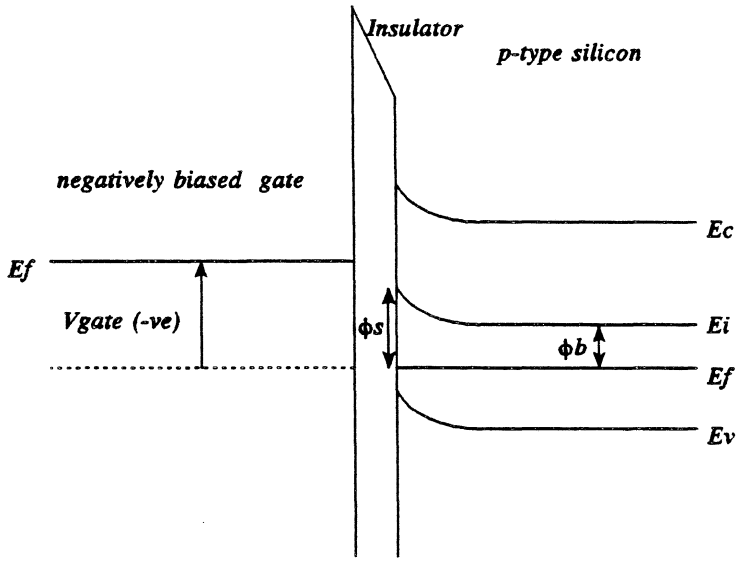


Fig 1. Potentials ϕ_b and ϕ_s.

It is not possible to calculate the potential barrier at the semiconductor surface (ϕ_s minus ϕ_b), directly as a function of gate bias, but by entering selected values for ϕ_b, and ϕ_s into equation (1), it is possible to determine the charge density at the silicon surface which corresponds to those potentials. Once the charge density is known it is possible to calculate the voltage drop across the insulator from its known capacitance, and then to determine the overall gate to substrate bias, as the sum of the insulator potential and the potential barrier.

2) Determination of Potential with Depth at an Accumulated Surface.

The potential ϕ_x, at a depth x into the silicon, is connected to the bulk potential ϕ_b and the surface potential ϕ_s, by equation 3 [2 p58];

$$\frac{x(m)}{\lambda_i} = \int_{u_s}^{u_x} \frac{du}{F(u_x, u_b)} \qquad (3)$$

where λ_i is called the intrinsic Debye length, and is given by;

$$\lambda_i(m) = \sqrt{\frac{\epsilon_s kT}{2q^2 n_i}}$$

with the units as for part 1.

By entering selected values of ϕ_b, ϕ_s, and ϕ_x into equation (3) and then solving numerically, the depth corresponding to the potential ϕ_x, is determined.

References for Appendix 2.

[1] J.T. Wallmark, and H. Johnson, "Field-Effect Transistors: Physics, Technology and Applications", Published by Prentice-Hall, 1966.

[2] E.H. Nicollian, and J,R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology", Published by John Wiley and Sons, 1982.