A cost effective harmonic cancellation method for high frequency Silicon Carbide MOSFET based single phase inverter

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***Abstract*-- This paper introduces a combinational modulation method to be used in classic full-bridge single phase inverters. The proposed method eliminates even-order harmonics at PWM stage in control section unlike the conventional method of even order harmonic cancelation in power stage and offers a cost effective design by switching one leg at high frequency. Using a low cost Digital Signal Controller (DSC) platform, regular sampling technique based on real time calculation was employed to verify the feasibility of the proposed method on a 500W single phase Voltage Source Inverter. Performance characteristics such as switching losses and harmonic distortions are presented for the new approach and compared with a classic inverter modulation method.**

***Index Terms*-- Combinational logic circuits, Harmonic distortion, Inverters, Pulse Width Modulation, Silicon Carbide, Switching frequency**

I. Nomenclature

F_0	Fundamental frequency (Hz)
F_S	Sampling frequency (Hz)
F_{SW}	Switching frequency across the load (Hz)
i_L	The instantaneous load current (A)
P_S	Switching power losses (W)
ΔP_S	Change in switching power losses (W)
THD_I	Total Harmonic Distortion for load current (%)
V_{DC}	Input DC voltage to inverter (V)
V_L	Voltages across load inductor (V)
V_R	Voltages across load resistor (V)
V_{XY}	Inverter output voltage across the load (V)
ζ	Efficiency of the inverter (%)

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II. Introduction

SINGLE phase inverters have numerous applications in industry. Various topologies and modulation methods have been proposed for single phase inverters [1]-[9]. Among the most common of these topologies is H-bridge. Over the past few decades, a number of modulation methods have been proposed, each with a set of objectives in mind [10]-[11].

Classic two high frequency leg operation method of even-order harmonic cancelation has been implemented in [12] where, both legs of the H-bridge are required to switch at ½ F_{SW} (i.e. half output load switching frequency), and even-order harmonic cancelation is applied at power stage. However, as explained in section IV, this method fails to fully remove the even-order harmonics. Moreover, this method requires four expensive high frequency switching devices.

In order to address the need for a cost effective solution, Three Level Discontinuous PWM (3-LDPWM) method was proposed [12]. In this modulation scheme the sinusoidal reference is modulated at high frequency in one leg of the H-bridge and the other leg switches at the fundamental sine wave frequency (i.e. 50Hz or 60Hz). As a result, switching losses are mainly generated in two of the four switching components [13]-[16]. Hence, by using high switching power components in one leg and low switching power components in the other leg, an economical design could be achieved. Despite cost effectiveness of 3-LDPWM method, the method was later abandoned due to its poor harmonic distortions, complexity of implementation and uneven switching loss distribution. Although nowadays transistors are capable of tolerating high switching loss dissipations and the issue of asymmetrical heat distribution is not as detrimental as it used to be, it seems that the inferior harmonic distortions of 3-LDPWM method results in the financial benefits of this method to be often overlooked in industry [17]-[21].

This paper aims to propose a novel modulation method which offers both the benefit of even-order harmonic cancelation of the Classic two leg high frequency operation method as well as cost effectiveness of 3-LDPWM method.

The novel feature of the proposed method is the use of combinational logic in the PWM control stage in order to achieve even order harmonic cancelation in single high-

frequency leg operation.

The presented method also benefits from low a component count compared to topologies such as multi-level inverters and interlaced inverters[22],[23].

In what follows, we aim to demonstrate that the proposed method is cost effective and can offer performance improvements over the 3-LDPWM method. Hence, we will compare the performance of the proposed method with the 3-LDPWM method. The classical two leg operation offers good performance but lacks cost effectiveness hence it will not be compared with proposed method.

Section III reviews principles and assesses harmonic distortions and switching losses of 3-LDPWM method [12], [24] and the proposed method. Section IV presents the mathematical principles of operation of the proposed modulation technique and its distinct benefits. Section V covers the detailed principle of operation of the proposed method. Section VI contains MATLAB simulations. Section VII includes the experimental setup and results. In section VIII the losses occurred in devices are calculated in details. Section IX discusses the issue of uneven switching loss distribution, and examines the sources of low order harmonic distortions. This section also compares and contrasts the cost of bill of material for classic, 3-LDPWM and the proposed methods.

III. Brief operation overview of 3-LDPWM and Proposed methods

3-LDPWM method involves applying discontinuous half sine wave reference based PWM to the high frequency switching leg as shown in Fig. 2 and a square wave at the fundamental frequency to the low frequency switching leg [24]. Effectively only two of the four switching devices need to deliver high frequency switching, which means cost effective alternative switching devices can be deployed for the low frequency switching leg. However, the very nature of this modulation method suffers from poor harmonic distortions particularly at low sampling frequencies. This will be discussed in section IV.

Similar to 3-LDPWM method, the proposed method has a low frequency square wave leg and a high frequency PWM leg. However, the proposed approach subtracts two pure sinusoidal reference signals, which are out of phase by π radian, at Pulse Width Modulation (PWM) stage using a combinational logic circuit hence removing the even order harmonics. The proposed method presents two salient benefits which are discussed in the following section.

IV. Benefits of the proposed method compared to 3-LDPWM method

A. Even-order harmonic cancelation

Even-order harmonic cancelation has been implemented before [12] where, both legs of the H-bridge are required to switch at ½ F_{SW} and even-order harmonic cancelation is applied at power stage but this method fails to fully remove the even-order harmonics [12].

The most salient feature of the proposed method is its capability of achieving better harmonic distortion and a lower THD through even-order harmonic cancelation using only one leg of the H-bridge at high frequency as well as offering a better cancelation compared to classical two high frequency leg operation method[12].

The proposed method achieves even-order harmonic cancelation by subtracting two PWM signals whose references are anti-phase sine waves. If a signal is shifted by π radian and subtracted from the original value, the odd order harmonics of the Fourier Transform describing the signal sustains and the even part cancels out. This can be demonstrated mathematically as follows:

Consider the general function for discrete Fourier Transform as given in (1).

$$X(e^{j\omega}) = \frac{1}{2\pi}\sum_{n=-\infty}^{+\infty} x[n]e^{-j\omega n} \quad (1)$$

The frequency components can be further split into even-order and odd-order harmonics:

$$X(e^{j\omega}) = \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty}\left(x[2k]e^{-j\omega(2k)} + x[2k+1]e^{-j\omega(2k+1)}\right) \quad (2)$$

$$X(e^{j\omega}) = \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k]e^{-j\omega(2k)} + \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k+1]e^{-j\omega(2k+1)} \quad (3)$$

If the signal in (3) is shifted by π radian we have:

$$X\left(e^{j(\omega+\pi)}\right) = \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k]e^{-j(\omega+\pi)(2k)} + \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2K+1]e^{-j(\omega+\pi)(2k+1)} \quad (4)$$

$$X\left(e^{j(\omega+\pi)}\right) = \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2K]e^{-j\omega(2k)}e^{-j(2\pi k)} + \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2K+1]e^{-j(\omega)(2k+1)}e^{-j(2\pi k)}e^{-j\pi} \quad (5)$$

Since for integer k where $-\infty < k < +\infty$

$$e^{-j(2\pi k)} = 1$$
$$e^{-j\pi} = -1$$

We have

$$X\left(e^{j(\omega+\pi)}\right) = \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[k]e^{-j\omega(2k)} - \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k+1]\,e^{-j(\omega)(2k+1)} \quad (6)$$

Hence after π radian shift the even order harmonics remain unchanged and odd order harmonics are made negative. The shifted signal is subtracted from the original version in (7).

$$X(e^{j\omega}) - X\left(e^{j(\omega+\pi)}\right) = \left(\frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k]e^{-j\omega(2k)} + \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k+1]\,e^{-j(\omega)(2k+1)}\right) - \left(\frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k]e^{-j\omega(2k)} - \frac{1}{2\pi}\sum_{k=-\infty}^{+\infty} x[2k+1]\,e^{-j(\omega)(2k+1)}\right)$$

$$X(e^{j\omega}) - X\left(e^{j(\omega+\pi)}\right) = \frac{1}{\pi}\sum_{k=-\infty}^{+\infty} x[2k+1]e^{-j\omega(2k+1)} \quad (7)$$

As shown in (7) after subtracting the shifted by π radian version of a signal from the original signal, the even order harmonics are canceled and the odd order harmonics are sustained.

However, in practice it is very difficult to achieve exactly π radian phase shift for all the frequency components of a signal and maintain that throughout the drive circuit and apply it to the switching devices. This is due to a non-zero group delay on the signal path which results in phase distortions and consequently some of the even-order harmonic components have a phase delay slightly greater or smaller than π radian. As a result, full cancelation cannot be achieved in practice if subtraction is performed at power stage which is suggested in [12]. On the other hand, the proposed method alleviates this inevitable effect by performing harmonic cancelation at logic level using a fast combinational logic circuit which compared to cancelation at power stage considerably reduces the group delay of the two reference signals hence enhancing the cancelation capability of the inverter. As a result, compared to previous harmonic cancelation methods in H-bridge inverters [12], the proposed method can achieve better even-order harmonic cancelation as well as operating one leg at high frequency, which allows the transistors in the other leg to be low switching frequency components.

B. Narrow reference signal bandwidth

The harmonic distortion of the inverter at low sampling frequencies heavily depends on the bandwidth of the sampled reference signal. The proposed method uses two pure sine waves as the reference signals of the PWM pulses which have very narrow bandwidth. However, in the 3-LDPWM method, the reference signal consists of two discontinued half-sine waves between 0 to π radian and π to 2π radians and there are abrupt changes in the reference signal at 0 and π radian as shown in Fig. 10b which introduce high frequency components to frequency spectrum of the PWM reference signal hence increasing its bandwidth.

The harmonic spectra of the reference signals of 3-LDPWM method and the proposed method can be compared by studying the Discrete-Time Fourier Transform (DTFT) of their references. The reference signal in 3-LDPWM method is constructed as the sum of a sine wave with a square wave at fundamental frequency (50Hz) as shown in (8)

$$f(t) = \sin(\omega t) + g(\omega t) \tag{8}$$

Where $g(\omega t)$ is a square wave which can be written as the sum of two Heaviside step functions as:

$$g(\omega t) = H(\omega t) - H(\omega t - 1) \tag{9}$$

Hence, the DTFT of the reference can be calculated as:

$$F[e^{j\omega}] = \sum_{n=-\infty}^{\infty} f[n]e^{-j\omega n} \tag{10}$$

$$F[e^{j\omega}] = \sum_{n=-\infty}^{\infty} (\sin[n] + g[n])e^{-j\omega n} \tag{11}$$

$$F[e^{j\omega}] = \sum_{n=-\infty}^{\infty} \sin[n]\, e^{-j\omega n} + \sum_{n=-\infty}^{\infty} g[n]e^{-j\omega n} \tag{12}$$

Hence, the expression at (12) can be evaluated as two DTFTs of a sine function and a square wave function as follows [12]:

$$F[e^{j\omega}] = \pi \sum_{k=-\infty}^{\infty} [\delta(\omega - \omega_0 - 2\pi k) - \delta(\omega + \omega_0 + 2\pi k)] + \frac{4}{\pi} \sum_{k=-\infty}^{\infty} \frac{\sin((2k-1)2\pi\omega t)}{2k-1} \tag{13}$$

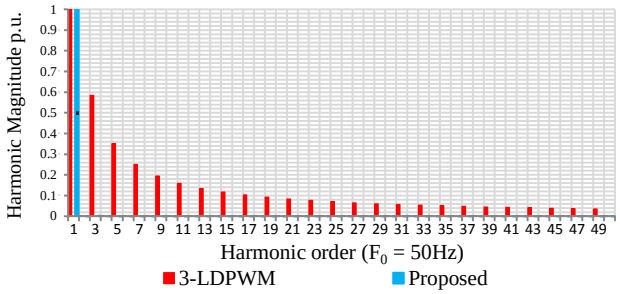


Fig. 1. Harmonic distortion of reference signals of the proposed and 3-LDPWM methods. Higher harmonics distortions are visible for 3-LDPWM method

It can be seen that the frequency contents of the reference signal for the 3-LDPWM method comprise of the frequency contents of a sine wave and a square wave. At the baseband, it contains two Dirac spikes at the positive frequency and the negative frequency for the sinusoidal component and all the odd order harmonics which are the results of the square waveform part of the signal.

The reference signal for the proposed method is sinusoidal and hence the frequency components can be described as (14) [12]:

$$F[e^{j\omega}] = \pi \sum_{k=-\infty}^{\infty} [\delta(\omega - \omega_0 - 2\pi k) - \delta(\omega + \omega_0 + 2\pi k)] \tag{14}$$

This is identical to the first part of (13). Hence, the baseband harmonic contents of the 3-LDPWM method are wider than those of the proposed method due to the square wave component of the reference signal in the 3-LDPWM method. This is shown in Fig. 1 where the frequency domain representation of the reference signals for the proposed and 3-LDPWM methods are plotted adjacent to each other to allow for comparison.

When sampling at low frequencies, due to the wide bandwidth of the reference signal of 3-LDPWM method, it is impossible to satisfy the Nyquist sampling criterion for perfect reconstruction. As a result, aliasing noise is introduced to the sampled reference signal [25]. On the other hand, in the proposed method, the reference signals are pure sine waves and have narrow bandwidths; hence perfect reconstruction can be achieved even at low sampling frequencies. As a result, the proposed method has a considerably better harmonic distortion at low sampling frequencies compared to 3-LDPWM method as will be demonstrated by simulation and experimental results in sections VI and VII.

V. Operation of Proposed Method

A. Principle of operation of the control section

Similar to 3-LDPWM method, the proposed method applies a square wave signal at the fundamental frequency to the low switching frequency leg and a high frequency PWM is applied to the high switching frequency leg. Contrary to 3-LDPWM method, the proposed method reduces harmonic distortions through even-order harmonic cancellation at PWM stage at

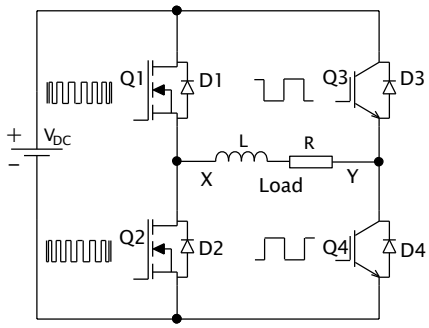


Fig. 2. H-bridge single phase inverter

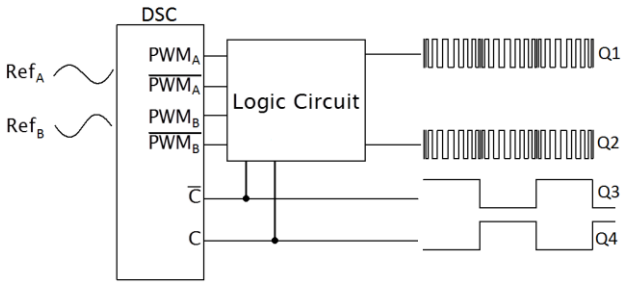


Fig. 3. Control curcuit for the proposed method with gate signals to four transistors in H-bridge from logic circuit and DSC

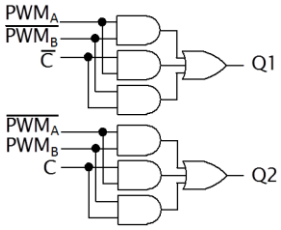


Fig. 4. Detailed proposed logic circuit

logic control section. To achieve this, two antiphase regularly sampled sinusoidal reference signals Ref_A and Ref_B are generated and are compared internally with triangular waveform carriers using the PWM channels of the DSC to generate PWM_A and PWM_B as shown in Fig. 3. Using a combinational logic control circuit which comprises of three AND gates and one OR gate, PWM_B is subtracted from PWM_A to generate gate pulses to Q1 as shown in Fig. 4. The two pulse trains which drive Q1 and Q2 in high frequency leg are formulated in (15) and (16). In low frequency leg, Q3 and Q4 are driven directly from the square wave signals as shown in Fig. 3.

$$Q1 = PWM_A\overline{PWM_B} + PWM_A\bar{C} + \overline{PWM_B}\bar{C} \quad (15)$$

$$Q2 = \overline{PWM_A}PWM_B + \overline{PWM_A}\,C + PWM_BC \quad (16)$$

Where PWM_A and PWM_B are the PWM pulses and C is the square wave all of which are generated by the DSC and fed into a logic circuitry as shown in Fig. 4.

By comparing (15) and (16) it can be seen that expression for (16) can be achieved by inverting (15). However, in order to avoid cross conduction, it is a common practice to allow for deadbands in the switching patterns of the complementary switches in inverter legs [12]. The DSC used in this paper is equipped with deadband facility in its complementary PWM

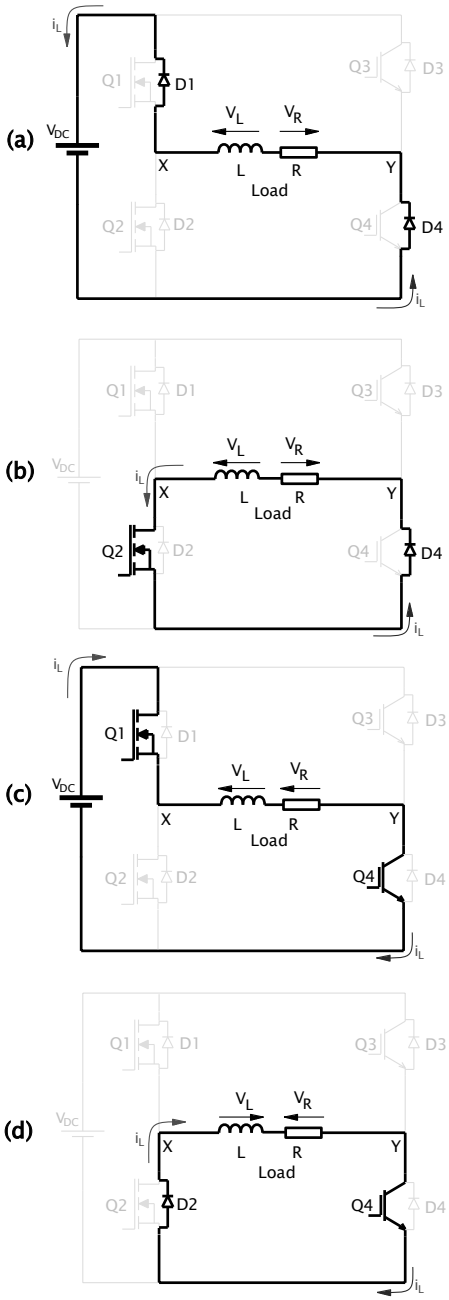


Fig. 5. Current loops in various states in positive half cycle (a) state 1: current flows through D1 and D4 (b) state 2: current flows through D4 and Q2 (c) state 3: current flows through Q1 and Q4 (d) state 4: current passes through D2 and Q4

TABLE I. PWM AND CORRESPONDING VOLTAGES ACROSS THE LOAD

C	PWM_A	PWM_B	V_{XY}	Q1	Q2	Q3	Q4
1	1	1	0	0	1	0	1
1	1	0	$+V_{DC}$	1	0	0	1
1	0	1	0	0	1	0	1
1	0	0	0	0	1	0	1
0	1	1	0	1	0	1	0
0	1	0	0	1	0	1	0
0	0	1	$-V_{DC}$	0	1	1	0
0	0	0	0	1	0	1	0

TABLE II. PROPOSED CIRCUIT OPERATION STATES FOR ONE CYCLE

One Complete Cycle Operation							
Positive half cycle				Negative half cycle			
Q3 = OFF, Q4 = ON				Q3 = ON, Q4 = OFF			
Region 1		Region 2		Region 3		Region 4	
$V_L = +V_{DC}$, $-i_L$		$V_L = +V_{DC}$, $+i_L$		$V_L = -V_{DC}$, $+i_L$		$V_L = -V_{DC}$, $-i_L$	
State1	**State2**	**State3**	**State4**	**State5**	**State6**	**State7**	**State8**
Q1=H Q2=L	Q1=L Q2=H	Q1=H Q2=L	Q1=L Q2=H	Q1=H Q2=L	Q1=L Q2=H	Q1=H Q2=L	Q1=L Q2=H

channels [31]. By using the DSC's complementary channel of PWM_A for $\overline{PWM_A}$ and the complementary channel of PWM_B as $\overline{PWM_B}$ in expressions for Q1 and Q2, the appropriate deadbands can be generated. Subtraction of reference signals at PWM stage can be perceived through the observation that the instantaneous voltage across the load can have one of the three values: $+V_{DC}$, $-V_{DC}$ or zero, where zero represents the freewheeling operation of the circuit. Table I shows all the possible combinations and the resulting voltages across the load i.e. V_{XY} in Fig. 2.

If Q1 and Q3 or Q2 and Q4 are both turned on or both turned off, the voltage across the load will be zero. If Q1 and Q4 are turned on, the voltage across the load will be $+V_{DC}$ and it will be $-V_{DC}$ if Q2 and Q3 are turned on. At no instance should the transistors of one leg be turned on simultaneously. The signal C is high during the positive half cycle and low during the negative half cycle. The expression for Q1 comprises of three terms. The first term implements the pulse trains for Q1 for its positive half-cycle interval and the other two terms constitute the pulse trains to Q1 for its negative half-cycle interval. The same explanation is valid for Q2.

B. Principle of operation of power section

The operation of the proposed method is divided into two half cycles and each half cycle comprises of two stages of operation. The positive half cycle is characterized with Q3 turned off and Q4 turned on and the voltage across the load pulsating to $+V_{DC}$. Tables I and II summarize the operation for various regions and states for the proposed method for one cycle of operation.

In regions 1 and 3, current through the load (i_L) has the opposite direction with respect to the direction of the switched DC voltage across the load. In regions 2 and 4, the current and the switched DC voltage have the same directions. During region 1 with the switched DC voltage across the load in its positive half cycle, and the load current still in its negative half cycle, state 1 takes place with Q1 turned on and Q2 turned off, the load current takes the path shown in Fig. 5(a). State 2 takes place with Q1 turned off and Q2 turned on hence current loop shown in Fig. 5(b) is developed. During the whole region 1, states 1 and 2 occur continuously and by doing so, the sinusoidal waveform nature of the load current is maintained. At the end of region 1, the value of load current reaches zero and region 2 starts. At the start of region 2, the positive switched DC voltage still exists across the load with a positive current flowing through the load in the direction from node X to node Y. State 3 occurs when Q1 is turned on and Q2 is turned off as shown in Fig. 5(c). State 4 takes place with Q1 turned off and Q2 turned on as shown in Fig. 5(d). At the end of region 2, the direction of the switched DC voltage changes from positive half cycle to negative half cycle with Q3 turned on and Q4 turned off. States 5 and 6 in region 3 and states 7 and 8 in region 4, follow the similar analysis as for states 1 and 2 in region 1 and states 3 and 4 in region 2 respectively but with current and the switched DC voltage being in the reverse directions.

During states 1, 2 and 4, the energy stored in the magnetic field of inductor section of the load is responsible for the current path formed in Fig. 5(a) which has a regenerative nature and in Fig. 5(b) and Fig. 5(d) which constitute to freewheeling paths. Fig. 5(c) shows the current path that stores magnetic energy in the inductor L which corresponds to state 3 in Table II.

VI. SIMULINK SIMULATION RESULTS

The proposed and 3-LDPWM methods were simulated in MATLAB Simulink in order to observe and contrast their practical performance with the ideal case. Fig. 6 shows the output voltage and current for the inverter using the proposed method for a load switching frequency of 3kHz, where regions 1 to 4 in Table II are marked. In the simulation setup the load consisted of a 37mH inductor in series with a 27Ω resistor. All components were assumed ideal and IGBTs and SiC MOSFETs with anti-parallel diodes were used as switching devices. Input dc voltage was 185V and $F_S = F_{SW}$ was varied from 1kHz to 6kHz while keeping $F_0 = 50$Hz.

Fig. 7 depicts simulation results for the harmonic spectra for various switching frequencies across the load for both 3-LDPWM method and the proposed method. The THD_I of the output current is shown in parentheses for each method. It is apparent that the load current harmonic spectra for the proposed method present better harmonic distortion compared to 3-LDPWM method. This is due to even order harmonic cancelation in the proposed method.

As observed in Fig. 7 (b) the harmonic distortions of both 3-LDPWM method and the proposed method are relatively low. This is due to higher sampling rate of the reference signal. The parameters affecting the harmonic distortions of the inverter will be further discussed in section IX.

Waveforms (a)-(d) in Fig. 8 show the simulation pulse trains for PWM_A, PWM_B, square wave C and the resultant gate pulses to Q1 according to (15) respectively. PWM_A and

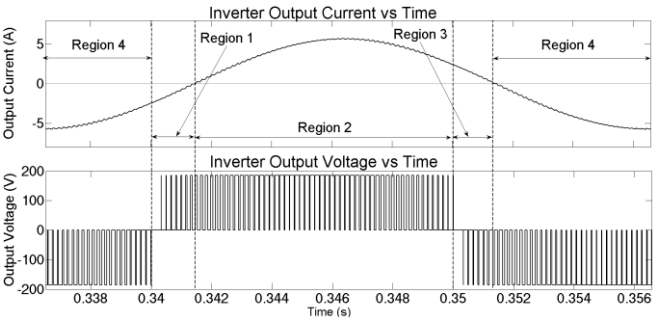


Fig. 6. Simulated inverter output voltage and load current versus time (Power Factor = 0.91)

PWM_B are constructed based on sinusoidal references Ref_A and Ref_B and are scaled such that their duty cycles approach to 100% at $\pi/2$ radians and 0% at $3\pi/2$ radians. At multiples of π radian, the duty cycles for PWM_A and PWM_B equate to 50% and they effectively cancel out one another when subtracted resulting in a no-pulse area which is shaded in Fig. 8. This quiet time is not to be confused with the blanking time compensation method [26] where blanking time error is compensated in PWM reference signals to improve the harmonic distortion of the inverter. The proposed method in this paper uses harmonic cancelation through subtraction of antiphase references and the quiet times are the mere effect of the subtraction. Although it is possible to further improve the harmonic distortion of the inverter by using blanking time compensation method in addition to the proposed method, the performance of the proposed method was intended to be studied on its own merits independent of any other classic improvements.

VII. Experimental Results

A 500W single phase H-bridge inverter setup shown in Fig. 9 was built to test the feasibility of the proposed method. Experiments were conducted on both 3-LDPWM and the proposed methods and the results were compared.

Experiment setup description:

Output Load:	27Ω in series with 37mH
Input Voltage (V_{in}):	185V DC
Load Current (I_L):	≈4A Sinusoidal
Output Measured Power (P_O):	500W
Load Switching Frequency (F_{sw}):	Varied from 1kHz to 20 kHz
Modulation Index (M):	0.9
Harmonics Measured	Up to 50th order harmonic

A. Reference signal construction

For simplicity, symmetric regular sampling was chosen for all experiments as only one sample per carrier triangular interval is required. It has been shown in [13] that for high switching frequencies there is barely any difference between symmetric and asymmetric regular sampling methods regarding harmonic distortions [27] - [30].

Figs. 10(a) and 11(a) show the experimental modulating reference signals construction. The upper traces shown by channel CH1 in Figs. 10(a) and 10(b) show the modulating reference signals for 3-LDPWM method which were obtained by regularly sampling technique at $F_S = F_{SW}$ = 1kHz and 6kHz respectively. The reference signals were compared with center-aligned triangular carriers within the DSC and the outputs were trains of PWM pulses to Q1 shown by the lower traces in channel CH2. It is evident that with increasing sampling frequency F_S, the modulating reference signal becomes more symmetrical for 3-LDPWM method which will be further discussed in section IX.

CH1 in Fig. 11(a) represents the modulating reference signal Ref_A for the proposed method which was constructed by the application of regular sampling method at $F_S = F_{SW}$ = 1kHz. This modulating reference signal is then compared with a center-aligned triangular waveform within the DSC. The output is a train of pulses, PWM_A as shown by channel CH2 in Fig. 11(a). During experimental tests, in order to illustrate how the gate pulses to Q1 in (15) were constructed, Fig. 11(b) was used to show PWM_A, PWM_B, the square pulse C signals and the gate pulses in (15) for Q1 for the proposed method by channels CH1, CH2, CH3 and CH4 respectively.

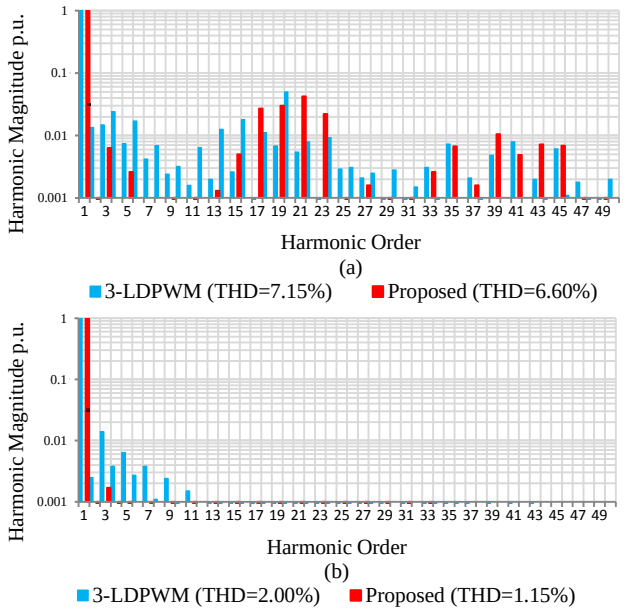


Fig. 7. Simulation results for load current harmonic spectra for 3-LDPWM vs Proposed method for switching frequency across the load of (a) $F_S = F_{SW}$ = 1kHz and (b) $F_S = F_{SW}$ = 6kHz

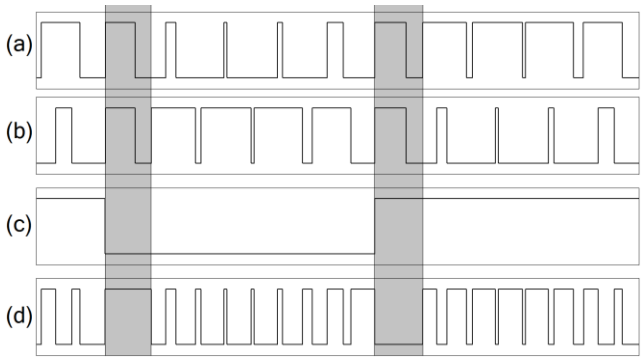


Fig. 8. Simulation waveform patterns for (a) PWM_A (b) PWM_B (c) C square wave (d) the Q1 drive signals according to (1)

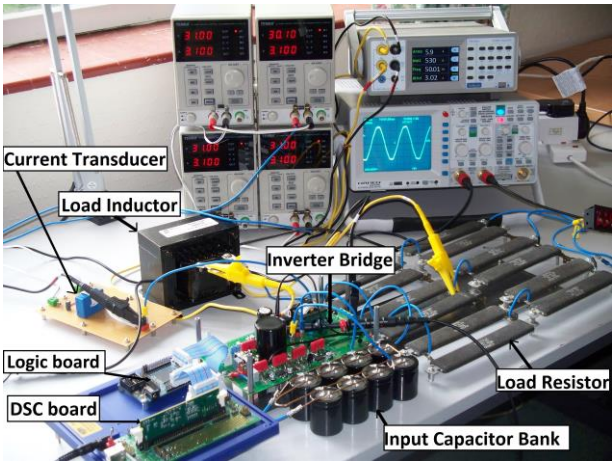
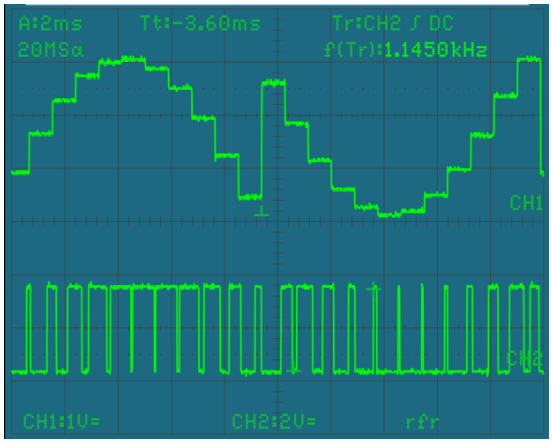
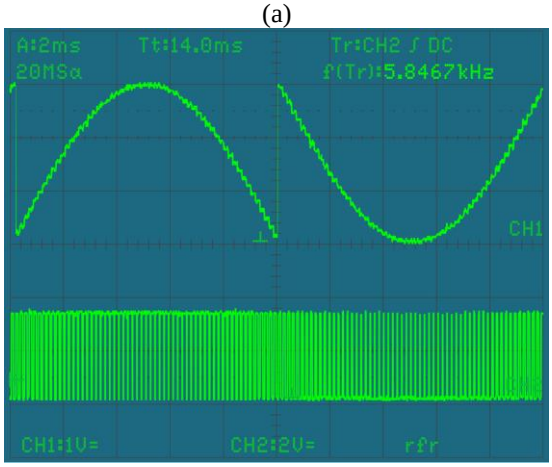


Fig. 9. Experimental setup showing the 500W single phase inverter

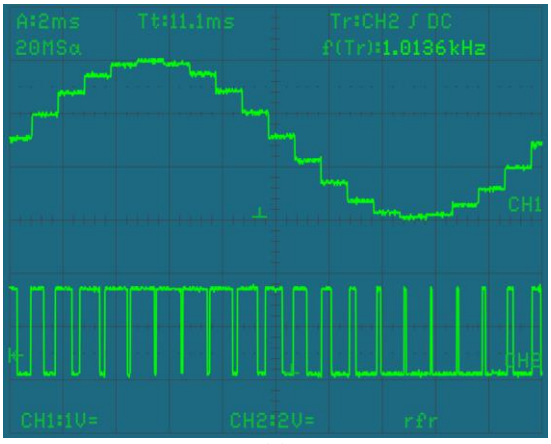


(a)

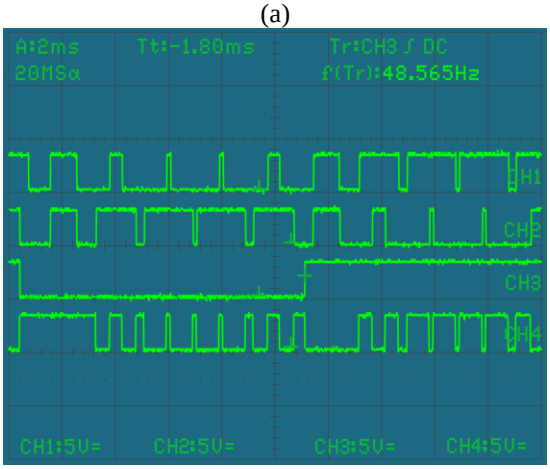


(b)

Fig.10. CH1 shows the reference signal for 3-LDPWM method and CH2 shows the corresponding gate pulses (a) at $F_S = F_{SW} = 1$kHz (b) at $F_S = F_{SW} = 6$kHz



(a)



(b)

Fig. 11. Construction of the modulating reference signal for the proposed method (a) CH1 and CH2 show the reference signal Ref_A sampled at 1kHz and the corresponding PWM_A pulse train respectively (b) CH1 and CH2 show PWM_A and PWM_B at 500Hz respectively and CH4 shows the resultant PWM after combinational logic at 1kHz.

CH4 in Fig. 11(b) contains no-pulse regions that correspond to the shaded areas in Fig. 8, which are responsible for the zero voltage periods in V_{XY} in Fig. 12 shown by CH3 at the vicinity of zero crossing point. The subtraction function of two PWM pulses with gradually incrementing and decrementing duty cycles ensures a smooth cross over from the negative half cycle to the positive half cycle and results in a smoother sinusoidal current waveform for the proposed method compared to the 3-LDPWM method as shown by channel CH1 in Figs. 13 and 14 in the vicinity of zero crossing for V_{XY}.

B. Testing and extracting results for the proposed method

Since the objective of this paper is to propose a cost effective modulation method to improve the THD figure, independent from increasing the load switching frequency, the study of effects of increasing F_{SW} above F_S is beyond the scope of this paper. Therefore, throughout the experiments, sampling frequency (F_S) was kept equal to the load current switching frequency (F_{SW}) for both methods. The experiments were conducted between 1kHz and 20kHz as shown in Fig. 16.

Construction of the output voltage of the inverter V_{XY}, is shown by Fig. 12 where CH1 shows the voltage at node X and CH2 shows the voltage at node Y relative to the negative supply rail of the input DC bus respectively and CH3 shows

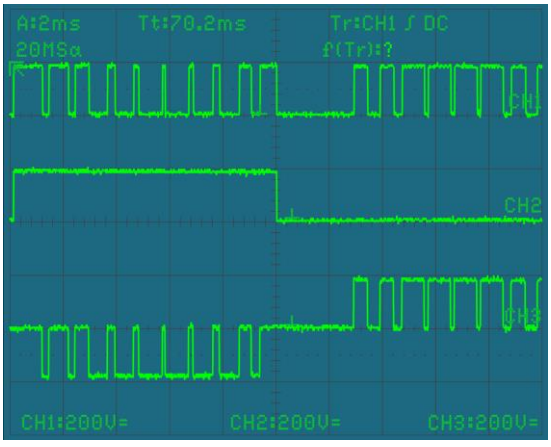
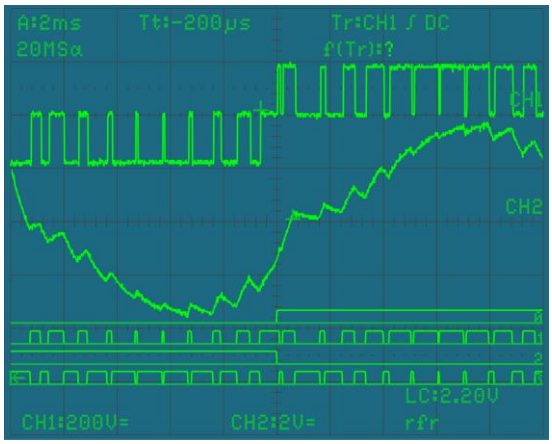


Fig. 12. CH1 and CH2 show the voltages between node X and node Y relative to the negative rail bus respectivly. CH3 shows the voltage across the load (i.e. V_{XY}) at full output load for the proposed method

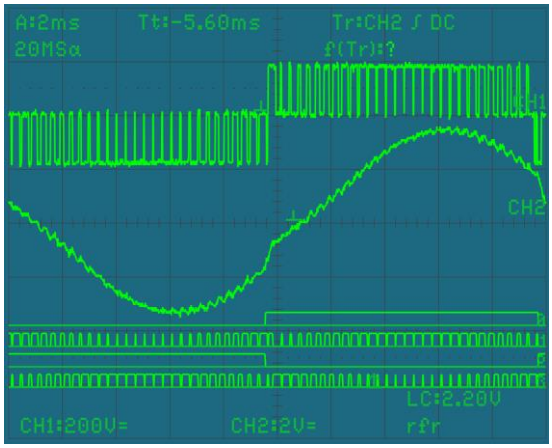
the voltage V_{XY} across the load for the proposed method.

Figs. 13 and 14 demonstrate the effect of increase in F_S and F_{SW} on the output load current quality where CH1 shows the switched output voltage V_{XY} and CH2 shows the output load current and the four channels of logic analyzer, Ch0, Ch1, Ch2 and Ch3 show gate pulses to Q4, Q1, Q3 and Q2, in H-bridge

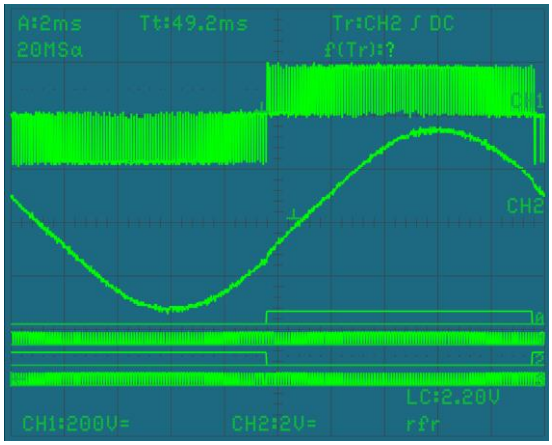
inverter in Fig. 2, respectively for both the proposed and the 3-LDPWM methods. The quantitative comparison of harmonic distortions is presented in Fig. 15.



(a)



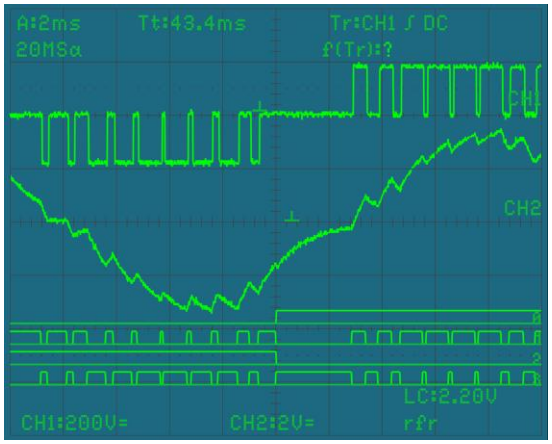
(b)



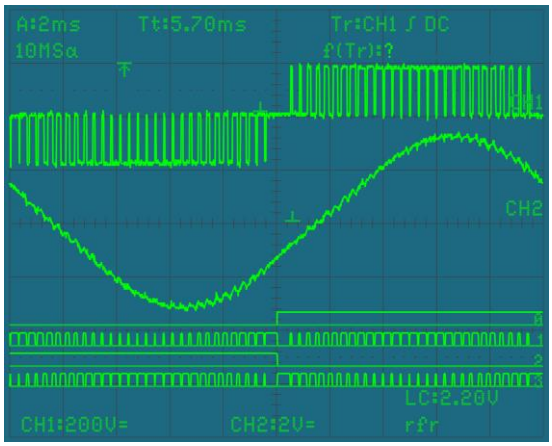
(c)

Fig. 13. CH1 shows switched voltage across load (V_{XY}) and CH2 shows load current iL for Discontinious method. Digital channels Ch0, Ch1, Ch2 and Ch3 show gate pulses to Q4, Q1, Q3 and Q2 respectively. (a) FS = F_{SW} = 1 kHz (b) F_S = F_{SW} = 6 kHz (c) F_S = F_{SW} = 10 kHz.

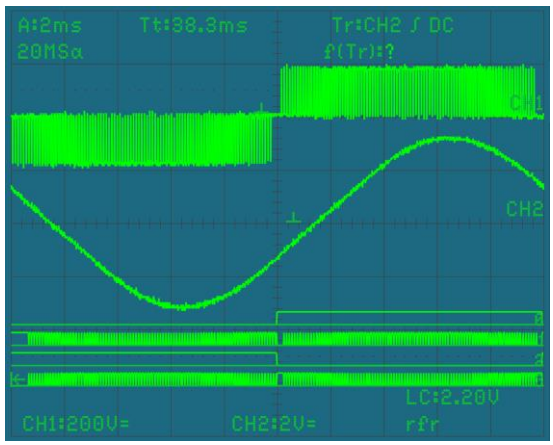
For illustrative purposes, Figs. 13 (a) and 14 (a) were taken at 1 kHz switching frequency to show in details the correlation of the switched output voltage across the load in CH1 and the load current in CH2 and the gate drive signals for both methods. A low cost, dsPIC30F3010 [31] DSC was used to perform real time calculations to construct a sinusoidal reference, based on which PWM signals were generated.



(a)



(b)



(c)

Fig. 14. CH1 shows switched voltage across load (V_{XY}) and CH2 shows load current i_L for Proposed method. Digital channels Ch0, Ch1, Ch2 and Ch3 show gate pulses to Q4, Q1, Q3 and Q2 respectively. (a) F_S = F_{SW} = 1 kHz (b) F_S = F_{SW} = 6 kHz (c) F_S = F_{SW} = 10 kHz.

The logic circuitry was implemented using low cost fast logic gates. For safe operation of the circuit, an interface between the DSC and power switching devices was employed using opto-isolators HCPL2631V [32]. High switching frequency commercialized Silicon Carbide (SiC) MOSFETs C2M0080120D [33] for high frequency leg and low frequency

IGBTs STGW12NB60HD for low frequency leg were used [34]. To drive the switching devices efficiently, IC drive IR2110 was used [35]. The load connected to the inverter was a 27Ω resistor in series with a 37mH inductor. The input voltage of the inverter was 185V supplied by a regulated linear DC power supply. The modulating index M for all the tests was kept at M = 0.9. The harmonic spectra were extracted up to the 50^{th} order harmonic using a PM1000+ Power Analyzer. The load current was measured using a LEM LA-55P current transducer with transformation ratio of 1:1000. The ratio was changed to 1:250 as four turns through the current transducer were used in order to increase the accuracy of the measurement. A 150Ω resistor was connected to the output of the current transducer. The voltage developed across this resistor represents the load current and is shown by CH2 in Figs. 13 and 14 where every volt division represents 1.67 amperes.

Fig. 15 shows harmonic spectra of the output currents for the proposed and 3-LDPWM methods up to the 50^{th} fundamental harmonic on the same bar chart for $F_S = F_{SW}$ at frequencies equal to 1kHz, 3kHz, 6kHz, 10kHz and 20 kHz. The sidebands were created as a result of regular sampling PWM at F_S = 1kHz which can be seen in Fig. 15(a). These sidebands are not shown in the spectra in higher sampling and switching frequencies as the power analyzer can only display up to the 50^{th} harmonic (i.e. up to 2.5kHz). The inferior harmonic performance of 3-LDPWM method stems from discontinuity in its PWM reference signal which will be discussed in section IX.

Table III shows that for the proposed and 3-LDPWM methods, the efficiency is reduced by almost 0.5% as switching frequencies increases from 10kHz to 20kHz across the load. The amount of increase in power loss (ΔP_S) is 2.6W which is an indication of the switching losses associated with 10kHz switching frequency increase

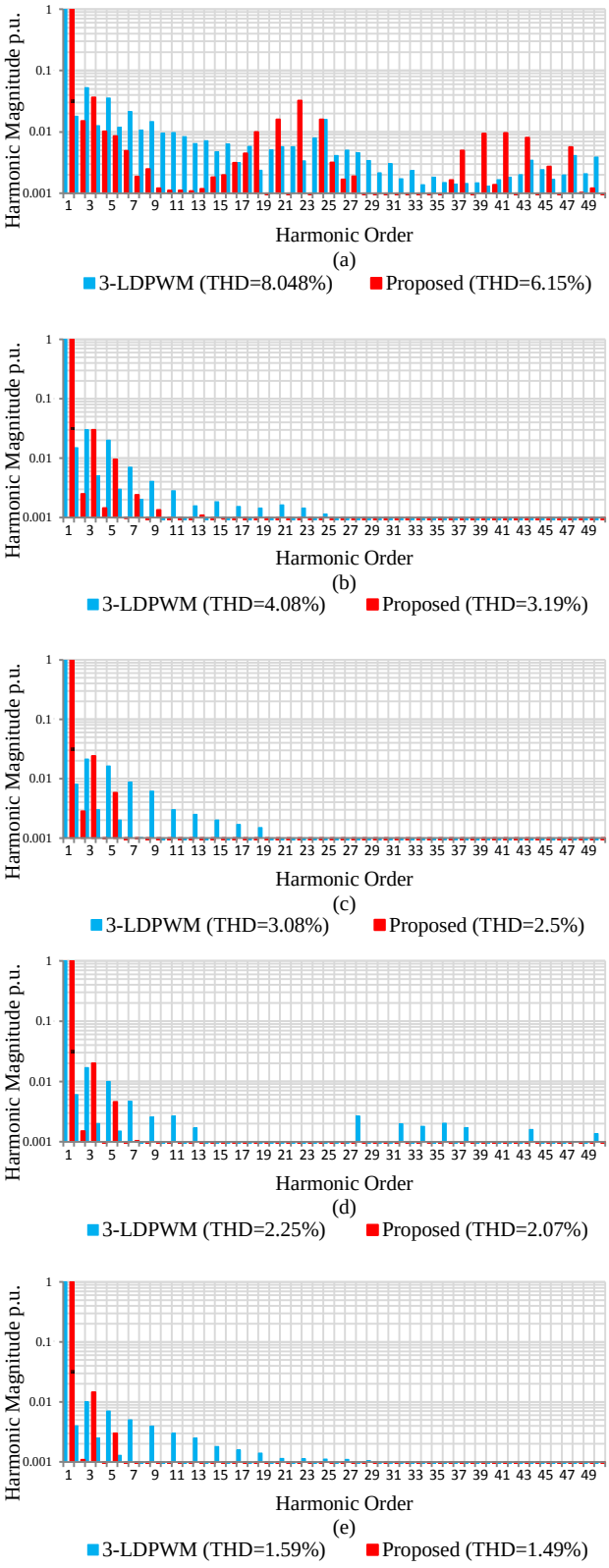


Fig. 15. Experimental load current harmonic spectra for 3-LDPWM method vs the proposed method at (a) $F_S = F_{SW}$ = 1kHz, (b) $F_S = F_{SW}$ = 3kHz, (c) $F_S = F_{SW}$ = 6kHz, (d) $F_S = F_{SW}$ = 10kHz, (e) $F_S = F_{SW}$ = 20 kHz

From comparing Figs. 7 and 15, it is evident that experiment results have richer harmonic contents compared to simulations. Non-ideal natures of both switching devices and input voltage source are the main causes of these discrepancies. In addition, the drive circuitry inherently introduces unequal turn-on and turn-off delays, which further deteriorates the harmonic distortions. It is therefore important to ensure that the combinational logic employed in the proposed method introduces minimal delays. To this end, fast logic gates were used to reduce logic propagation delay.

TABLE III. INVERTER PERFORMANCE CHARACTERISTICS

Parameter	Proposed		3-LDPWM	
F_{SW} (kHz)	10	20	10	20
THD (%)	2.07	1.49	2.25	1.59
Power Input (W)	493.5	496.1	494	496.65
Power Output (W)	460	460	460	460
Power loss (W)	33.5	36.1	34	36.65
ζ (%)	93.2	92.7	93.1	92.6
ΔP_S(W)*	2.6		2.65	
Total switching loss (W)	2.6	5.2	2.65	5.3
Total conduction loss** (W)	6.2		6.2	
Miscellaneous Loss (W)	24.7		25.15	

*Indicates switching loss increase for 10kHz load switching frequency increase

**Calculated from datasheet

The effect of increasing sampling frequency of the modulating reference signal on the THD of the load current for the proposed and the 3-LDPWM methods is shown in Fig. 16, where the THD is plotted against the sampling frequency. It is evident that the proposed method offers better harmonic distortion especially at low sampling frequencies; this issue will be further discussed in section IX.

VIII. LOSS CALCULATION

In order to analyze the sources of losses in the devices used in the H-bridge, mathematical expressions for conduction losses and datasheet information for switching losses were used. The results were compared with the experimental results shown in Table III.

The expression for the total losses in the switching devices is shown in (17):

$$P_{total} = P_S + P_C \tag{17}$$

Where, P_S is the switching loss and P_C is the conduction loss. The total bridge losses can be further broken into the losses incurred in the high frequency leg (HF) and losses in the low frequency leg (LF) as shown in (18).

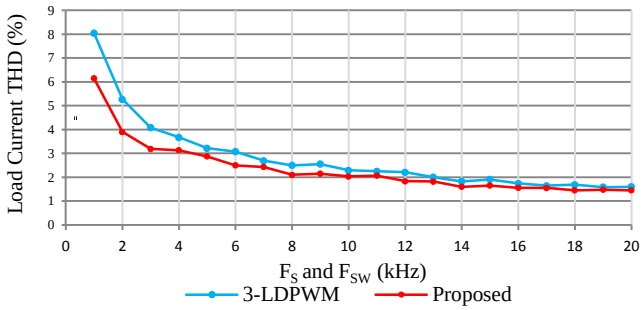


Fig. 16. Experimental load current THD at verious $F_{SW} = F_S$ for proposed method and 3-LDPWM method

$$P_{total} = [P_S + P_C]_{HF} + [P_S + P_C]_{LF} \quad (18)$$

Since the switching frequency of low frequency leg is negligible the formula can be approximated to (19).

$$P_{total} = [P_S + P_C]_{HF} + [P_C]_{LF} \quad (19)$$

$[P_S]_{HF}$ can be calculated by referring to the datasheet in [33], it can be found that for the SiC MOSFET employed in H-bridge in Fig. 2, the total switching energy loss E_{Tot}, is 120µJ at drain rms current I_D(rms) ≈ 5A. The switching losses can be calculated using (20).

$$P_S = E_{Tot} \times f \quad (20)$$

Hence for a switching frequency equal to 20kHz, the switching losses (P_S) for each SiC MOSFET will be 2.4W and for the two SiC MOSFETs this value will sum up to 4.8W. In Table III the switching losses for both proposed and 3-LDPWM were measured to be 2.6 W for 10kHz increase in load frequency for the two SiC MOSFETs therefore we can conclude that if the output load is subjected to a frequency of 20kHz, the total switching loss for two SiC MOSFETs will be 5.2W. This is evident by observing the values in the last row of Table III.

Total conduction loss $P_{C(tot)}$ can be calculated using the approximated algebraic function for regularly sampled PWM in [36]. The conduction losses incurred comprise the transistor losses and anti-parallel diode losses for each device [36]:

$$P_{C(tot)} = \left[P_{C(V_{TO})} + P_{C(r_T)}\right] + \left[P_{C(V_{DO})} + P_{C(r_D)}\right] \quad (21)$$

Where:

$P_{C(V_{TO})}$:Loss due to constant voltage drop (V_{TO})across transistor
$P_{C(r_T)}$: Loss due to conduction resistance (r_T) of transistor
$P_{C(V_{DO})}$:Loss due to constant voltage drop (V_{DO}) across diode
$P_{C(r_D)}$: Loss due to conduction resistance (r_D) of diode

$$P_{C(V_{TO})} = \frac{V_{TO} I_M}{2\pi}\left[1 + \frac{\pi}{4} M \cos\phi\right] \quad (22)$$

$$P_{C(r_T)} = \frac{r_T {I_M}^2}{2\pi}\left[\frac{\pi}{4} + \frac{2M}{3}\cos\phi\right] \quad (23)$$

$$P_{C(V_{DO})} = \frac{V_{DO} I_M}{2\pi}\left[1 - \frac{\pi}{4} M \cos\phi\right] \quad (24)$$

$$P_{C(r_D)} = \frac{r_D {I_M}^2}{2\pi}\left[\frac{\pi}{4} - \frac{2M}{3}\cos\phi\right] \quad (25)$$

Where:

M: The modulation index
cos ϕ: The power factor of output power
I_M: The transistor peak current
r_T: Transistor On resistance [37]
V_{TO}: Constant term of transistor voltage drop [37]

From datasheets [33],[34] , the following specifications for the switching devices used in this paper were extracted:

M: 0.9
cos ϕ: 0.87
I_M: 5.34A
$r_{T_{MOS}}$: 128mΩ for SiC MOSFET
$V_{DO_{MOS}}$: 1.5V for anti-parallel diode in SiC MOSFET
$r_{D_{MOS}}$: 140mΩ for anti-parallel diode in SiC MOSFET
$r_{T_{IGBT}}$: 60mΩ for IGBT
$V_{TO_{IGBT}}$: 0.8V constant term for IGBT
$r_{D_{IGBT}}$: 40mΩ for anti-parallel diode in IGBT
$V_{DO_{IGBT}}$: 0.6V for anti-parallel diode in IGBT

The $P_{C(V_{TO})}$ term in the expression for the losses in SiC MOSFET is negligible as MOSFETs are majority carrier devices and when operating in saturation mode present a linear output current characteristic [36].

Using the equations for the conduction losses, the following results are calculated for the particular devices used in the experiments.

For two IGBTs we have:

From (22):

$$P_{C\left(V_{TO_{IGBT}}\right)} = 2 \times \frac{0.8 \times 5.34}{2\pi}\left[1 + \frac{\pi}{4} \times 0.9 \times 0.87\right] = 2.19\ W$$

From (23):

$$P_{C\left(r_{T_{IGBT}}\right)} = 2 \times \frac{0.06 \times 5.34^2}{2\pi}\left[\frac{\pi}{4} + \frac{2 \times 0.9}{3} \times 0.87\right] = 0.7\ W$$

From (24):

$$P_{C\left(V_{DO_{IGBT}}\right)} = 2 \times \frac{0.6 \times 5.34}{2\pi}\left[1 - \frac{\pi}{4} \times 0.9 \times 0.87\right] = 0.39\ W$$

From (25):

$$P_{C\left(r_{D_{IGBT}}\right)} = 2 \times \frac{0.04 \times 5.34^2}{2\pi}\left[\frac{\pi}{4} - \frac{2 \times 0.9}{3} \times 0.87\right] = 0.09W$$

From (21) the total conduction losses of two IGBTs are:

$$P_{C(tot)_{IGBT}} = [2.19 + 0.7] + [0.39 + 0.09] = 3.37\ W$$

Similarly, for the two SiC MOSFETs from (22) to (25) we have: $P_{C(V_{TO\_MOS})} \approx 0\ W$, $P_{C\left(r_{T_{MOS}}\right)} = 1.52\ W$,$P_{C(V_{DO_{MOS}})} = 0.98\ W$and $P_{C(r_D)} = 0.33W$.

The total conduction losses for two SiC MOSFETs are:

$$P_{C(tot)_{SiC\ MOSFET}} = [0 + 1.52] + [0.98 + 0.33] = 2.83\ W$$

Total conduction losses for the bridge in Fig. 2 are:

$$P_{C(tot)} = P_{C(tot)_{IGBT}} + P_{C(tot)_{SiC\ MOSFET}}$$
$$P_{C(tot)} = 3.37 + 2.83 = 6.2W$$

The above calculated conduction losses are the same for both the 3-LDPWM and the proposed methods. Table III shows the conduction and switching losses occurred in devices in details. It also shows miscellaneous losses for both 3-LDPWM and the proposed methods. Miscellaneous losses include snubber losses for the devices in the bridge and losses incurred within

the auxiliary power supply for control and drive sections. It also includes the losses of the output filter.

The efficiencies for both 3-LDPWM and proposed methods are almost the same. However, Table V shows superiority of the proposed method to the 3-LDPWM method from a performance point of view.

IX. Discussion

A. Switching loss distribution

Concerns regarding the issue of uneven switching loss distribution have been the predominant barrier for developments of modulation methods involving one high frequency leg and one fundamental frequency leg operation in single phase inverters. These concerns should be discussed and addressed to justify developments in this field. Contrary to the common belief, with the development of new switching devices such as high frequency IGBTs and MOSFETs, uneven heat loss distribution has negligible effect on the safe operation of devices located in the high frequency leg in Fig. 2.

What follows addresses the question whether it is possible, for the same output power, to change the modulation type from the case where four transistors in Fig. 2 operate at half the load switching frequency (½F_{SW}) [12], to the proposed method where transistors in the high frequency leg operate at the load switching frequency (F_{SW}) without exceeding the specifications of the transistors. If the answer is positive then the main benefit that is gained by this trade would be the possibility of substituting the two high frequency and expensive transistors in one leg in H-bridge single phase inverter in Fig. 2 with two low frequency inexpensive transistors which will operate at low frequency and keep using the same high frequency transistors located in the high frequency leg, hence effectively reducing the overall cost of components. To address this, question the following argument is pursued.

By referring to the datasheet in [33], it can be found that for the SiC MOSFET employed in H-bridge in Fig. 2, the total switching energy loss E_{Tot}, is 120μJ at drain rms current I_D(rms) ≈ 5A. Hence for a switching frequency equal to 10kHz, the switching losses (P_S) for each transistor will be 1.2W.

By altering the modulation method from the type mentioned in the above paragraph where four transistors in H-bridge single phase inverter operate at ½F_{SW} (assuming F_{SW} = 20kHz) to the proposed method, the switching frequency of transistors in the high frequency leg increases from 10 kHz to 20 kHz which consequently increases P_S from 1.2W to 2.4W for each transistor. This amount of increase in power loss i.e. ΔP_S = 1.2W for each transistor in the high frequency leg due to the application of the proposed method, constitutes to less than 2% of the total power loss capability of the SiC MOSFET which is 65W at device case temperature T_C = 100°C with a Power De-rating Factor = 1.7 W/°C [33].

The above calculation is further supported by the experimental results in Table III from where it can be deduced that for the proposed method, an increase in switching loss (ΔP_S) of 2.6W occurred due to the load switching frequency change from 10 kHz to 20 kHz. This increase in switching frequency, caused an increase of switching losses which amounted to $\frac{\Delta P_S}{2}$ = 1.3W for each SiC MOSFET located in the high frequency leg which corresponds to 2% of 65W total device power loss handling capability for each SiC MOSFET as indicated in [33]. This test reveals that if the switching frequency in the proposed method is changed from 10kHz to 20kHz it is equivalent to the case where the load switching frequency is kept constant at F_{SW} = 20kHz but the modulation method is changed from the commonly used type in which four transistors in Fig. 2 operate at 10kHz for F_{SW} = 20kHz, into the proposed method in which two transistors in the high frequency leg operate at 20kHz for F_{SW} = 20kHz. This would result in an extra 1.3W power loss increase per transistor in high frequency leg in the proposed method compared to the aforementioned commonly used method for the same output power.

The above argument can be extended to the situation where the switching devices employed in the experiments in section VII, were to be used in their full rating capacities i.e. $I_{D(rms)}$ = 20A, then the total switching loss (E_{Tot}) would be equal to 420μJ [33]. Therefore, by employing the proposed modulation method, an extra power loss of 4.2W is exerted to each transistor located in the high frequency leg for an increase of 10kHz in switching frequency, which would be less than 6.4% of 65W of total power loss handling capability of each SiC MOSFET device used in the experiments in section VII.

The analytical values for power loss from SiC MOSFET datasheet and the experimental results in Table III suggest that even though the switching frequency of the SiC MOSFETs located in the high frequency leg is doubled by the application of the proposed method, the devices and the circuit arrangement can remain unchanged as the small percentage of power loss increase in the high frequency leg in Fig. 2 can be accommodated without any major engineering challenge. This argument is equally valid for any switching devices such as any high frequency IGBTs or MOSFETs if they were to be used in the high frequency leg in Fig. 2.

Hence, uneven power loss distribution is no longer a major concern as the switching loss increase in the high frequency leg, constitutes to a small portion of total power dissipation ability for the SiC MOSFET in question. Therefore, it can be deduced that by employing the proposed method not only do we not exert a significant extra power loss burden on the existing transistors in the high frequency leg but also we make it possible to use cost effective low frequency IGBT transistors in the low frequency leg which will considerably reduce the production cost of the single phase inverters. This is shown in Table IV.

B. Base band harmonic distortion

Harmonic distortion of an inverter is often assessed through inspection of output current harmonic spectrum as the output voltage spectrum is usually dependent on the output filter characteristics [29]. In the case of the proposed method, a set of low order harmonic distortions near the fundamental frequency can be observed in Figs. 7 and 15. This is not a direct consequence of the application of the proposed method but is a side effect of regular sampling of the reference signal. As suggested in [12], regular sampling inherently results in low order harmonic distortions. This is further proved by the simulation results in Fig. 7 where low order harmonics can be observed for both 3-LDPWM and proposed methods. By applying other ways of implementation for reference signal, such as naturally sampled technique [2], [10], the low order harmonic distortion near the fundamental frequency can be removed. Since regularly sampled technique is a straightforward method for the construction of the reference signal in microcontrollers and DSCs, the issue of low order distortions is often considered a fair compromise between ease of implementation and low-order harmonic distortion[12].

Crucially, as shown in Fig. 16 for the proposed method, increasing the sampling frequency beyond 3kHz has negligible effect on the THD_I figure. This is due to the narrow bandwidth of the reference signal in the proposed method which was mathematically studied in section IV. Fig. 16 also demonstrates the fact that with sampling frequency at 1kHz, the THD_I figure for the proposed method is lower than that of 3-LDPWM method but as sampling frequency increases to 20kHz, the THD_I figures for 3-LDPWM reduce and approximate to those of the proposed method, which further supports the above analytical argument in section IV regarding the origin of poor harmonic distortions of 3-LDPWM at low sampling frequencies compared to the proposed method.

C. Low production cost

Use of discrete fast logic gates for PWM subtraction is an inexpensive solution which offers a small propagation delay in the order of nano-seconds.

TABLE IV. INVERTER PROTOTYPE PRODUCTION COST ANALYSIS [31]-[35], [38] - [43]

Component				Classic		3-LDPWM		Proposed	
Description		Part No.	Unit Price (USD)	Qty.	Total (USD)	Qty.	Total (USD)	Qty.	Total (USD)
	Control								
1	DSC	dsPIC30F3010	4.50	1	4.50	1	4.50	1	4.50
2	Logic AND gate	NC7SZ08M5X	0.08	-	-	-	-	6	0.48
3	Logic OR gate	SN74LVC1G332DCKR	0.21	-	-	-	-	2	0.42
	Switching Devices								
4	High Frequency SiC MOSFET	C2M0080120D	17.00	4	68.00	2	34.00	2	34.00
5	Low Frequency IGBT	STGW12NB60HD	3.00	-	-	2	6.00	2	6.00
	Miscellaneous								
6	Auxiliary Power Supply	MTU1S1215MC	2.76	3	8.28	3	8.28	3	8.28
7	Gate Drive Components	IR2110	2.71	2	5.42	2	5.42	2	5.42
8	Gate Opto-isolator	HCPL2631V	2.10	2	4.20	2	4.20	2	4.20
9	Heat-sink	SK 61/100 SA	16.54	1	16.54	1	16.54	1	16.54
10	Input and Output Filtering	SMV40	5.88	2	11.76	2	11.76	2	11.76
11	Other Components	-	10.00	-	10.00	-	10.00	-	10.00
12	PCB	2-layer 30cm × 20cm	30.00	1	30.00	1	30.00	1	30.00
Total Cost (USD)				158.70		130.70		131.60	

TABLE V. INVERTER PROTOTYPE PRODUCTION COST ANALYSIS

Parameters involved in decision making		Classic	3-LDPWM	Proposed
1	Production Cost	Bad	Good	Good
2	Even-order Harmonic Cancelation	Moderate***	Bad	Good
3	Harmonic Distortion at Low F_S	Good	Bad	Good
4	Reference Bandwidth	Good	Bad	Good

*** Refer to section III for further information

Table IV shows a summary of major components' cost breakdown comparison of the classic inverter, 3-LDPWM and the proposed methods based on a prototype production cost for a 500W with 200V DC input and 110V AC output, single phase inverter. The classical method, where four transistors in Fig. 2 operate at high frequency shares most of its bill of material with the other two methods. In contrast both the proposed and the 3-LDPWM methods offer a cost saving of about 17.6% compared to the classical design thanks to application of low switching frequency transistors in one leg of the inverter. By comparing the total cost of the proposed method with the 3-LDPWM method, it is seen that the extra logic circuitry in the proposed method increases the production cost by less than 1 USD which constitutes to only 0.76% increase in the total production cost of the inverter [31]-[34]. In return the proposed method offers a significantly better harmonic distortion compared to 3-LDPWM method as was discussed in the previous sections and is summarized in Table V.

X. Conclusion

A cost effective modulating method for single phase H-bridge inverters was proposed. The proposed method subtracts two antiphase sinusoidal based regular sampled PWMs using a combinational logic circuit to create a new continuous PWM signal with even-order harmonics cancelation capability. The performance of the proposed method was evaluated and compared with 3-LDPWM method using commercialized SiC MOSFETs and IGBTs in a 500W single phase inverter on the bases of switching losses, harmonic distortions production cost and sampling rate. Similar to 3-LDPWM method, the proposed method offers low production cost benefit. In addition, the comparison showed that the proposed method also offers the ability of removing even-order harmonics and provides a considerably better THD figure compared to 3-LDPWM especially at low sampling frequencies due to the narrow bandwidth of its reference signal. The combinational control cancels the even-order harmonics and significantly improves the harmonic distortion of the output current in the proposed method whilst the additional logic circuitry only increases the production cost by less than 1 USD. Table IV and Table V, indicate that from the efficiency and cost reduction point of views, both proposed and 3-LDPWM methods present almost identical merits however, as shown in Table V it is clear that the proposed method can offer a significantly better harmonic distortion hence making the proposed method an attractive solution in industry.

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