Brunel University London

CURRENT-SOURCE-BASED LOW FREQUENCY INVERTER TOPOLOGY

Department of Electronic and Computer Engineering

College of Engineering, Design and Physical Sciences

Brunel University, London

By:

Mansour Salehi Moghadam

A thesis Submitted for the degree of Doctor of Philosophy

Supervised

By:

Dr. Mohamed Darwish

December 2015

I dedicate this thesis to

My family, My wife,

Humanity and my country

Contents

LIST OF FIGURES AND TABLES

Figures

Tables

ABSTRACT

A DC to AC inverter can be classified in different topologies; some of these topologies are three level and multilevel inverter. Both types have some advantages and disadvantages. Three level inverters can be applied for low power applications because it is cheaper and has less semiconductor losses at high switching frequencies with poor total harmonic distortion (THD). Multilevel inverters (MLI) can be applied for higher power applications with less THD. However, the MLI has more cost and conductive power losses in comparison with three level inverters.

In order to overcome the limitations of three and multilevel topologies, this thesis presents a new controlling topology of multilevel DC/AC inverters. The proposed multilevel inverter topology is based on a current source inverter, which consists of a buck/boost, boost and flyback converters, and an H-bridge inverter. The output voltage of the inverter is shaped through the control of just one main semiconductor switch. This new topology offers almost step-less output voltage without the need for multi DC source or several capacitor banks as in the case of other multilevel inverter topologies. The efficiency of the proposed topology is higher than other inverter topologies for medium power applications (2-10 kW). The proposed topology also generates smaller Total Harmonic Distortion (THD) compared to other inverter topologies. The two main key aspects of the proposed circuit is to keep the switching losses as low as possible and this is achieved through the control of a single switch at relatively low frequency and also to generate an improved AC Voltage waveform without the need for any filtering devices. The output frequency and voltage of the proposed circuit can be easily controlled according to the load requirements. The proposed inverter topology is ideal for the connection of renewable energy; this is due to its flexibility in varying its output voltage without the need of fixed turns-ratio transformers used in existing DC/AC

inverter topologies. The harmonic contents of the output of this proposed topology can be controlled without the need of any filter.

The simulation and practical implementation of the proposed circuits are presented. The practical and simulation results show excellent correlation.

Acknowledgement

First, I would like to thank to my PhD supervisor, Dr. Mohamed K. Darwish, for supporting me in during my study in past 4 years. Dr Darwish advised me to have right direction on the project. He is the helpful advisor and one of the kindest people I know. I would like to special my thanks to Dr Christos Marouchos, Dr Michael Theodoridis, Dr Alireza Harasi and Mr Tony Wood who support and help me with a PhD project by their advice.

Also, I am thankful to my friends for their support and friendship, Dr.Armin Kashefi, Dr.Mohamad Sadeghi, Dr.Hossien Madani, Dr.Mohamdreza Behjati, Dr.Roohalla Haghpanahan, Dr.Kamran Pedram, Dr.Reza Abbaszadeh, Dr.Morad Danshvar, Dr.Sohil Hassanzadeh, Mr.Ahamd Nasrolahi, Mr.Babak Atallohai and Mr.Sasha Kaveh.

Great thanks to My family, especially my father, my mother, my brother and my sisters for their emotional support in my difficult situation. Special thanks to my family in law for their support.

Great thanks to my lovely wife

Mansour Salehi Moghadam

LIST OF PUBLICATIONS

1) MAROUCHOS, C., XENOFONTOS, D., DARWISH, M., MOGHADAM, M. and ARMEFTI, C., 2014. The switched capacitor inverter as a MPPT in a photovoltaic application, Power Engineering Conference (UPEC), 2014 49th International Universities 2014, IEEE, pp. 1-4.
2) MOGHADAM, M., DARWISH, M. and MAROUCHOS, C., 2013. A simple drive induction motor based on buck/boost inverter topology, Power Engineering Conference (UPEC), 2013 48th International Universities' 2013, IEEE, pp. 1-4.
3) MOGHADAM, M.S. and DARWISH, M., 2012. A buck/boost based Multilevel inverter topology for UPEC2012 conference proceeding, 2012 47th International Universities Power Engineering Conference (UPEC) 2012.
4) MANTOCK, P.L., MOGHADAM, M. and DARWISH, M., 2012. A Charge Transfer Cable (CTC)'an ultra-low loss cable', 2012 47th International Universities Power Engineering Conference (UPEC) 2012.
5) *M.S.Moghadam, , M.K. Darwish,, C.Marouchos,* A Boost-Based Low Frequency Inverter Topology summited in IEEE Transactions on Power Electronics

List of Symbols & abbreviation

ABBICI	Active Buck-Boost Inverter with Coupled Inductors
AC	Alternating Current
ABS	Absolute Value
BBLFI	Buck/Boost-based Low Frequency Inverter
BJT	Bipolar Junction Transistor
BLFI	Boost-based Low Frequency Inverter
C	Capacitor
CBBCHI	Combination Buck/Boost Converter and H-bridge Inverter
CCMI	Capacitor Clamped Multilevel inverter
CCSMI	Combination of Current source with Multilevel inverter
CHBI	Cascading H-Bridge Inverter
CS	Control Signal
CSI	Current Source Inverter
CSSPWM	Current Source Sine Pulse Width Modulation
D	Duty cycle
DC	Direct Current
DCMI	Diode clamped Multilevel inverter
DSPWM	Double Sinusoidal Pulse Width Modulation
ζ	Efficiency
F_c	Carrier Frequency
F_s	Switching Frequency
FFT	Fast Fourier Transform
FLFI	Flyback-based Low Frequency Inverter
GTO	Gate Turn-off Thyristor
G_{off}	Conductance of switch when is off

$I_{switch\ when\ is\ off}$	Leakage current in switch when is off
IGBT	Insulated Gate Bipolar Transistor
I_{on}	Average current in a switch when is on
L	Inductor
m	Levels of Voltage
M_a	Amplitude ratio modulation
M_f	Frequency ratio modulation
mH	millihenry
mF	milliFarads
µ	Micro
M_v	Output Voltage modulation
ms	Millisecond
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NPD	Number of Power Devices
NSD	Number of Semiconductor Devices
Ω	Ohms
PSpice	Personal Simulation Program with Integrated Circuit Emphasis
PWM	Pulse Width Modulation
R_{on}	Resistance of the switch when is on
RMS	Root Mean Square
RSPWM	Rectifier Sinusoidal Pulse Width Modulation
S	Semiconductor Switch
SHD	Sum of n^{th} Harmonic Distortion
SPL	Switching Power Loss

SPWM	Sinusoidal Pulse Width Modulation
T	Time for the fundament frequency
t	Time
Td (on)	Turn on delay time
t_{on}	ON time
t_{off}	Off time
t_{ron}	Rising ON time
t_{roff}	Rising Off time
t_{fon}	Fall ON time
t_{foff}	Fall Off time
THD	Total Harmonic Distortion
TLBI	Transformer-Less Boost Inverter
UPS	Uninterruptible Power Supply
V_{AB}	Voltage across inverter
Vin	Input Voltage
V_{off}	The average voltage across the switch when is off
Vout	Output Voltage
V_{pk}	Voltage Peak
$V_{rms\ (fundamental)}$	Root Mean Square Fundamental voltage
$V_{rms\ (output)}$	Root Mean Square output Voltage
VSI	Voltage Source Inverter
VSSPWM	Voltage Source Sine Pulse Width Modulation
XOR	eXclusive Or gate

Chapter 1 Introduction

1.1Introduction

The benefits of DC to AC inverter are varying the output voltage and frequency of the system by controlling switching pattern of semiconductor switches in power electronic system. The most common semiconductor switches in power electronic are MOSFT, IGBT, GTO, Thyristors, etc. (Malinowski, Gopakumar et al. 2010, Hu, Zhang et al. 2015)

These days power electronic field is growing very fast for using different applications, such as renewable energies, motor drive, HVDC network and else… The most systems are supplied from the grid as AC with different frequency and voltage. The power electronic stuffs can be connected between DC systems & AC systems and vice versa. (Rodriguez, Lai et al. 2002, Cao, Loo et al.)

The DC to AC inverter is one of the main application systems of power electronics. There is a lot of topology of DC to AC inverter that have some advantages and some limitations. The most common topology of inverter is PWM and multilevel inverters. Each one of these two methods has some limitation in comparison to each other. (Zhang, Qu 2015, Ng, Tu et al. 2014a, Nguyen, Nguyen et al. 2015a). These two topologies have two main parts power circuit and control circuit (control system). Each of these two parts has some limitations and benefits (Draxe, Ranjana et al. 2014, Chunxia, Lei et al. 2014). Efficiency, cost and total harmonic distortions are the objectives of DC to AC inverter. The power circuit of these inverter topologies is looking to improve these objectives. The control system of these methods is focusing on points to the control system to have less stress and more balance on the power system circuit (Ravindranath, Mishra et al. 2013). These objects of inverters make limitation for each topology in past

30 years, so that means each topology can have one or two of these objects (Rodriguez, Lai et al. 2002, Muthukumar, Sankar et al. 2015, Bhagwat, Stefanović 1983).

The recent researches are about combination of different topologies together to improve the system. This improvement depends on control techniques and electrical material of semiconductor components (Atly, Aathira 2015a, Atly, Aathira 2015b, Zhang, Qu 2015, Ho, Chun et al. 2015, Ma, He et al. 2015).

1.2 Research Scope

The power electronic field is very wide in comparison to other part of electrical engineering because of being a combination of power and control system. This thesis focuses to present a new control topology of DC to AC inverter. This topology can be applied in different current source inverter with multistage output voltage. The multistage output voltage can reduce a total harmonic distortion and reduce switching losses at high frequency.

The controlling topology can optimize to eliminate specific harmonic order by controlling switching pattern and frequency. Also the switching frequency has a direct relationship to size of passive components in power electronics (Zheng, Wang et al. 2014, Prasadarao, Sudha Rani et al. 2014). So high switching frequency increases losses in switches; especially in industrial power application (Ranjana, Maroti et al. 2014, Ng, Tu et al. 2014b). The multilevel inverter can be applied in high power application, where the cost is not the main issue in the system (Narimani, Wu et al. 2014).

There are different types of multilevel inverters, which can invert DC voltage to AC output with a number of levels. These numbers of level can be chosen by power application required (Sruthi, Saritha 2014, Yadav, Bansal et al. 2014, Singh, Tiwari et al. 2012). The number of passive and semiconductor devices increase with the increasing number of levels (Chulan, item 2014).

1.3 Research Motivation

The research motivation for this project is to have less number of passive and semiconductor components to shape multilevel output voltage. The multilevel output voltage does not have poor THD in comparison with 3levels inverter (PWM) (Kanimozhi, Geetha 2014a, Law, Dahidah 2014). However, amplitude of lower order harmonics is high at multilevel inverter, which can be eliminated by optimising switching pattern. The multilevel inverter has more semiconductor devices in comparison into 3-levels inverter topology for having more levels, which increases conductor power losses and cost as well (Sato, Kawasaki et al. 2011a, Dixon, Pereda et al. 2010).

The number of components in 3-levels inverter topologies is less than the number of components in multilevel inverter topologies. Also the amplitude of lower order harmonic is very low at 3-levels inverter topologies then a smaller size filter can reduce THD (Kanimozhi, Geetha 2014b).

1.4 Research aim and objective

The aim of this project is to introduce a new DC to AC inverter topology. This new topology is controlling current source inverter to have a varying multistage output voltage. The new controller can be applied in different type of current source such as buck/boost, boost and flyback converters. The objective to use this controller in different types of current source inverter is to have different application such as residential and industrial. This control signal in applied on main switch of the current source in medium frequency 1 kHz to 5 kHz. The switching frequency of the circuit could be more or less than medium frequency, which depending on the application required. The voltage ratio of proposed circuit can be easily controlled by the varying switching pattern of control

signal. This variation voltage ratio can be useful for maximum power point tracking for renewable energy source. Also, these variation ratios can balance the system when the load changes in the system. However, varying switching frequency in inverters can control the output frequency. These frequency and voltage variation can be applied as motor drive to control speed and generate specific harmonics as active filter.

THD of this proposed topology can be reduced to 5% with no filter required. The efficiency of this topology is high in comparison to other topologies, which is the main reason to use this topology for high power application at single phase.

1.4.1 Research approach

This topology is combination current source and H-bridge inverter. Only the main switch of current source operates at high frequency and switches of H-bridge operate at low frequency. The control signal of this main switch is double sinusoidal pulse width modulation (DSPWM). This control signal operates at medium frequency (1 kHz to 5 kHz), which a switching loss is low at these frequencies. The switching frequency losses are not limitation for this topology. This control signal has direct relation to output voltage and frequency. Controlling switches frequency in H-bridge inverter can vary the output frequency.

1.4.2 Expected contributions

There are gaps in different topologies to have main objectives of DC to AC inverter topologies in one circuit, which are low losses, low THD and low cost. This limitation could be solved by the new control system, which is a DSPWM control signal. This control signal can apply to different type of the current source to have low or high power application in low frequency. The conductive power losses and switching losses of this proposed circuit could be lower in comparison to other topologies. Also, this control signal can reduce THD in the output of the proposed circuit by controlling the switching

pattern. The output can form closely to an AC sinusoidal waveform, which could reduce THD in the system. This new control system can be optimized to generate or eliminate specific harmonic order in the output of proposed circuit. The proposed circuit has multistage AC output with less number of semiconductor components, which reduces cost and losses in comparison to multi-level inverter topologies.

This control signal applied to different current source in different situation and different loads in simulation and practical to implement. The results of practical implement, simulation and theory experiment were almost the same. This topology achieves good results, which can help since to improve for the next step. The next step could be 3 phases of current source inverter at low frequencies.

1.4.3 Research overview and structure

This thesis includes of seven chapters as follows:

- **Chapter one** an introduction of the research objective and contribution.
- **Chapter two** is a literature review;
  - Background of three-level and multilevel inverter topologies.
  - Introducing and comparison between new topologies, which are a combination of current sources and multilevel inverter topologies.
  - There is a brief description of new topology advantages, limitations and critical points of these topologies.
- **Chapter three** is introducing proposed Buck/Boost-based low frequency inverter BBLFI with the new proposed control signal
  - Pulse width modulation (PWM) control signal.
  - This proposed circuit is controlled by Rectifier Sinusoidal Pulse Width Modulation (RSPWM) control signal in main switch of the current source.

- There is discussion about these two types of controller for BBLFI. This discussion is about the advantages and limitations of these two controllers for BBLFI.
- There are simulation examples for these two control topologies.

- **Chapter four** presents a double sinusoidal pulse width modulation (DSPWM) for different current source inverters.
  - Introduce circuit of DSPWM control signal generator.
    - Introduce Buck/Boost-based Low Frequency Inverter
    - Introduce Boost-Based Low Frequency Inverter
    - Introduce Flyback-based Low Frequency Inverter.
  - Design example for these proposed circuit.
  - Optimising switching pattern to reduce low order harmonics
- **Chapter Five;** There are examples for these different current source inverters, which are simulated in chapter five. This chapter is simulation of these three topologies in same condition and discuss about simulation results.
- **Chapter six** is about practical implemented of these three different current source inverter topologies. This chapter discusses about different case studies, which are for different loads and frequencies.
- **Chapter seven** is a conclusion and future work of this research.
- **Appendices A, B and C** present proof of equations, microcontroller/ MATLAB programmed code and practical implement the results of case studies.

Chapter 2 Literature review of DC to AC inverter topologies

2.1 Introduced three and multilevel DC to AC inverter

A DC to AC inverter is designed for converting DC power to AC power. The waveform of the AC could be a square waveform or pure sine wave. The square wave is constructed by adding all odd order harmonics for odd signal. The pure sine wave can have only fundamental frequency and other odd order harmonics are minimized to zero (Atly, Aathira 2015a, Tourkhani, Viarouge et al. 1999, Nho, Cong et al. 2007). The pure sine wave can be reached by adding the right value of the filter at the AC output waveform (Georgakas, Vovos et al. 2014, Agorreta, Borrega et al. 2011). The DC/AC inverter can be designed for different application in variable frequency and variable AC output voltage. An application of DC/AC inverter could be a driver of an electrical machine such as induction and synchronous machine (Hothongkham, Kinnares 2007, Nisha, Jain 2015). The most common application of DC/AC inverter is for connecting renewable sources to power grid network. Another application of DC/AC inverter is Uninterruptible Power Supplies (UPSs) for constant regulated voltage AC. Additionally, a DC / AC inverter is also used in passive / active filter and could also be in series or parallel configurations, voltage compensation, Flexible AC transmission systems (FACTSs) and Static variables (reactive power) compensations (Chang 2011, Sanchis, Ursæa et al. 2005).

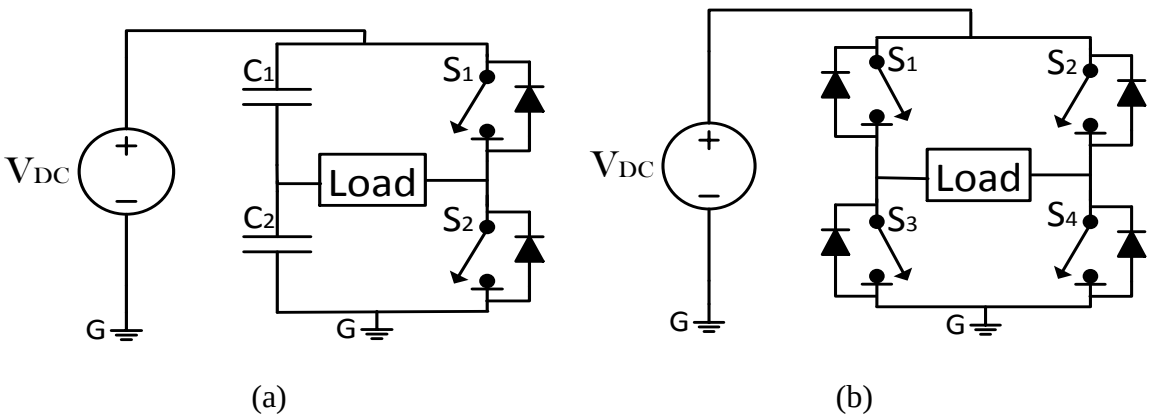
There are many DC to AC topologies in industrial applications; two categories of DC to AC topologies are focused on in this thesis. These two categories are classified according to the output waveform of the inverter, which are two/three-level and multilevel inverter topologies. The three-level inverter includes $+V_{dc}$, zero and $-V_{dc}$

levels; however, multilevel inverters can have different levels in the output waveform. These levels could be $+V_{dc}$, $+0.5V_{dc}$, $+0.25V_{dc}$, $+0.125V_{dc}$ and also zero level. These levels could be repeated at the negative side of the cycle (Azli, Bakar 2004, Gupta, Khambadkone 2005, Bai, Zhang et al. 2007). This chapter introduces topologies of three-level and multilevel inverters. The next part of this chapter covers voltage and current sources in three-level inverter. Then there are brief descriptions about different models of multilevel inverter in this part. There is a summary of the advantages and disadvantages of these topologies. The next part of this chapter (2.4) covers some new topologies which have more advantages than three and multilevel inverter circuits. The last part (2.5) all DC to AC inverter topologies is critically covered.

2.2Three level inverter

The three-level inverter includes three main parts: positive, zero and negative voltage or current. These levels can be repeated several times in one cycle. These repetitions (switching) depend on a carrier frequency of pulse width modulation. The waveform generated from a square wave output inverter circuit contains all odd number harmonics. However, there is an option to reduce or minimise some of the harmonics through the control of the on-off ratio of the switches (Binesh, Wu 2011, Takatsuka, Yamanaka et al. 2013, Xujiao, Zhengming et al. 2001). This three-level inverter can be designed in half or full H-bridge inverter configurations. Figs 1-(a) and 1-(b) show circuit diagrams of half and full H-bridge three-level inverter. This type of inverter includes all numbers of harmonics in the output waveform, so the total harmonic distortion (T.H.D) of this waveform is very high (Kang, Park et al. 2004, Luo, Ye 2010). The THD can be reduced or minimised by applying filters to cancel the amplitude of harmonic orders. There are some other methods to reduce the T.H.D by increasing carrier frequency in control modulation waveform (means increasing the switching frequency within one output

cycle) then the low order harmonics will be minimised. Also, lower order harmonics can be minimized or cancelled by having more than 2 or 3 output levels (Hagh, Taghizadeh et al. 2009). On the other hand, and in order to reduce the harmonics associated with 3-level inverters, the electronic devices (switches) need to operate at higher frequency and that in turns increases the switching losses. Although increasing the switching frequency does not reduce the THD, however, lower order harmonics are pushed down the frequency spectra range to become higher order harmonics (Ng, Tu et al. 2014a, Kang, Lee et al. 2003). These higher order harmonics are easier to filter in comparison to their previous position at low order frequencies. This is due to the fact that the filter size (L, C) needed for filtering actions is smaller in sized in comparison to those used to filter lower order harmonics. The amplitude modulation can be varied from 0 to 1. At zero amplitude modulation the output voltage is zero and at 1 amplitude modulation the output voltage will have a square waveform (Agorreta, Borrega et al. 2011, Arman, Marouchos et al. 2012).



(a) (b)

Fig. 2-1 (a): half bridge (b): full bridge

2.2.1 Pulse Width Modulation (PWM)

The three level inverter could be an AC square waveform in half or full H-bridge. This square wave is caused by the high amplitude modulation ratio (M_a) or low frequency modulation ratio (M_f), which means the carrier frequency and main frequency of modulation are the same. The main idea of pulse width modulation is to increase

frequency modulation ratio to minimise the magnitude of the low order harmonics. The low order harmonics generated by inverter circuits create imbalance and instability and decreases the power factor in the distribution / transmission levels. Such harmonics could be generated from inverter circuits connected to renewable energy sources (Lei, Wang et al. 2012, Zhang, Wang et al. 2005, Kanchan, Baiju et al. 2005, Dahidah, Konstantinou et al. 2010).

The number of switching in one cycle depends on the frequency modulation ratio. The frequency modulation is the ration between carrier frequency and main frequency. For example if the carrier frequency is 20 times the main frequency, then the number of switching (pulse) in the cycle is 20 times. The duty cycle of pulse Width Modulation (PWM) depends on the amplitude modulation ratio. The duty cycle can be from zero to 1 which depends on the ratio between the square-wave reference signal and the carrier signal of modulation. This ratio controls the amplitude of the inverter output and also has an effect on the distortion of the output waveform (Kanimozhi, Geetha 2014a, Nguyen, Nguyen et al. 2015b, Bao, Bao et al. 2011, Bao, Bao et al. 2009).

The H-bridge inverter (Fig. 2-1 (b) operates in a manner where the 4 switches control the current during the positive (S1, S4) and the negative (S2, S3) half cycles. The value of the inverter output voltage is controlled by controlling the amplitude modulation ratio (M_a). This ratio can either be controlled through hardware analogue circuits or software based digital microcontroller system. These control pulses are at low voltage and they can be used directly via drive circuits to control the main inverter semiconductor switches (MOSFET, IGABT, etc.) (Chakraborty, Hasan et al. 2014, Malinowski, Gopakumar et al. 2010)

Fig.2-2 shows an example of PWM pulses where the carrier frequency is 14 times the square-wave frequency. The control pulses are generated by comparing the triangular

and the square waveforms. The control output signals from the comparator takes the form of a train of pulses which can be fed to a driver circuit in order to control the switches. The control pulses could also be generated as digital pulses from a microcontroller and then fed to driver circuits to control the switches. The duty cycle, which is called amplitude modulation ratio (M_a) can be calculated from the formula (2-1) (Azli, Bakar 2004, Adda, Mishra et al. 2011, Nguyen, Nguyen et al. 2011). M_a is the ratio of the amplitudes of the square to the triangular waveforms. M_a for this example is 0.8. The frequency modulation ratio M_f is calculated from a formula (2-2) which is the frequency of the triangle waveform over the frequency of the square waveform. M_f for this example is 14, which is 7 pulses in the positive and 7 pulses in the negative sides. All generated pulses are positive and it is the action of the inverter switches which generate positive and negative output waveform from such control pulses. The control system of the DC/AC inverter could be open or close loops. Both control methods can utilise analogue as well as digital controllers (Ebadi, Joorabian et al. 2014, Dahidah, Konstantinou et al. 2010).

$$\mathbf{M_a = \frac{V_{in}}{V_{tri}}} \qquad \textbf{(2-1)}$$

$$\mathbf{M_f = \frac{f_{tri}}{f_{in}}} \qquad \textbf{(2-2)}$$

Where $f_{tri\text{-}m}$ is the frequency of the carrier signal. And V_{tri} is the voltage of the carrier signal.

Where f_{in} is the main frequency and V_{in} (amplitude of the square waveform) controls M_a which in turn controls the output voltage.

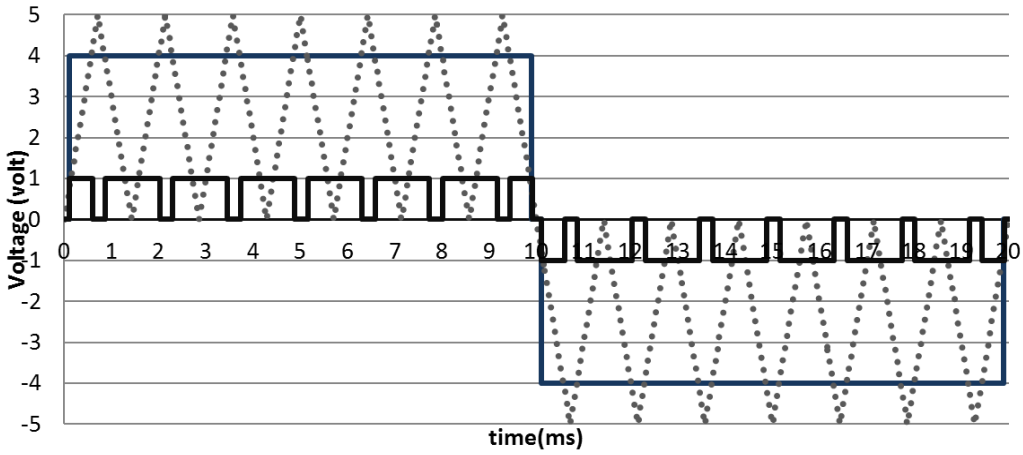


Fig. 2-2 Pulse Width Modulation of AC waveform

Sinusoidal pulse width modulation (SPWM) can reduce T.H.D in the output waveform by having a different pulse width on each of the half cycles (Sekhar, Das 2006, Bai, Zhang et al. 2007). The amplitude voltage of the sine wave is the main voltage (V_{in}) for modulation. The amplitude of triangle waveform is carrier voltage (V_{tri}) for modulation. The amplitude and frequency modulation ratio can be founded from formula (2-1) and (2-2) (Luo, Ye 2010, Gajanayake, Luo et al. 2010a). The Fig.2-3 shows an example of SPWM for 50Hz output frequency. The M_a for this example is 0.8 which means the r.m.s value of AC output voltage is 0.8 times the DC voltage source. M_f determines the sidebands of the output frequency For example M_f in Fig. 2-3 is 14 so the first harmonics in the output waveform are 13^{th} and 15^{th} followed by 27^{th} and 29^{th} and so on according to the modulation theory (Bai, Zhang et al. 2007, Gupta, Khambadkone 2005, Navabalachandru, Ashok et al. 2013).

The three levels DC to AC inverter can have three different topologies which are voltage, current and impedance source inverters. These types of inverter are explained in more detailed in section 2.2.2 and 2.2.3. The three level inverters discussed in this chapter are controlled by sinusoidal pulse width modulation (SPWM) technique which controls the semiconductor switches in all topologies (Binesh, Wu 2011, Shahalami,

Damirof 2012, Guedouani, Fiala et al. 2011, Chamarthi, Pragallapati et al. 2014, Saghaleini, Mirafzal 2012).

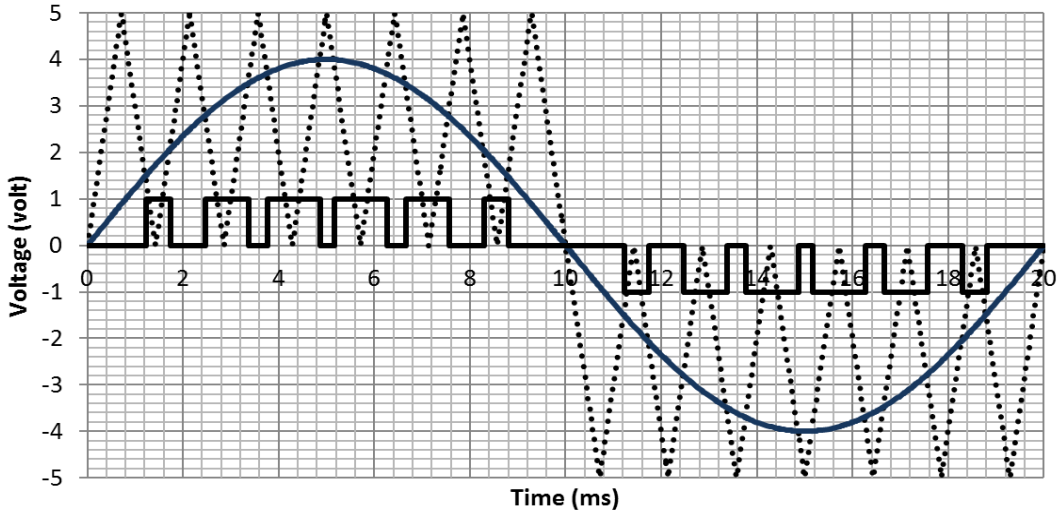


Fig. 2-3 Sinusoidal Pulse width modulation (SPWM).

2.2.2 SPWM voltage source

The SPWM can be applied to half and full H-bridge (Fig 2-1). The SPWM pulses control the switches in the voltage source inverter and the semiconductor switches control the flow of the main inverter current. In order to cancel low order harmonics (say from the 3rd to the 11th), the frequency of the carrier signal should be at least 15 times the reference frequency. The THD which is a measure of how the waveform is distorted is not controlled by M_f. M_f only pushes the frequency range to a higher value. THD can only be reduced either through the use of passive and active filters or through the use of multilevel inverters which is covered in section 2.3. However, the advantage of increasing M_f is mainly to reduce the size of the filter. The filter size is inversely proportion to the switching frequency. This is the main limitation of voltage source inverters as in order to reduce the size of the filter, one has to operate at higher switching frequency and as a result of that the switching losses will increase as it is directly proportional to the frequency of the semiconductor devices (Suh, Choi et al. 1996, Zhang, Wang et al. 2005, Kanchan, Baiju et al. 2005).

The SPWM voltage and current source inverters convert DC voltage into the AC voltage output of the inverter. The DC voltage source connects to inverter directly, then switches

which are controlled by Pulse from SPWM controller. The load can be resistance or inductance load as well, which could be single phase or 3 phase. The SPWM signal has two cycles, which depend on the main frequency of modulation. The number of pulses in the half cycle depends on carrier frequency. In the 3-phase inverter the main frequency for each phase is same as main frequency, but there are three different modulations with 120 degree phase shift. The M_a value can be described in three different categories, which are linear range, over-modulation and square wave if the M_f value of PWM is less than 21. The Ma value is less than one for linear range. In this range the lower harmonic order is minimised by increasing switching frequency. The Ma value is between 1 and 3.24 in over-modulation (Luo, Ye 2010, Shen, Joseph et al. 2007).

The fundamental amplitude output is not linear in over-modulation. The square wave is applied if the Ma value is more than 3.24. However, the output rms value of voltage source inverter is always less than the input value of DC source in the linear range (M_a<1). So the output rms value can be higher or lower than the input voltage if the H-bridge inverter connects to the current source. In that case this topology is called SPWM current source inverter, which is explained, in the next part of this chapter. The SPWM current source has three different categories buck, boost and buck, and boost inverter(Koushki, Khalilinia et al. 2008, Rahnamaee, Mazumder 2014, Hauke 2009).

2.2.3 SPWM current source inverter

The SPWM current source inverter (CSI) converts DC input current to AC output voltage of the inverter. The energy is transferred from the DC source into the inductor as a form of current. This energy is then transferred to the load. CSI can be used in three-phase and single-phase applications (Caceres, Barbi 1999, Chen, Liang et al. 2013, Qin, Sha et al. 2012).

The semiconductor switch is controlled by PWM signal, which is compared to the main frequency and carrier frequency (Fig.2-2). The current source could be boost, buck or

buck/boost DC to DC converter. The CSI is using PWM or SPWM controlling signal in semiconductor switches to invert DC voltage to AC output voltage. There are 3 different types of current source inverters, boost, buck and buck/boost inverters covered in this chapter (Wang 2003, Chakraborty, Annie et al. 2014).

In the buck type CSI the voltage is stepped down from high value (DC source) to a lower value (capacitor voltage). This is done through the control of the switch S_1 and the use of diode D_1. Then the DC voltage is inverted to AC voltage at H-bridge by controlling S_2-S_5 at high frequency SPWM. For clarification Fig.2-3 demonstrates the operation at lower frequency. Fig.2-4 shows a buck current-source inverter; this circuit includes two parts DC to DC converter and H-bridge inverter. The frequency of all switches in this type of inverter is high (higher than 50 Hz) in order to reduce size of inductor, capacitor and passive filter in the circuit. The passive filter can reduce THD to a desired value (usually less than 2%) (Agorreta, Borrega et al. 2011, Arman, Marouchos et al. 2012, Georgakas, Vovos et al. 2014). So this circuit needs to have the filter on the load side to have a pure sine wave.

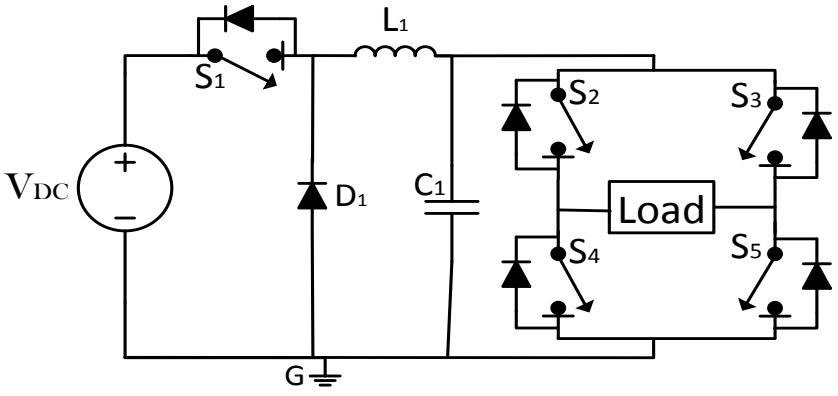


Fig. 2-4 Current source (Buck converter) DC to AC inverter

The second type of CSI is a boost DC to AC inverter; S_1 is controlled by PWM signal in high frequency; usually in the range of 1-5 kHz the lower and upper limitation are the

magnetic size and the switching losses (Fig.2-2). The voltage across the capacitor is higher than the input DC voltage. The inductor is charged and discharged through the PWM operation of S_1 D_1. The energy stored in the inductor in terms of current is then transferred to the capacitor in terms of voltage. The S_2- S_5 switches on the H-bridge operate in the same manner as the H-bridge in the buck-based current-source inverter which was shown in Fig. 2-4. Fig.2-5 shows a boost-based current-source inverter which includes boost DC –DC converter and H-bridge inverter (Zhang, Liu et al. 2014, Wu, Ji et al. 2015a, Atly, Aathira 2015b, Luo, Ye 2010).

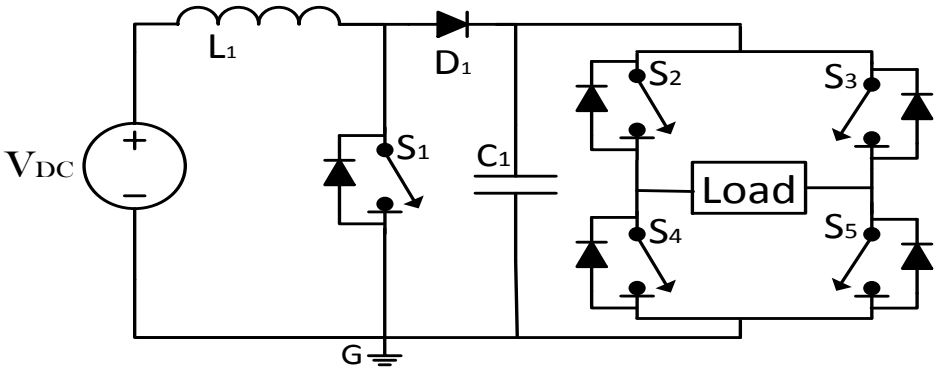


Fig. 2-5 Current source (Boost converter) DC to AC inverter

The third type of current source is a buck and boost inverter. This type of CSI can step up or down the inverter voltage. The output voltage can either be higher or lower than the DC voltage source. This is achieved through the control of the duty cycle PWM (M_a) of switch S_1 (Fig.2-6). This type of CSI is working the same as other type of CSIs. The polarity of the capacitor and H-bridge voltage are opposite to that across the DC source. Fig.2-6 shows the circuit of buck/boost-based current-source inverter (Chen, Smedley 2008, RW.ERROR - Unable to find reference:68, Tampubolon, Purnama et al. 2015, Jang, Agelidis 2011).

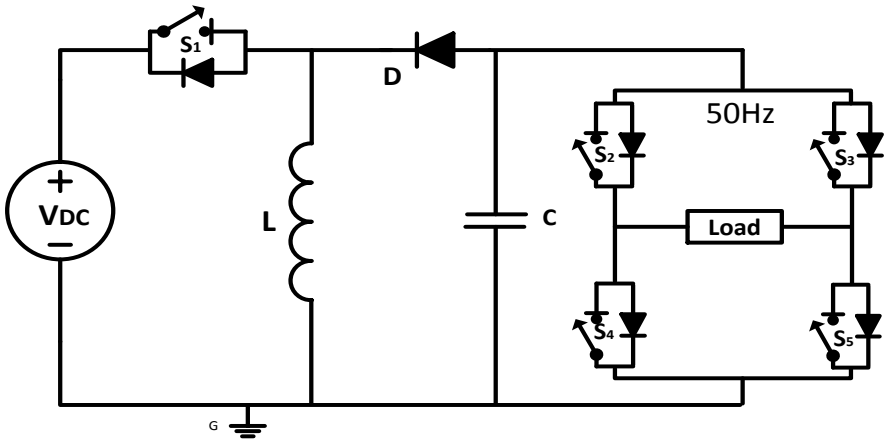


Fig. 2-6 Current source (Buck/Boost converter) DC to AC inverter

The main advantage of CSI is not using a transformer to increase or decrease voltage in the inverter. The size of inductor and capacitor could be very small in low power applications because of the use of high frequency of the main switch in the DC to DC converter. The current ripple in the current source converter depends on the value of inductance, duty cycle and frequency of the PWM controller of the main switch S_1. Also the voltage ripple of the load depends on switching frequency, duty cycle and the value of the capacitance. The size of the capacitor and inductor is inversely proportion to the switching frequency of S_1. In these types of current source inverters the high semiconductor switching losses are the main limitation/disadvantage (Sanchis, Gubía et al. 2005, Chowdhury, Chakraborty et al. 2014). The high switching losses are as a result of 5 switches operating at high frequency. On the other hand the main advantage is the reduction of the inductor and capacitor sizes. The CSI can be applied for small size of load 1000W for single phase and 3kW for 3 phases current source inverters (Xujiao, Zhengming et al. 2001, Lei, Peng 2014, Cancellier, Colli et al.).

Section 2.2.4 introduces the SPWM impedance source inverter, which is another interesting type of inverter to cover in the evolution of DC/AC inverter configurations.

2.2.4 SPWM Impedance-source inverters

The SPWM impedance-source inverter is a combination of voltage and current source SPWM inverters (Zhu, Yu et al. 2010, Bao, Bao et al. 2011). Fig 2-7 shows a 3-phase X shape impedance source inverter (ZSI), which is a buck/boost DC to AC inverter. This inverter includes seven semiconductor devices, which are six switches and one diode. Also, this circuit has two inductors and capacitors. However, the ZSI is a voltage source inverter if the value of L is zero. Also the ZSI is a current source inverter if the value of C is zero. So this topology has the same advantages of voltage and current source inverter. Moreover, this circuit does not have the limitations of voltage and current source inverter such as dead time for voltage source and overlap time for current source inverters because of the two inductors and two capacitors. Additionally the AC output amplitude of this topology could be more variable than current and voltage source inverter. Finally the ZSI is more reliable in comparison with other configurations. It has fewer problems in shoot-through of EMI noise, because of its ability to have anti-noise function (Shen, Joseph et al. 2007, Peng, Shen et al. 2005, Zhu, Yu et al. 2010, Lei, Peng et al. 2013).

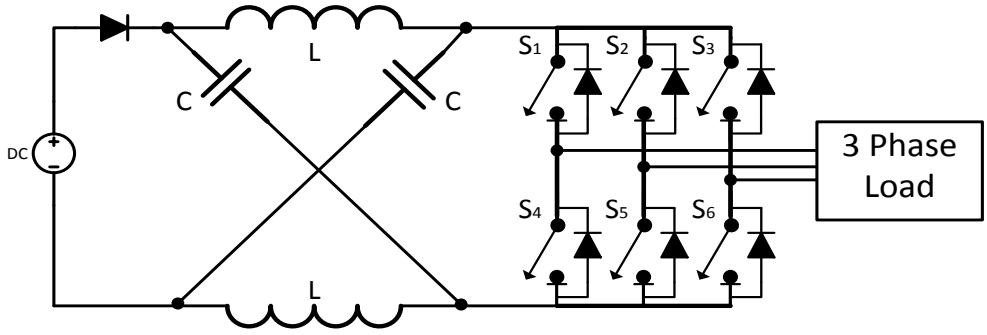


Fig. 2-7 SPWM impedance source inverter circuit

The voltage, current and impedance source (three level inverter) has two main problems when used in high power applications, which are, low efficiency and high total harmonic distortion. However, there are other topologies, which do not have the three level

inverter limitations. One of these topologies is called multilevel inverter, which is explained in more detail in section 2.3.

2.3Multilevel Inverters

The Multilevel Inverters topology uses low frequency switching to invert DC to AC. The DC voltage source divided into different levels by using and controlling semiconductor switches. The DC voltage levels can be used as different numbers of DC sources and DC capacitors. The voltage levels at the output can be higher than 3 (only odd number in order to eliminate any even harmonics). The higher number of levels needs to have more semiconductor components such as switches and diodes and also more DC voltage sources or DC capacitors (Arman, Darwish 2009, Nedumgatt, Vijayakumar et al. 2012, Zamiri, Hamkari et al. 2014, Sruthi, Saritha 2014).

In this section, the focus is on three main types of multilevel inverters: Diode clamp, Capacitor clamp and cascading H-bridge.

2.3.1Diode-Clamped Multilevel inverters

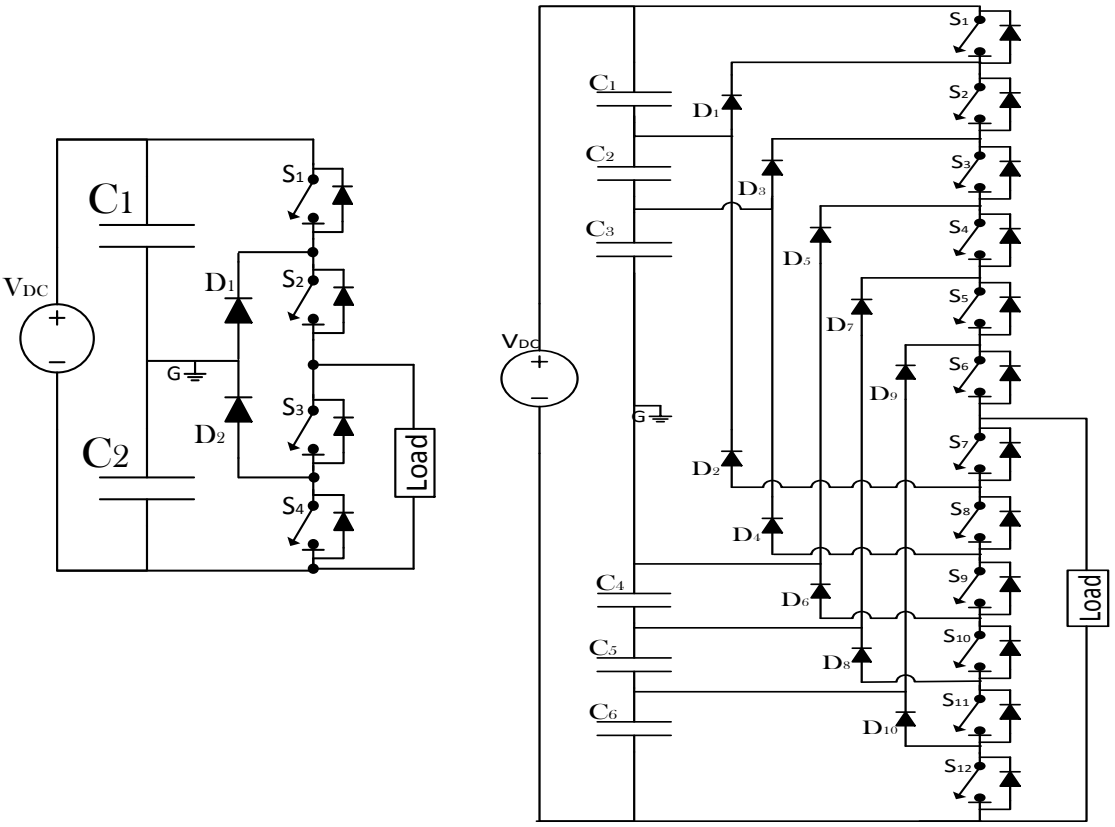
The output voltage in the Diode-clamped Multilevel Inverters (DCMI) is constructed through switching in or out of different DC capacitors (Yuan, Barbi 2000). The positive and negative output voltage waveform is formed through the number of capacitors/switches connected in series. Each capacitor works as a DC source in this topology . The capacitor voltages are clamped by two extra diodes. A m-level inverter requires a voltage level of $V_{dc}/(m-1)$ for positive and negative polarity(Yuan, Barbi 2000). Then the voltage across each DC capacitor is $V_{dc}/(m-1)$.

In summary the number of devices required for DCMI depends on the m-levels of inverter which are:

- Number of power electronic semiconductor switches =2(m-1)
- Number of DC-link capacitor = (m-1)

- Number of semiconductor diodes= 2 (m-2)

Fig.2-8 (a) and (b) shows an example of CDMI circuit for 3 and 7 level inverter.



(a) (b)

Fig. 2-8 (a) three levels DCMI circuit AND (b) Seven levels DCMI circuit

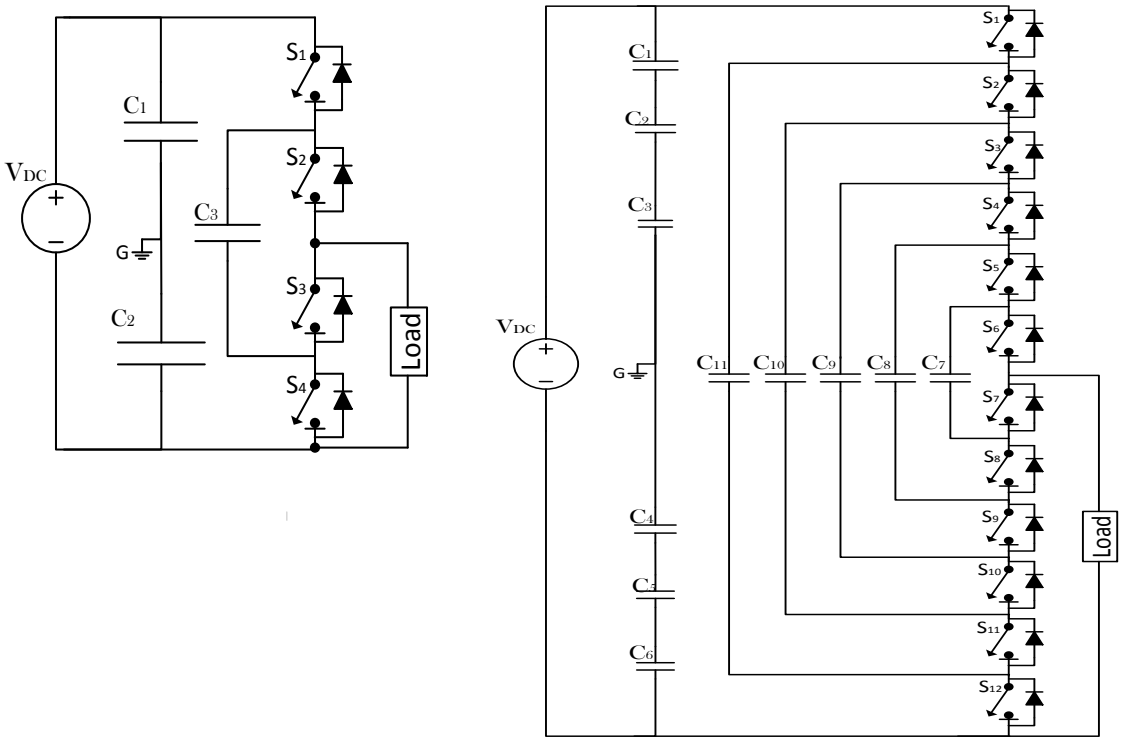
2.3.2 Capacitor –Clamped Multilevel inverters (flying Capacitor Inverters)

A voltage level is clamped by capacitors in the circuit, so each capacitor has a DC-link voltage for different levels. C_1 and C_2 of the circuit are for positive and negative polarity of V_{dc} in Fig 2-9 (a). A m-level inverter requests a voltage level of $V_{dc}/(m-1)$ for positive and negative polarity of capacitor (Kanimozhi, Geetha 2014b, Kalashani, Farsadi 2014, Rahnamaee, Mazumder 2014, Ranjan, Gupta et al. 2012, Huang, Corzine 2006). In summarizing the number of devices required for a Capacitor-Clamped Multilevel Inverter (CCMI) depends on them-levels of the inverter, which are:

- Number of power electronic semiconductor switches =2(m-1)

- A number of DC-link capacitor = 2 (m-1) -1

Figs.2-9 (a) and (b) show an example of a CCMI circuit for three and seven level inverter.

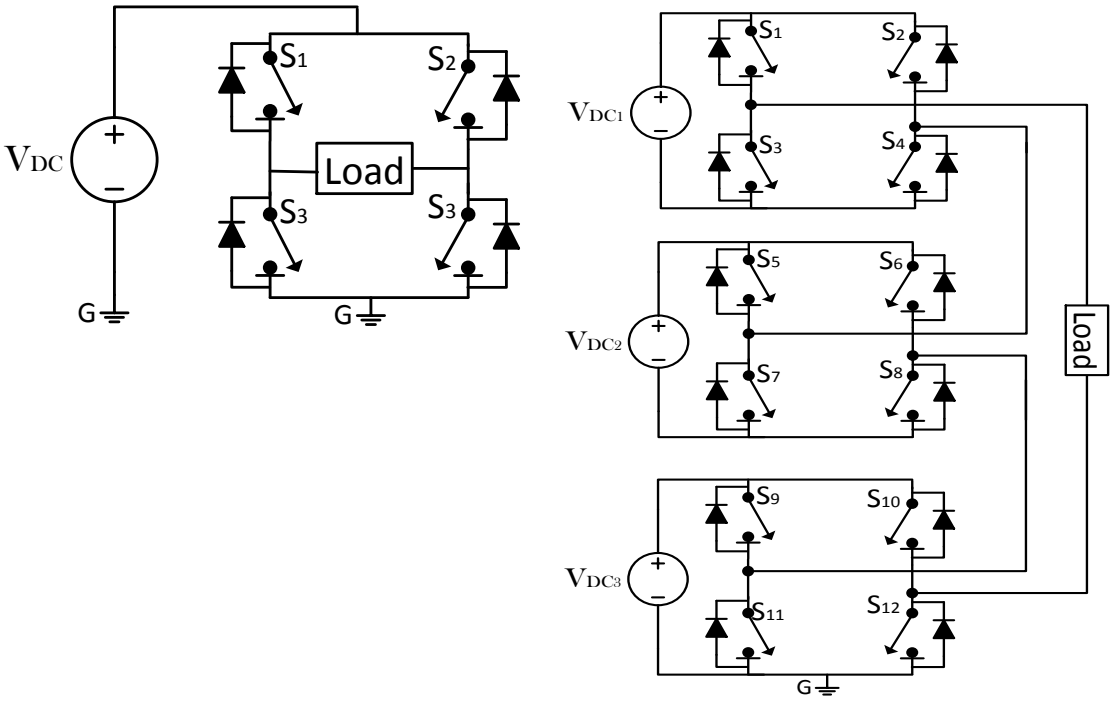


(a) (b)

Fig. 2-9 (a) three level CCMI circuit AND (b) Seven level CCMI circuit

2.3.3 Multilevel inverters using Cascaded H-bridge

The Cascaded H-Bridge (CHBs) DC to AC inverter is a combination of H-bridge inverters, each inverter has its own DC source (Corzine 2003). The Number of DC sources and H-bridges determine the number of levels which requests for application. Each DC source and H-bridge makes 2 levels of output and zero level can be applied in load by switching off on H-bridge (Zamiri, Hamkari et al. 2014, Zheng, Wang et al. 2014, Tuteja, Mahor et al. 2013, Malinowski, Gopakumar et al. 2010, Madouh, Ahmed et al. 2012). The Fig2-10 (a) and (b) Shows 3 levels and 7 level inverters for CHBs.



(a) (b)

Fig. 2-10 (a) three level CHBs inverter circuit (b) Seven level CHBs inverter circuit

There is a way to increase the number of levels by having different switching patterns and different values of voltage in the DC - link. So The V_{dc} can add to or subtract from each other by putting V_{dc} in series connection. Fig.2-10 (b) can have 15 or 27 levels if the voltage DC-link sources are different value. Table.2-1 shows an example of CHBs inverter with 7, 15 and 27 levels output with 12 switches and 3 different values of DC-link sources (Malinowski, Gopakumar et al. 2010, Rodriguez, Lai et al. 2002, Sujitha, Ramani 2012).

Table 2.1 shows CHBs inverter with different levels

CHBs levels for 12 switches	**V_{dc1} (Volt)**	**V_{dc2} (Volt)**	**V_{dc3} (Volt)**
7 levels	3	3	3
15levels	3	6	12
27 levels	3	9	27

This part is brief short explanation about three main different multilevel inverter topologies. The multilevel inverter has some advantages in comparison with the three

level inverters. The next part will explain and compare the advantages and limitations of two main DC to AC inverter topologies.

2.4Summary of three-level and multilevel DC to AC inverters

There are lists of the advantages and limitations of three-level and multilevel inverters.

The main advantages of three level inverters (PWM and SPWM inverter) for voltage and current source inverter topologies in comparison to multilevel inverters are (Kanimozhi, Geetha 2014b, Bai, Zhang et al. 2007, Gúrpide, Sádaba et al. 2001, Narimani, Wu et al. 2014, Muthukumar, Sankar et al. 2015):

- Less number of switches (less cost).
- Low amplitude of low order harmonics.
- Only a small size of output filter required.
- The small size of inductors and capacitors used in current source inverter.

Because of these advantages three-level inverters are still used in some low power industrial applications such as small induction AC Motor drivers and small size inverter for renewable energies (photovoltaic) (Kouro, Bernal et al. 2006, Zhang, Wang et al. 2014, Nisha, Jain 2015, Murugesan, Sivaranjani et al. 2011, Liu, Luo 2008, Chowdhury, Chakraborty et al. 2014).

The main limitations of three-level inverters (PWM and SPWM inverter) for voltage and current source topologies in comparison to multilevel inverters (Kjaer, Pedersen et al. 2005) are:

- Higher semiconductor switching power loss at high frequencies
- Higher conduction losses.
- Larger dv/dt, and di/dt which cause very big electromagnetic interference (EMI).
- Poor total harmonic distortion (THD)
- The RMS value of output voltage is always lower than input voltage.

- Controlling system is quite complicated for three level inverters.

However, the multilevel inverter can be applied for industrial high power applications and their advantages can be summarised as low power semiconductor switching losses, because of low switching frequency(Sekhar, Das 2006, Kabalci, Colak et al. 2011, Navabalachandru, Ashok et al. 2013).

- Low conduction power losses in each switch, because the current and voltage is distributed between numbers of switches.
- Very low electromagnetic interference (EMI) because of the output amplitude voltage is distributed between m-levels of multilevel inverter. So this causes a small dv/dt at each level.
- The pulse widths of all pulses can directly control the value of the AC output voltage.
- Lower THD, this is due to the low switching frequency and also due to the multilevel configuration.
- Selective harmonic elimination can also be implemented in MLIs.
- The controller is relatively simple. This is due to the relatively low frequency and it could be implemented easier in closed loop control system.

These advantages are the reasons to use multilevel inverter topologies for high power application and for specific applications such as the connection of high power, renewable energies to the power grid (Dash, Kazerani 2011, Muthukumar, Sankar et al. 2015, Prasadarao, Sudha Rani et al. 2014, Jang, Ciobotaru et al. 2013, Malad, Rao 2012).

The mechanism of the multi-level inverter is simply to add different voltage levels in the series at predefined timings. These voltage levels can be from different voltage source or capacitor by adding several power semiconductor devices. These semiconductor devices

are switches and diodes. Normally multilevel inverter adds voltage sources or capacitor voltages step-by-step from minimum negative through zero to maximum positive. The switching frequency in the MLI is at least twice the output frequency (Ebadi, Joorabian et al. 2014, Liu, Luo 2008, Lopatkin 2011, Yusof, Othman et al. 2014, Hasan, Mekhilef et al. 2014, Banaei, Dehghanzadeh et al. 2013). However, MLI also has its own limitations which can be summarised as:

- High number of semiconductor devices such as diodes and switches (this will cause more cost)
- A high number of DC voltage links such as DC voltage sources or DC capacitors (this you also will increase the cost).
- High amplitude of lower order harmonic distortion.
- Large sizes of passive filter to cancel/control low order voltage harmonics
- Using boost DC to DC converter or transformer to step up the voltage at the output. This is due to the fact that the required output voltage, usually has a higher amplitude in comparison to the DC input voltage.
- There is a higher voltage drop due to the larger number of semiconductor devices in comparison to 3-level inverters. However, this should be seen in relation to the lower switching losses.
- Could be less reliable than three level inverter because there are more devices in multilevel inverter topologies

On the other hand, multilevel inverters can be used for specific applications in which the cost and size of the inverter are less important. There are different topologies which can have some advantages of multilevel and three levels inverter (Kalashani, Farsadi 2014, Atmopawiro, Rachmildha et al. 2012, Bhatnagar, Nema 2013, Mosazadeh, Fathi et al. 2012). There is more explanation in section 2.5, which introduces different models and

combinations of multilevel and three level DC to AC inverter. There are also two examples of how selected harmonic elimination is applied in MLI and in multistage PWM inverters.

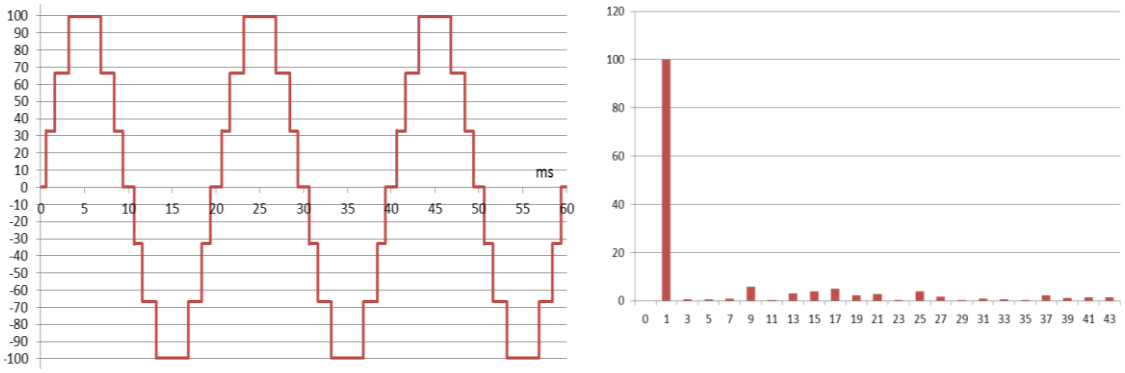
2.5 Improved multilevel DC to AC inverter topologies through the optimisation and multistage control techniques.

Some researchers at universities and RD within industries are trying to find a solution to the challenges within the three levels and multilevel inverter topologies. They try to combine the advantages of both techniques into single topology. For example, a multistage PWM inverter is a combination of multilevel and PWM inverter topologies aiming to achieve less power loss in the switches and reduce total harmonic distortions (Axelrod, Berkovich et al. 2004). In this section the focus is on introducing state of the art topologies which has the advantages of both SPWM and MLI topologies(Tolbert, Habetler 1999, Prashanth, Kumar et al. 2011, Li, Czarkowski et al. 2000, Colak, Kabalci et al. 2011). There are also some critical points of these modern topologies (combination of multilevel and three-levels inverter topologies) in this section.

The multistage PWM inverter topologies could be a combination of two circuits together, or could be a multilevel inverter circuit with PWM or SPWM switching pattern to control switches in the multilevel inverter circuits. However, these two combinations of inverter topologies have some advantages and disadvantages, which are explained further in the next section.

First, the PWM and SPWM switching pattern applies to switches at multilevel inverters to reduce total harmonic distortion and choose to eliminate specific low order harmonic distortion such as minimising 3^{rd} ,5^{th} ,7^{th} and 9^{th} harmonic orders. There are two main methods to minimise lower order harmonics by optimising the switching pattern or more switching at each level (Salehi, Farokhnia et al. 2011, Kumar, Das et al. 2008). Fig.2-11

(a) shows the time domain of 7 level inverter, which the voltage of each level is 33.33 volts and amplitude of output voltage is 100 volts. The pulse widths of switches are chosen by optimising switching pattern to minimise 3rd, 5th and 7th harmonic orders in this 7 level inverter (Lei, Peng et al. 2013, Zhou, Low et al. 2006, Guan, Song et al. 2005). Fig.2-11 (b) shows the fast Fourier transforms (FFT) of 7 level inverter when the amplitude of lower order harmonics are minimised by choosing the right values of control pulses. The control pulses are selected through Newton Raphson method (Hagh, Taghizadeh et al. 2009, Prashanth, Kumar et al. 2011, Salehi, Farokhnia et al. 2011).



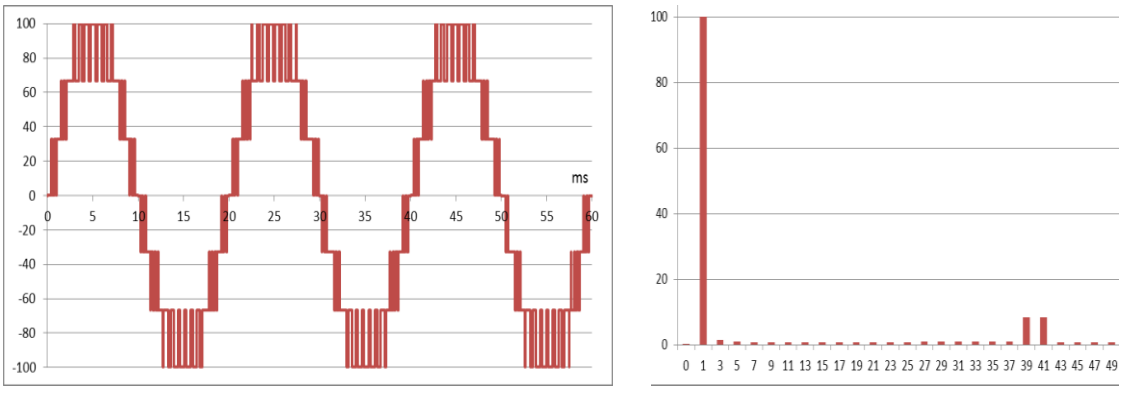
(a) (b)

Fig. 2-11 voltage waveform are 3rd 5th and 7th are eliminated and their frequency spectra

Fig.2-11 (b) shows the voltage amplitudes of 9th, 13th, 15th and 17th harmonics. Their values are between 7% to 10% of the fundamental components. The reason these values are high because they are outside the optimisation process, unlike the 3rd, 5th and 7th harmonics also the THD increased in this case. So a low pass filter is required to minimise 9th, 13th, 15th and 17th harmonic distortion. The low pass filter increases power loss in the system and reduces inverter efficiency (Chen, Liang et al. 2013, Zhou, Huang 2012). This method of switching pattern has a limitation which is by minimising amplitude of the lower harmonic order, the other odd order harmonics increase and also the total harmonic distortion increases. So there is another way to solve this problem,

which is by using pulse width modulation to control each level in the inverter(Barkati, Baghli et al. 2008, Taghizadeh, Hagh 2010, Ozpineci, Tolbert et al. 2004).

Fig.2-12 (a) shows 7 multistage PWM DC to AC inverter. So the total harmonic distortions decrease and eliminates lower order harmonic in the output. The PWM pulses are applied at each level of multilevel inverter (Ray, Chatterjee et al. 2009, Li, Czarkowski et al. 2000, McGrath, Holmes et al. 2003, Ozpineci, Tolbert et al. 2004, Hagh, Taghizadeh et al. 2009). So it means there are several 'on' and 'off' in each level of the multilevel inverter. The number of 'on' and 'off' at each level depends on the carrier frequency of the modulated waveform. The carrier frequency of PWM in this example is 2 kHz in order to minimise the harmonics at low order. Fig2-12 (b) shows the FFT of 7 levels multistage PWM inverter. The amplitude value of 3^{rd} -37^{th} voltage harmonics are less than 2 volts in this case, but the THD is about 17%. The reason to have poor THD is due to the high switching frequency of the inverter and the sidebands associated with this switching frequency. The passive filter can minimise the amplitude the harmonics associated with these switching frequencies. A simulation results show that the THD is less than 2%.



(a) (b)

Fig. 2-12 a)Output voltage b) FFT of output voltage of seven levels multistage inverter

The MLI and MSI (Multistage Inverter) share the same number of devices (for the same number of levels), however the control techniques are different. These methods apply different pulses to control the switching pattern in order to have different performance in

these two cases. These two methods are very useful for resistive loads and no variable input voltages. The variable inductive loads and variable input voltages (renewable energy sources) needs to have very complicated control systems (Muthukumar, Sankar et al. 2015, Prasadarao, Sudha Rani et al. 2014, Agorreta, Borrega et al. 2011). Also, there is more switching loss at multistage PWM inverter. So there is a method which can have the best solution for these two methods, limitations: "The combination of multilevel and current source inverter together". This method can have variable input voltage and variable loads(Bao, Bao et al. 2011, Adda, Mishra et al. 2011, Nguyen, Nguyen et al. 2011, Peng 2003). Section 2.6 has more explanation about this combination.

2.6 Combination of multilevel and current source inverter

Research at present focuses on the idea of bucking / boosting the DC level before the use of the MLI (Wu, Ji et al. 2015b, Li, Liu et al. 2009, Chakraborty, Annie et al. 2014). The buck/boost process can be in the form of a current source inverter (CSI). There is a lot of topologies and methods to combine CSI with multilevel inverter in industrial for small and big size, power applications(Kwak, Kim 2009, Takatsuka, Yamanaka et al. 2013, Guedouani, Fiala et al. 2013). The current source can generate different levels as DC link for multilevel inverter. The current source can have different levels by having a greater number of power devices such as inductors and capacitors. Also, it needs to have more semiconductor devices such as diodes and Switches (MOSFET or IGBT) (Bao, Bao et al. 2011, Li, Anderson et al. 2009, Peng 2003). These methods are a good combination of current sources and multilevel inverter for some applications (Kjaer, Pedersen et al. 2005, Axelrod, Berkovich et al. 2005). The output performance of these types of inverter is good in terms of low total harmonic distortion (THD). The reason of the low THD is that the harmonics in the whole inverter circuit are modulated

(frequency and amplitude modulations 'M_a' and 'M_f') through the control of a single switch (current source switch) (Luo 2007, Gajanayake, Luo et al. 2010b, Cortes, Svikovic et al. 2014). The THD is inversely proportional to the number of levels. The stepping up/down transformers is not required for these types of inverters (Marcos-Pastor, Vidal-Idiarte et al. 2014, Ho, Chun et al. 2015, Ng, Tu et al. 2014a). However, these types of inverter have a high number of power and semiconductor devices, and also these topologies have more power losses in these devices. Additionally the switching losses are high in these types of inverter because of the high switching frequency of the main CSI switch. The controlling system for these types of inverter is complicated because of the numbers of passive devices used are high. Also the number of linear and nonlinear devices increases as the number of levels in the MLI goes up.

2.6.1 Combine current source / H-bridge inverter topology (seven-levels)

Fig. 2-13 shows an example of current source which can generate three different voltage levels (V_1, V_2 and V_3). These voltages can be controlled by changing the duty cycle and the frequency in current source switch (S_1). The output voltage of this circuit is higher than the input voltage. If this current source is connected to an H-bridge inverter then this combination can generate seven levels. The value of these levels could be the same ($V_1 = V_2 = V_3$) or difference ($V_1 \neq V_2 \neq V_3$) which could reduce the THD (Lopatkin 2011, Elsheikh, Ahmed et al. 2011). The number of power and semiconductor devices will increase in this circuit with the request number of levels. This topology has some advantages; transformer less, the output is easily controllable from the single switch (S_1) of the current source, in addition to all the other advantages of multilevel inverters (Malad, Rao 2012, Luo, Ye 2003). However, this topology is high on cost (more devices), less reliable (inductor current does not respond spontaneously to the change in

load) and less efficient (high switching frequency and more devices) compared to other methods (Luo, Ye 2003).

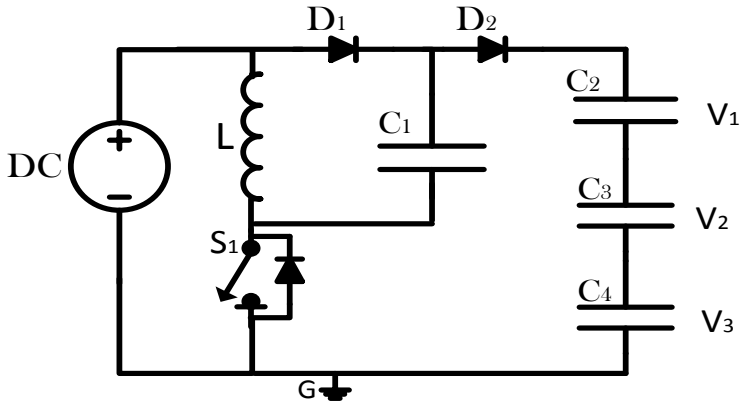


Fig. 2-13 The circuit of 3 different output voltages from current source

There are other types of combination of current source and multilevel inverter, which can have less numbers of semiconductor components. These types of inverter generate different levels of DC-link through the change in the switch duty cycle and frequency. The number of levels is determined by the number of series combination of the DC links (Bai, Zhang et al. 2007, Du, Ozpineci et al. 2009, Jamaludin, Rahim et al. 2014). This type of combination has all advantage of previous combination methods. Also this method has fewer switches for the same number of levels. On the other hand the power losses and power switching losses are high which cause a poor overall efficiency. The controlling system of this method is much complicated than other topologies. Fig. 2-14 shows an example of a combination of a current source with multilevel inverter circuit with fewer components (Axelrod, Berkovich et al. 2005). This circuit generates seven levels only by having seven switches, four diodes, one inductor and three capacitors for single phase (Bao, Bao et al. 2009, Du, Ozpineci et al. 2009, Liu, Tolbert et al. 2008, Axelrod, Berkovich et al. 2004). However, this topology is suited more for high-frequency, low-power applications. Also, this circuit can be used in low frequency DC to

AC inverter for industrial applications. But the value of capacitors and inductance would be increased in high value if the switching frequency of this circuit becomes 50 or 60Hz. So this circuit is not recommended for high power industrial applications.

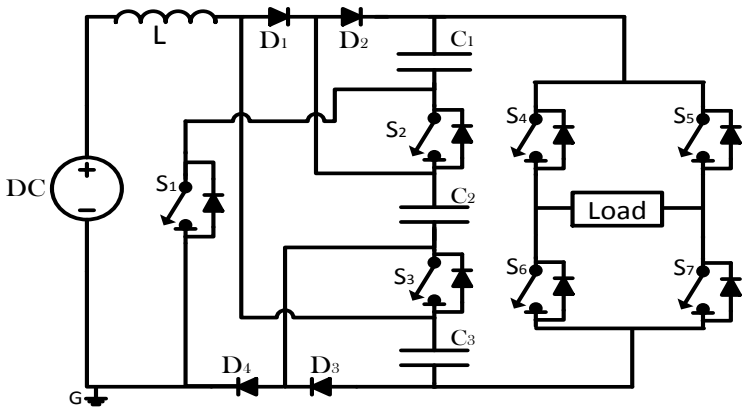


Fig. 2-14 The circuit of combination current source with H-bridge inverter topology (seven-level)

The high number of power and semiconductor devices is the main limitations in these topologies. Also the frequency of the switches in these topologies is high in order to reduce the size of the inductor and capacitor at the DC link. Also the size of the passive filter used is still large. (Axelrod, Berkovich et al. 2005).

2.6.2 Active Buck-Boost Inverter with Coupled Inductors

Fig2-15 shows the circuit of a new topology that is a combination of Buck/Boost current source and H-bridge. This topology can control the switches of the current source (Q_5, Q6, Q7 and Q8) to shape DC voltage (V_i) into a sine wave at the inverter output. The voltage output of the current source increases step by step until the maximum output is reached, then it decreases to zero (in half cycle). It is repeated in the negative half-cycle. Switches Q_5-Q_8 operate at high frequency in the first half cycle. On the other hand the switches Q_1-Q_4 operate at low frequency 50 or 60Hz(Tang, He et al. 2014a).

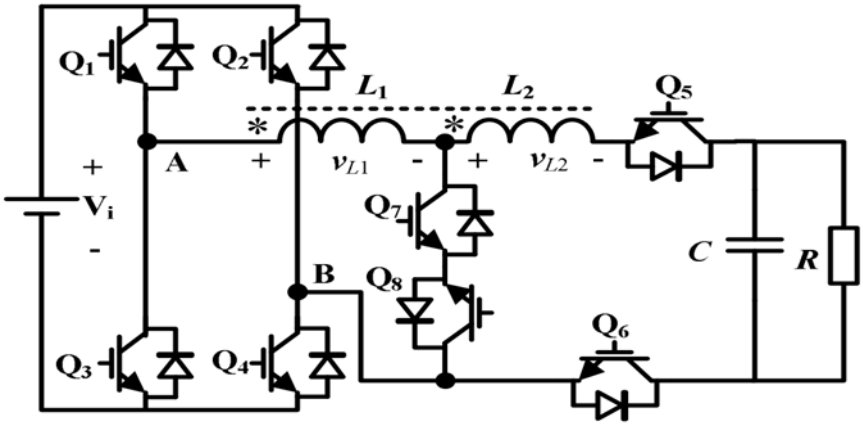


Fig. 2-15 Active Buck-Boost Inverter with Coupled Inductors

This method is the best way to invert DC to AC step-by-step by having fewer switches and capacitors in comparison with previous methods (combination current source with H-bridg). Also the amplitude of lower order harmonics in this method is less than the amplitude of lower order harmonics in other multilevel and three level inverter topologies. The THD in this topology is about 10-15% without using passive filters on the load side. The efficiency of this topology is still on the low side in comparison with previous configurations (Current source inverter) due to the high switching frequency and the losses in inductors. The reason is that two switches operate at high frequency (typically 20 kHz) during the positive half cycle while the other two operate at the negative half cycle; so that the switching losses over a whole complete cycle is only related to two switches (Tang, He et al. 2014b). However, this method has some limitations and for these reasons a recent topology (transformer-less boost inverter) was introduced.

2.6.3 Transformer-Less Boost Inverter

This recent topology introduces normal boost DC to AC inverter with intelligent ideas to reduce switching power losses in switches of the H-bridge (Chakraborty, Hasan et al.

2014). The main switch of the current source is operating at high frequency to reduce the size of L and C in the current source inverter. This circuit is designed as transformer-less boost inverter. Fig.2-16 shows the circuit, which includes five switches and one diode as semiconductor devices. The capacitor and inductor of the current source can step up the input voltage to a higher voltage by switching the main switch (S). This circuit operates as a normal current source inverter, but only two switches (S_1 and S_2) at H- Bridge operate at high frequency in one half cycle. The other two switches (S_3 and S_4) operate at the output frequency (50 or 60 Hz). So the switching loss is reduced in the H-bridge because only two switches are operating at high frequency (SPWM) in half cycle. However, this method has a poor THD at the output, therefore a large passive filter is required to reduce it to less than 5%. On the other hand, this circuit could be suitable for low power applications such as residential photovoltaic applications where the power rating is small and the cost is an important factor.

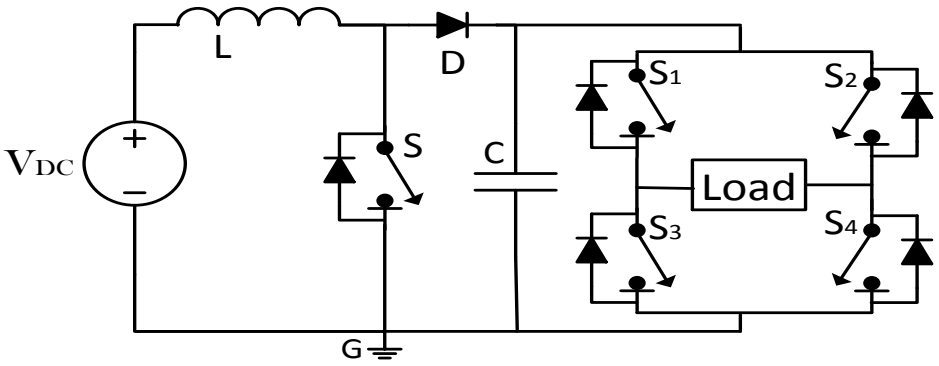


Fig. 2-16 Transformer-Less Boost Inverter

The active buck-boost inverter with coupled inductors has the following limitation over this topology (transformer-less Boost Inverter):

- Two inductors.
- Using freewheel diodes of switches to direct current in load side, this causes more losses and voltage drop at diodes.

- Two switches and two diodes are working at high frequency
- Controlling of switches in this method is more complicated.
- Lower efficiency because having more switches and an inductor

However, this topology still has some limitations such as a high THD and a total of two switches operate at high frequency. Researcher in the field came out with recent topology (Chakraborty, Hasan et al. 2014), which overcomes some of the previous limitations. This topology is called "buck/ boost inverter connected to H-bridge"

2.6.4 The Buck/ Boost inverter connected to the H - bridge

Fig.2-17 shows the circuit of the buck/boost with H-bridge inverter topology which is introduced by Konstantinos Georgkas in IEEE (Georgakas, Vovos et al. 2014). This topology has some advantages, which include a smaller number of switches and inductors in comparison to previous topologies. There are only five switches in this method of which four switches operate at low frequency and one switch operates at high frequency (SPWM). Also, this method uses a single diode to direct current from H-bridge to the buck-boost inductor (L). This advantage can be seen in comparison with the four high switching frequency freewheel diodes used in Fig. 2-15(Georgakas, Vovos et al. 2014).

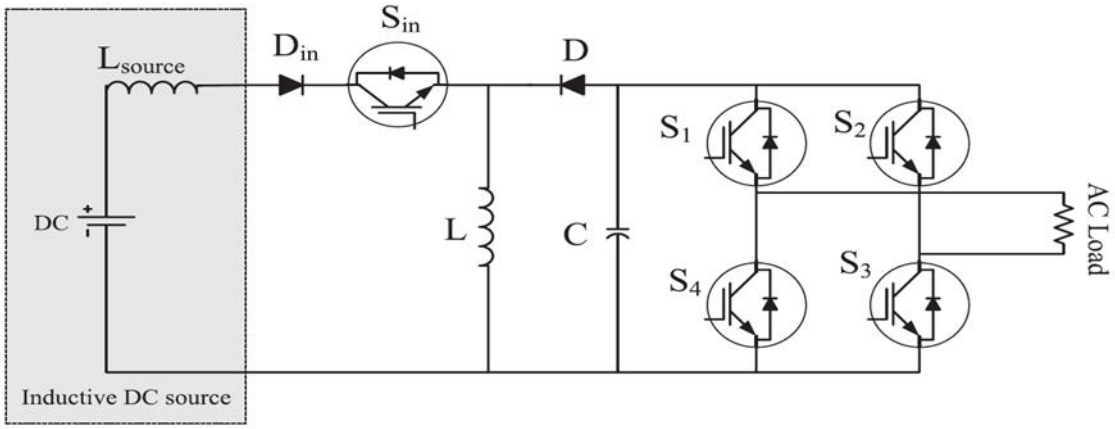


Fig. 2-17. The circuit of Buck/ Boost inverter connected to the H - bridge

However, the output voltage of these two methods (Fig. 2-15 and Fig. 2-17) is the samilar (Georgakas, Vovos et al. 2014, Tang, He et al. 2014b). The output of the BUCK/BOOST inverter is a sinewave with low total harmonic distortion occurring around the switching frequency. The output is inverted from DC to AC by H-bridge. The DC input of the H-bridge is shown in Fig.2-18, which is mainly the voltage across the capacitor (V_C). This voltage (V_C) increases from zero to maximum and then zero again in small steps and this is repeated every 10ms. The H-bridge alternates the waveform every 20ms to shape a 50Hz output.

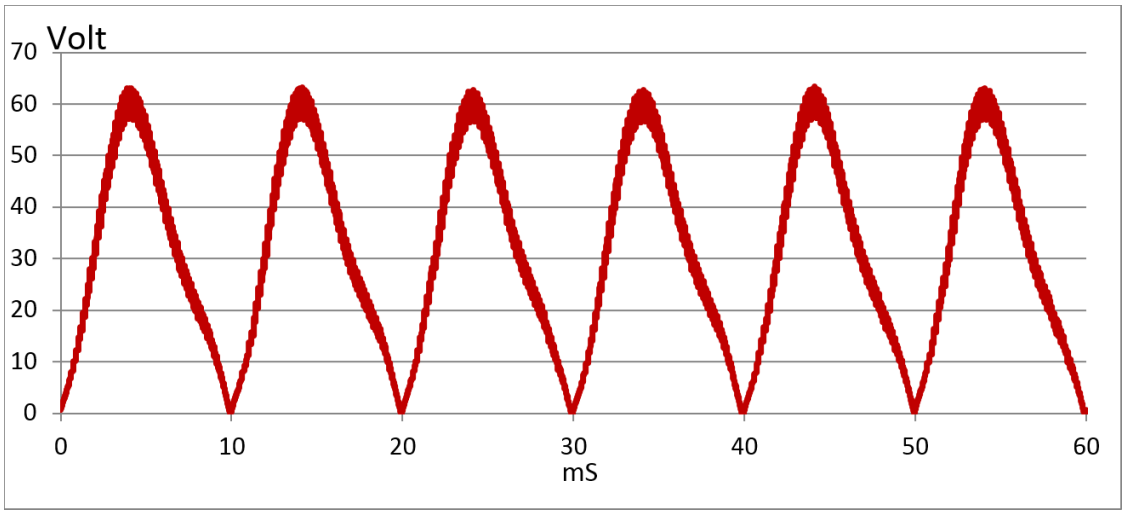


Fig. 2-18 The DC input voltage of H-Bridge in circuit of Buck and Boost inverter

The Fig.2-19 shows the voltage across the load (output from the H-bridge inverter). The total harmonic distortion of this topology is 13.3%. The 3rd harmonic in this case is 12.63% of the fundamental component. The 3rd harmonic of the voltage waveform can be eliminated by optimising the switching pattern of the current source. The THD is then reduced to less than 5% without the need of any filtering (Georgakas, Vovos et al. 2014, Madouh, Ahmed et al. 2012, Tang, He et al. 2014b).

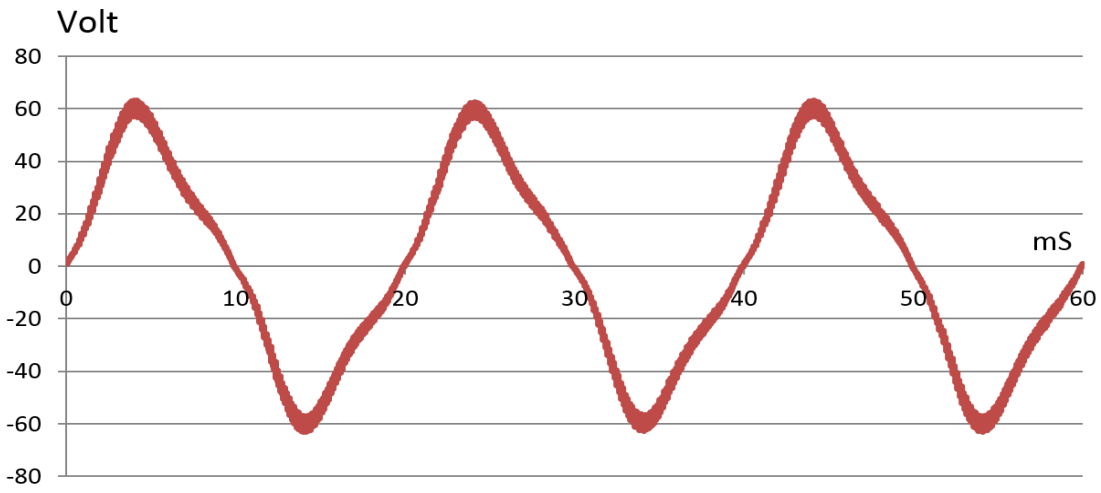


Fig. 2-19 The output voltage of H- bridge without passive filter.

In this topology, the output voltage can be increased or decreased by changing the amplitude modulation ratio in the main switch of the current source. Also the size of the inductor and the capacitor of the current source can be decreased by increasing the frequency modulation ratio in the main switch of the current source. Also the size of the output filter can be chosen by optimising the switching pattern and the frequency modulation ratio in the main switch of the current source (Georgakas, Vovos et al. 2014). However, this topology has some limitations which are:

- The inductor value is big for this 20 KHz topology. The value of inductor for the buck and boost is 1mH and rated at 30A.
- The value of the capacitor is very big for this 20 kHz topology. The capacitor value for the buck and boost is 10 mF and rated at 450 volts. This is the reason that the 3rd harmonic is very high in this case. The switching pattern is then optimised in order to eliminate the 3rd harmonic.
- The voltage ratio of the output over the input is limited in this case. So a transformer is required to step the voltage up. For example, if the input voltage is 90V d.c., the maximum value of the rms of the output voltage will be 110V.

- In this topology, source inductor was not taken into consideration. Obviously, if it is considered then more devices will be required for freewheeling action.

Finally, this circuit is suitable for connecting renewable energy sources to the grid and in the use of UPS systems in low power applications (Georgakas, Vovos et al. 2014). So far there are nine topologies, which have been reviewed in this chapter. Perhaps by putting their advantages and limitations together in a critical way, then a clearer picture will emerge.

2.7Critical Review of the Different Topologies

Table 2-2 illustrates a comparison between different topologies of DC to AC inverters, which was explained in this Literature Review. This table compares the efficiency (η), Total Harmonic Distortion (THD), Sum of n^{th} Harmonic Distortion (SHD), Number of Semiconductor Devices (NSD), Number of Power Devices (NPD), Semiconductor Power Loss (SPL), Control System (CS), Cost and Electromagnetic interference (EMI). This comparison between these topologies has been carried out for the same power rating and the same output/input voltage ratio.

The different topologies compared in table 2-2 are:

- Voltage Source Sine Pulse Width Modulation (VSSPWM) (Zhang, Wang et al. 2014)
- Current Source Sine Pulse Width Modulation (CSSPWM) (Takatsuka, Yamanaka et al. 2013)
- Diode clamped Multilevel inverter (DCMI) (Duggapu, Pulavarthi et al. 2013)
- Capacitor Clamped Multilevel inverter (CCMI) (Kanimozhi, Geetha 2014b)
- Cascading H-Bridge Inverter (CHBI) (Lakshmi, George et al. 2013)
- Combination of Current source with Multilevel inverter (CCSMI) (Axelrod, Berkovich et al. 2005)

- Active Buck-Boost Inverter with Coupled Inductors (ABBICI) (Tang, He et al. 2014b)
- Transformer-Less Boost Inverter (TLBI) (Chakraborty, Hasan et al. 2014)
- Combination Buck/Boost Converter and H-bridge Inverter (CBBCHI) (Georgakas, Vovos et al. 2014)

Table 2.2 is comparison between different topologies of DC to AC

Topology	η	THD	SHD	NSD	NPD	SPL	CS	Cost	EMI
VSSPWM	Low	High	Low	Low	Low	High	No	Low	High
CSSPWM	Low	High	Low	Low	Low	High	No	Low	High
DCMI	Good	Low	High	High	High	Low	Yes	High	Low
CCMI	Good	Low	High	High	High	Low	Yes	High	Low
CHBI	Good	Low	High	High	Low	Low	Yes	High	Low
CCSMI	Good	Low	Low	High	High	High	Yes	High	Low
ABBICI	High	Low	Low	Low	Low	High	Yes	Low	Low
TLBI	High	High	Low	Low	Low	High	Yes	Low	High
CBBCHI	High	Very Low	Low	Low	Low	High	Yes	Low	Low

In general, table2-2 shows that the best topology is the Combination Buck/Boost Converter and H-bridge Inverter CBBCHI in comparison with other method in this thesis**.** However, this method has some limitations, which have been summarised in section 3-1. One of the main limitations is the high switching frequency on the buck and boost DC-to-DC converter. Also the di/dt in the inductor and the main switch of the DC-DC converter at low frequency is higher in this case. This means that the switching power losses are high at both low and high switching frequencies.

In order to overcome the limitations of all previous topologies and in particularly the last one, a new control algorithm is introduced in this thesis. The proposed control operates a single switch at 2 kHz and operates the four H-bridge switches at 50 Hz. Chapter 3 covers two new different control algorithms where the small size of passive filters is required in comparison to other control techniques. Also in the proposed algorithm the values of the buck/boost 'L&C' are reduced in comparison with other techniques.

Chapter 3 Buck/Boost Based Low frequency inverter topology

3.1Introduction

There are three main types of DC/AC inverter topologies from a summary of the background of inverter in chapter two, which are The Pulse Width Modulation (PWM), Inverters the Multilevel Inverters (MLI) and a combination of the PWM and the MLI inverter topologies.

The PWM is based on generating an output voltage (voltage source inverter) or current (current source inverter). All PWM inverters are 3-levels. Although the THD is constant for PWM inverters (before any filtering), the higher switching frequency pushes the lowest order harmonics to a higher value which can be filtered with a smaller filter size. However, the high switching frequency causes higher switching losses which are one of the limitations of PWM inverters (Moghadam, Darwish et al. 2013).

The MLI is based on shaping the output voltage through generating an output waveform at different levels. The number of levels is an odd number (5, 7, 9, etc.). The higher level number results in lower Total Harmonic Distortion (THD). However, it is also obvious that the higher the level number requires more number of semiconductor switches, capacitors, and voltage sources; depends on the configuration used in MLI (Arman, marques et al. 2012). Because of the mentioned limitation, researchers in the field of DC/AC inverters came with the idea of a buck/boost based inverters (Moghadam, Darwish 2012). The main concept is to shape the output waveform through a boost converter prior to the conventional H-bridge configuration. The limitation of the buck/boost-based inverters is that the H-bridge still operates at a relatively high switching frequency (Li, Liu et al. 2009, Chakraborty, Annie et al. 2014, Wu, Ji et al. 2015b); or it consists of multiple numbers of inductors, large number of semiconductors and operate relatively high switching frequency (Chen, Liang et al.

2013, Tang, He et al. 2014b, Ho, Chun et al. 2015, Du, Ozpineci et al. 2007). It also consists of a large value of inductor and capacitor with high frequency in the CBBCHI circuit (Georgakas, Vovos et al. 2014). To overcome all the previous limitation, a proposed circuit has introduced a new control system in current source inverter topology which is based on the idea of the buck/boost-based inverter.

In the proposed circuit the switching frequencies of the buck/boost part as well as in the H-bridge are much lower and hence the proposed inverter has much lower switching losses. The proposed circuit has also less number of semiconductor devices (switches and diodes), less number of power devices (DC voltage sources and capacitors). The main idea is to buck/boost a constant DC voltage source in order to produce a sinusoidal AC voltage. This is done through two stages; the first stage uses a single switch buck/boost converter which operates at relatively high frequency (similar to the sinusoidal pulse width modulation) and the second stage uses a basic square wave inverter which operates at 50/60 Hz frequency. The main concept is to have a high efficient topology (based on low frequency inverter) and a sinusoidal shaped output voltage (based on the frequency modulation of the boost converter). Losses within the single-switch, single-diode buck/boost converter are much less compared to switching losses associated with several semiconductor switches/diodes used in VS-MLI.

The Buck/Boost based low frequency inverter (BBLFI) can invert DC voltage to AC output voltage with high efficiency and low total harmonic distortion (THD) with no filter. High power loads can be used in this type of inverters because the switching frequency of the current source and H-bridge inverters are low, so efficiency is high. The THD can be reduced to 6% without using filters, because the output voltage is multi-stage. Also, this type of inverter can control the output voltage by controlling the duty cycle of the current source switch which is very useful for maximum power point tracking for renewable energies. Additionally, this circuit can be used as motor drive in increasing voltage and frequency in order to control the speed. Fig.3-1 shows a block diagram of the proposed boost-based low frequency inverter (BBLFI).

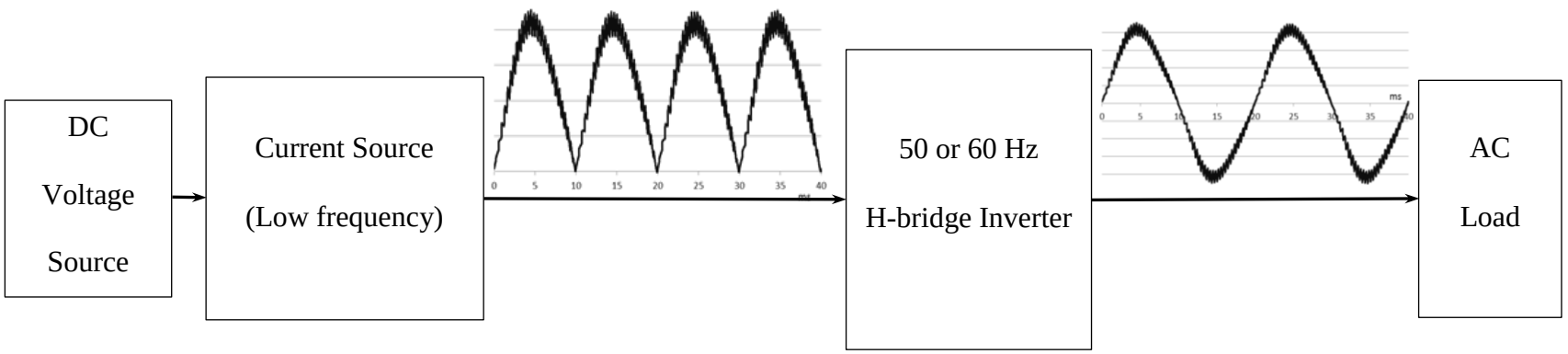


Fig. 3-1 A block diagram of the proposed boost-based low frequency inverter (BBLFI).

The proposed circuit focuses to change the switching pattern in buck/boost converter is closer to a sinusoidal waveform. So there are two different switching pattern buck/boost converter.

This chapter includes two sections which are:.

- Pulse Width Modulation (PWM) controller for BBLFI topology (section 3.2); explains how this proposed circuit is designed (switching pattern 1). Also, this section includes simulation of proposed circuit as well.
- Rectifier Sinusoidal Pulse Width modulation (RSPWM) controller for BBLFI topology (section 3.3) explain how this proposed circuit is improved (switching pattern2) to have better efficiency, less THD and minimised lower harmonic order distortion. Also, this section includes simulation of proposed circuit.
- Section (C); finalising these two switching patterns of buck/boost inverter.

3.2Pulse Width Modulation (PWM) controller for BBLFI

In this section the controller and the simulation of the proposed circuit are introduced

3.2.1 Proposed circuit topology with PWM controller and analysis

A good performance in MLI is associated with either a large number of split DC sources or equivalent number of DC capacitors in order to achieve the multilevel voltage (Moghadam, Darwish et al. 2013). The switching pattern of the inverter is selected in a way in order to have the desired output voltage level. If more levels are required, then more DC sources or capacitors are added. Also, if the amount of switches increase, the power losses (switching losses) also increase. In this section a single DC source is used and the level of the output voltage can be controlled through buck/boost configuration in order to achieve the required frequency and voltage by controlling the duty cycle and frequency of switch in the buck/boost converter (Marouchos, Darwish et al. 2013). This

can be achieved through the control of the switching pattern of the buck/boost circuit without the need to add more semiconductor switches, DC supplies or capacitors. In this section the switching frequency of Buck/Boost converter is chosen to be at 2-3 kHz and the output frequency of the inverter is 50 Hz. This section demonstrates the principle of operation of the proposed topology. However It is essential before considering the topology of the Buck/Boost based Low frequency Inverter (BBLFI) to introduce the following features which distinguish this proposed topology in comparison to other types of DC/AC inverters (Moghadam, Darwish 2012, Marouchos, Xenofontos et al. 2014).

1. The BBLFI is integrated buck/boost converter with full H bridge inverter.
2. The output voltage of the BBLFI can be controlled by varying the switching frequency and pattern of the buck/boost section.
3. The output frequency of the BBLFI can be controlled in the same way as other DC/AC inverters. This is achieved by selecting the appropriate (1/T), where T is the time for the fundament frequency component.
4. The single source used in the BBLFI can be increased if the output voltage required to be stepped up or down in huge steps.

Fig. 3-2 shows the proposed BBLFI power circuit. The circuit includes one DC voltage source, one inductor, one capacitor, one diode and five semiconductor switches. The operating frequency of the buck/boost converter switch (S) is 2 kHz, which is quite high for large power applications. The frequency of the H-bridge switches is 50 or 60 Hz.

This proposed circuit operates in 3 modes within a 50/60 Hz cycle. The first mode is increasing the voltage across the H-bridge (V_{AB}) from zero to peak value of a controlling switch (S) in the first 5ms of the half cycle (0 to 5ms).

- The second mode is decreasing V_{AB} from the peak value to zero in the second 5ms half cycle (5ms to 10ms).
- The third mode is to change polarity at the load from positive to negative every 10ms (half cycle).

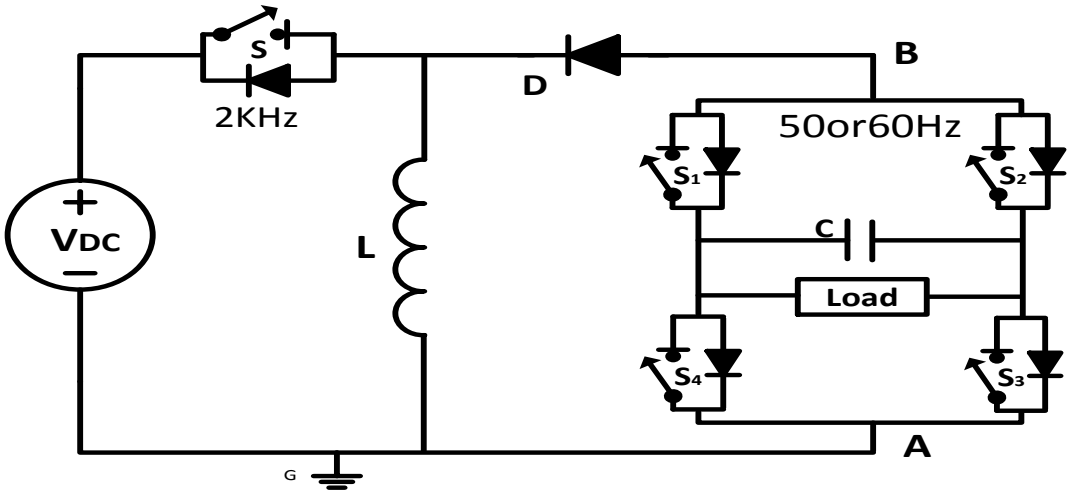


Fig. 3-2 The proposed buck/boost based low frequency inverter power circuit

Fig3-3 shows the diagram control signal of main switch (S) buck/boost converter. This control system has two pulse generators. First one generates 2 kHz pulses and the second one generates 100 Hz pulses. So there are 4 input signals from these two pulse generators.

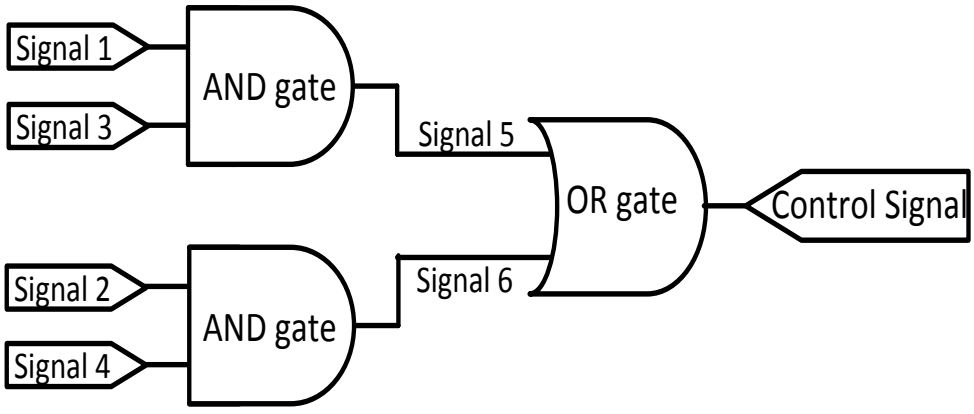


Fig. 3-3 control logic circuit of main switch (S) buck/ boost converter

The frequency of signal 1 and signal 2 are 2 kHz, but duty cycle of these two signals complement each other's. The frequency of signal 3 and signal 4 are 100 Hz with same duty cycle with 180 degree phase shift. The fig. 3-4 shows the inputs and the output signal of control logic circuit. Also, there are 2 modes of the proposed circuit in this figure. Additionally, the signal 2 is the inverse of signal 1. A duty cycle of signal 1 is the D and the duty cycle of signal 2 is (1-D).

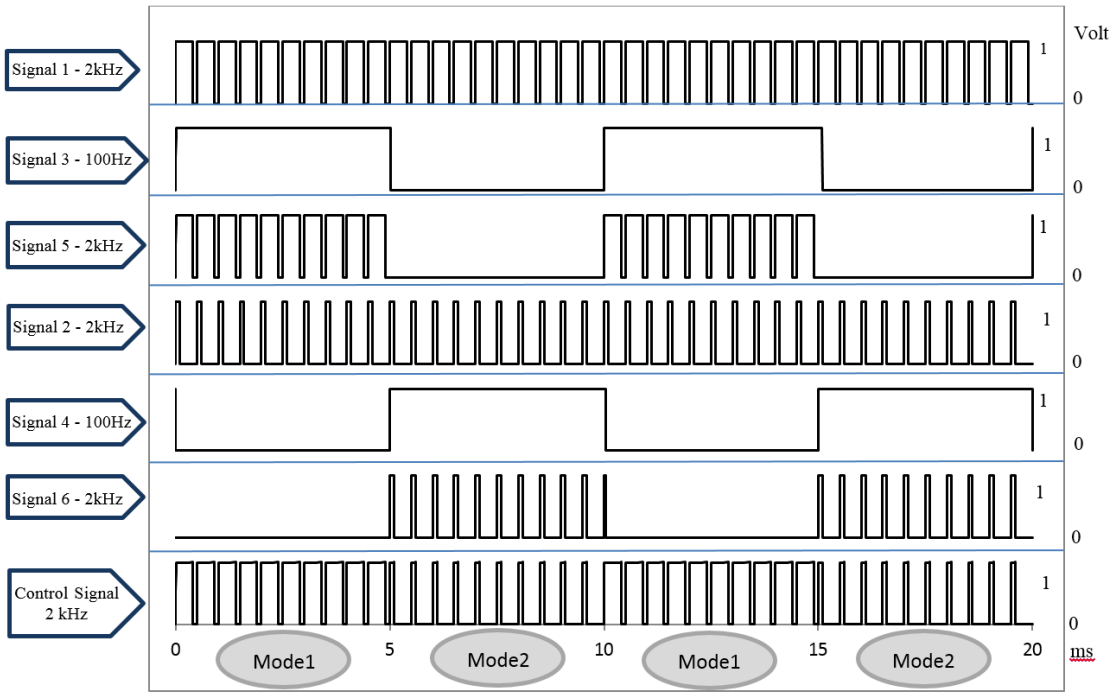


Fig. 3-4 the progress of logic input signals (binary) for controlling main switch (S).

The control signal from switch S is connected to a semiconductor switch (MOSFET or IGBT) driver. This controller is generating pulses in digital (binary number) or analogue (0 or 5 volts). Then this signal becomes the input signal for MOSFET drivers, then the MOSFET driver converts this input signal to 0 and 12 volts. However, a voltage in the capacitor and load increases when the main switch (S) is OFF. The voltage at the load and the capacitor decreases slightly or become a constant when the main switch (S) is ON. So the current is charged in the inductor of the buck/boost converter when switch S

is ON. Then the current charge of the inductor is discharged in the capacitor and the load when the switch S is OFF. The timing of charging the inductor in mode 1 is higher than the timing of charging the inductor in mode 2. This is the reason that the voltage increases in mode 1 and decreases in mode 2. For example the duty cycle of this buck/boost converter is 90% so the r.m.s output voltage is boosted for this case. The output voltage of this circuit can easily increase and decrease by controlling the duty cycle of the main switch (S) in the buck/boost. Also the number of increasing and decreasing steps can be controlled by changing frequency in the main switch.

Fig3-5 shows a process of load output voltage from mode 1 to mode 3. The voltage increases large steps up from zero to peak value in V_{AB} in first mode (0 to 5ms). The V_{AB} is the voltage across the H-bridge and this voltage is an input DC voltage for the inverter. The voltage V_{AB} is decreased in small steps down to zero value in the second mode (5ms to10ms). These two modes are repeated every 10ms for 50 Hz inverter.

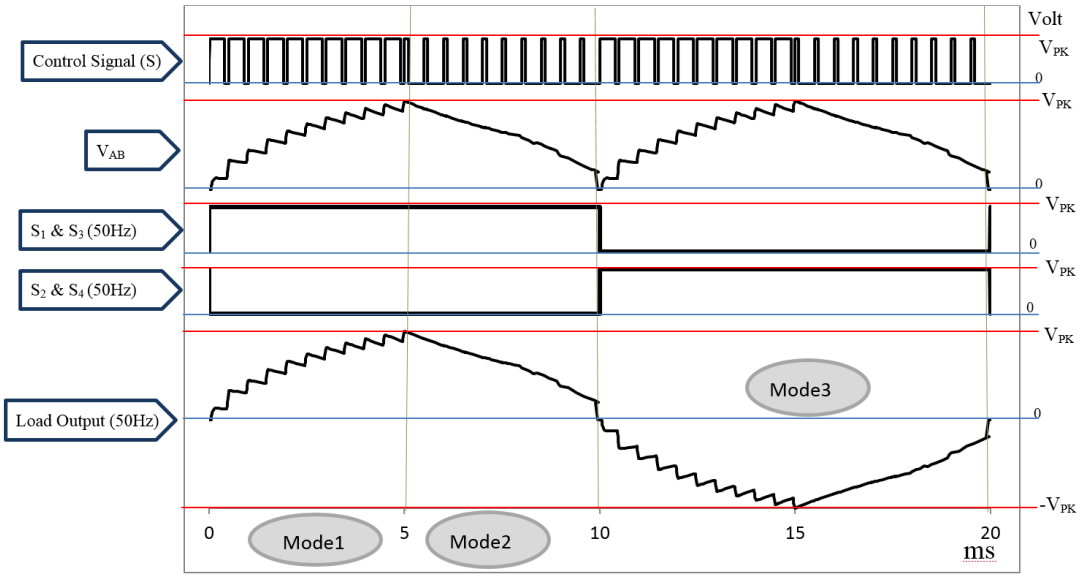


Fig. 3-5 control signals for switch S, S1, S2, S3 and S4 and output voltage from current source and H-bridge.

The next mode is to invert DC (V_{AB}) voltage to AC output voltage across the load, which is mode 3 in this process. The switches S_1 & S_3 are ON at the first 10ms (0 to

10ms) and these two switches are OFF during the following 10ms (10ms to 20ms). The switches S2 and S4 are ON from 10ms to 20ms. So the load voltage is the same as V_{AB} in the first 10ms and the load voltage is negative value of V_{AB} for the following 10ms in the third mode. Then these three modes are repeated every 20ms for 50 Hz output voltage in the inverter. Finally the input DC voltage is boosted in the Buck/ Boost – based Low Frequency Inverter then the output is inverted to AC. The BBLFI topology has the capability to invert single DC voltage source to multilevel AC output by having one small capacitor (100µF), one small inductor (100µH), one diode, one switch operating at 2 KHz, four switches operating at 50 or 60Hz. In this topology, if the switching pattern is optimised to eliminate low order harmonics, then it has a potential to reduce THD to less than 10% with no filter connected. So this topology has more advantages than CBBCHI topology (Georgakas, Vovos et al. 2014). The switching frequency of CBBCHI topology is 20 kHz and using a bigger size inductor (1mH) and capacitor (10mF) to buck/boost DC to DC (Gajanayake, Luo et al. 2010a). The BBLFI can invert DC to AC with lower value of inductor, lower value of the capacitor and lower switching frequency in comparison to CBBCHI topology.

The voltage ratio of BBLFI circuit can be controlled by changing the duty cycle of the control signal main switch (S) in the buck/ boost converter. The voltage ratio of this topology is between 0.8 to 4, with no need to change any of the passive devices (capacitor or inductor values), in the BBLFI circuit. However, there is a limitation in having a high voltage ratio as this may cause an increase in the low order harmonics specially 3^{rd} and 5^{th} harmonics. For example the 3^{rd} harmonic is 12% of the fundamental in a voltage ratio of 4. This limitation causes to increase THD in the output waveform and hence a passive filter will be required to reduce the THD. Also the THD can be reduced to less than 10% by changing the frequency and duty cycle in the control signal

of the main switch (S). However, the THD of this circuit is reduced to less than 5% by using small size of inductor connected in series with the load. So this circuit has the following advantages in comparison to CBBCHI topology (Georgakas, Vovos et al. 2014).

- The small size of inductor and capacitor for a buck/boost converter. The inductor size of the BBLFI circuit is 100μH which is 10 times smaller than the inductor size of the CBBCHI circuit. The value of the capacitor in BBLFI circuit is 100μF and this value is 100 times smaller than the capacitor in the CBBCHI circuit (Georgakas, Vovos et al. 2014).
- There is no need to use transformer in the BBLFI circuit for higher voltage ratio (less cost). For example transformer is requested in CBBCHI where the voltage ratio in this circuit is four (Georgakas, Vovos et al. 2014).
- Lower switching frequency in the main switch of the buck/ boost converter in BBLFI circuit. For example the switching frequency in CBBCHI topology is 20kHz in the main switch, which is 10 times bigger than the switching frequency in BBLFI topology (Georgakas, Vovos et al. 2014).
- The BBLFI topology has less switching and conduction power losses.

On the other hand, this topology has the following limitations in comparison with CBBCHI..

- Higher amplitude of low order harmonic distortion, especially 3^{rd} harmonic.
- Higher ΔI in inductor of the BBLFI circuit.

These two limitations can be solved by changing the duty cycle and frequency in the main switch of the buck/boost converter in the BBLFI. So the BBLFI circuit needs to have different modes for half cycle. These modes can have different duty cycles in the control signal of the main switch in BBLFI for half cycle. For example, there are five

modes in the control signal of the switch in the BBLFI circuit which can eliminate lower order harmonic distortion in the output. Fig.3-6 shows the control signal of the main switch (S) which shows 5 different modes. These modes (switching pattern) are chosen manually by trial and error to find a good solution in generating multistep with low THD. A program can be used in order to optimise the switching pattern to reduce THD and minimise lower order harmonic distortion. However, it is really complicated to generate different duty cycles and frequencies in one control signal in this method. Additionally, section 3-3 chapter has a better solution for less complicated control logic circuit for the control signal of the main switch (S).

Fig.3-6 shows an example of five modes in digital (binary) control signal for the main switch in the BBLFI circuit for half cycle (10ms) of the output. The duty cycle is 70% and the frequency is 2 kHz in the first mode. The first mode is from zero to 2ms. The duty cycle is decreased to 60% at the same frequency during the second mode (from 2ms to 4ms). The frequency is increased to 4 kHz during the third mode (4ms to 5ms) and the duty cycle is 60%. The frequency is the same as in the previous mode (4 kHz) but the duty cycle is 20% during the fourth mode (5ms to 7ms). The frequency decreases to 2 kHz and the duty cycle decreases to 10% in the last mode (7ms to 10ms). These modes are repeated every 10ms in order to control the main switch in the buck/boost circuit. Then the buck/boost circuit forms the input DC voltage across the H-bridge (V_{AB} in Fig.3-2). H-bridge inverts the V_{AB} to AC voltage across of load. This example control signal is applied to simulate circuit in part 3.2.2 which is the simulation part (PSPICE software) of this chapter.

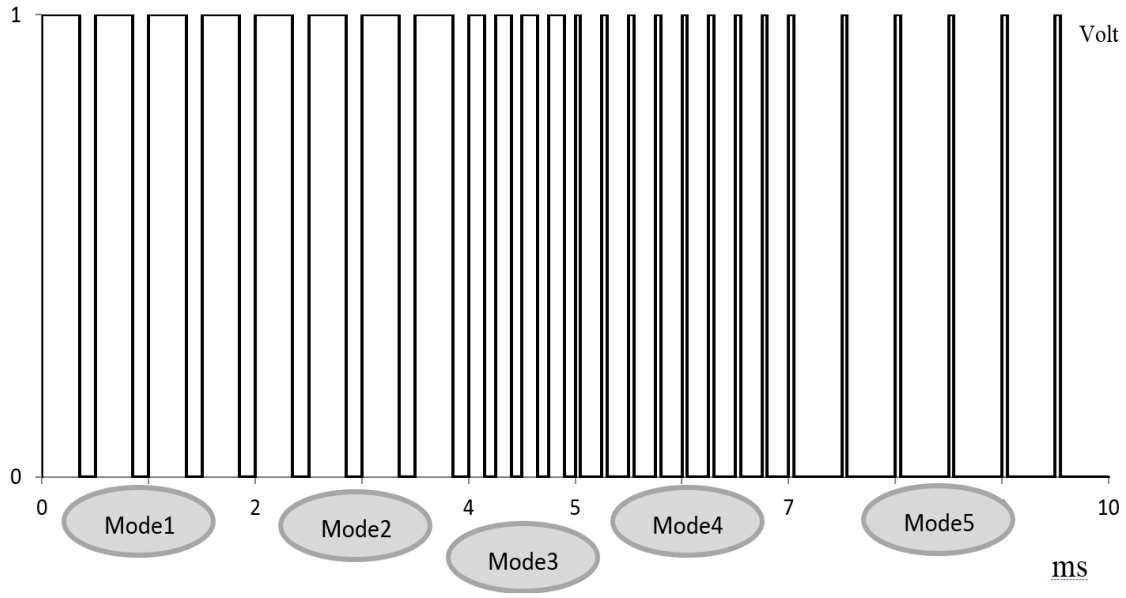


Fig. 3-6 An example of digital control pulse of main switch (S) in BBLFI topology in five modes.

3.2.2 Simulation of BBLFI topology with PWM controller

The Buck/Boost-based low frequency inverter topology is simulated in PSpice software. The load and input DC voltage of this circuit in this simulation are chosen to be the same as the load and input DC voltage in CBBCHI circuit (Georgakas, Vovos et al. 2014). The load and the input voltage are 54Ω and 30 volt DC.

Fig.3-7 shows the proposed simulation BBLFI circuit. The circuit includes one DC voltage source, one inductor, one capacitor, one diode, a control circuit (V pulse is used as the control signal circuit in PSpice simulation) and five semiconductor switches (MOSFETs). This circuit is simulated on PSpice software with the following circuit parameters:

30V V_{DC} source; Load (R=54Ω), buck/boost capacitor (100μF) in load side, inductor (100μH), one diode (D1N5404), MOSFET (IRF150 in PSpice) and V-pulse source. V-pulse source is programmed to generate the same control signal shown in fig.3-6.

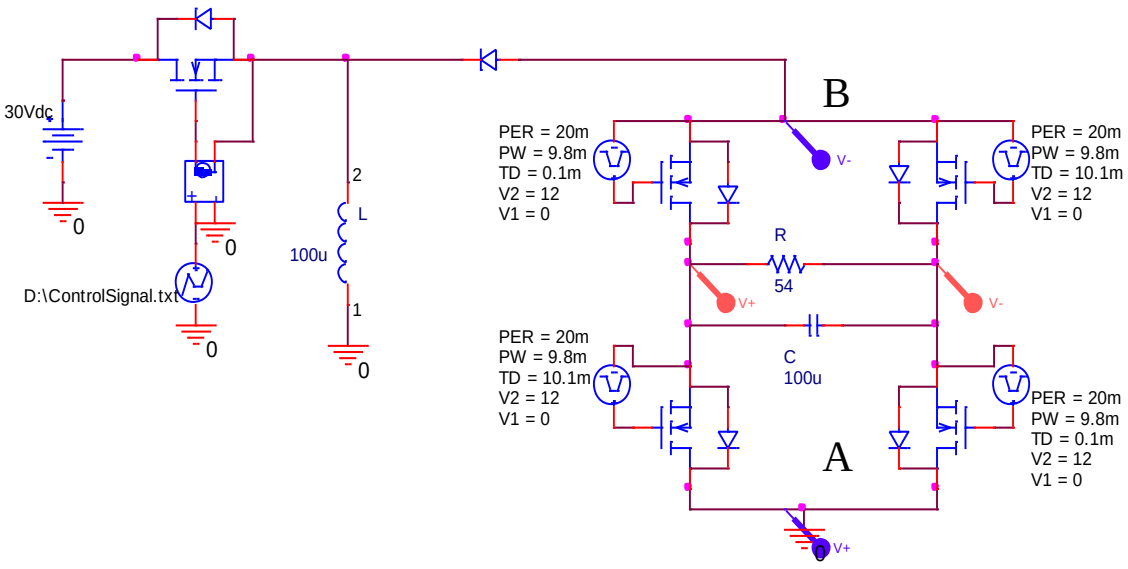


Fig. 3-7 proposed simulation BBLFI circuit in PsPice software

The frequency of the semiconductor switch used in the buck/boost converter is 2 kHz in mode 1, mode 2 and mode 5. The switching frequency in the third and fourth modes is 4kHz. The switching frequency of the H-bridge is 50Hz; there is 0.1m time delay in the H-bridge to switch ON. This delay can reduce the value of 3rd harmonic at the output. The value of inductor in this simulation is 10 times smaller than the inductor in CBBCHI (Georgakas, Vovos et al. 2014). Also the capacitor in this simulation is 100 times smaller in comparison with the capacitor in CBBCHI circuit (Georgakas, Vovos et al. 2014). However the voltage ratio in this simulation is three. The r.m.s value of output voltage is 90volt when the input voltage is 30 volts. This ratio voltage in this simulation is nearly two times higher than the voltage ratio in CBBCHI circuit (Georgakas, Vovos et al. 2014).

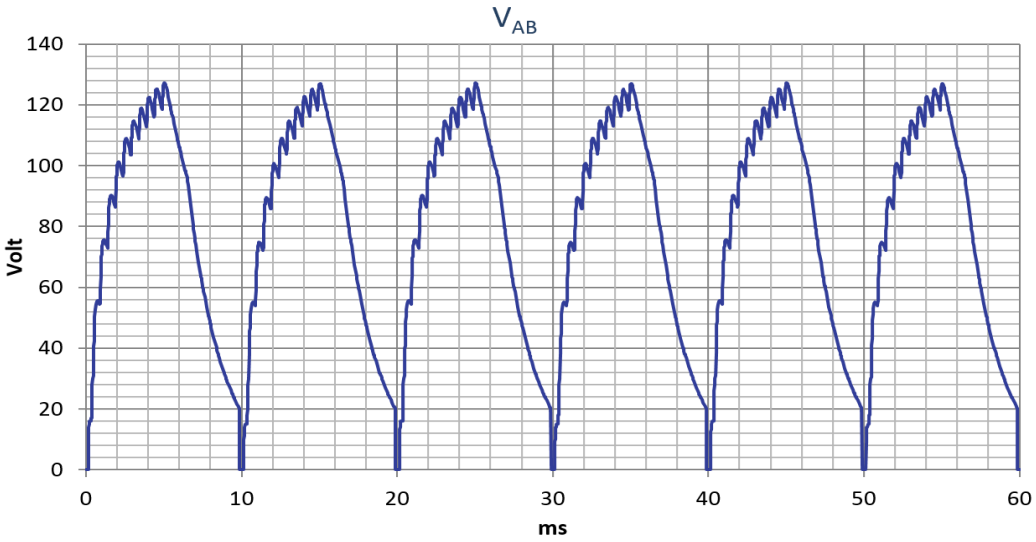


Fig.3-8 The voltage across of H-bridge (DC output voltage of buck/boost converter)

Fig.3-8 shows the voltage across of H-bridge (V_{AB}). The V_{AB} is the DC output voltage of buck/boost converter, which is stepped up from DC voltage sources to 125 volt at the peak value. The Peak value of the V_{AB} can be controlled to be a smaller or larger value than DC source (input voltage in the buck/boost converter). The peak value of V_{AB} depends on loads, type of semiconductor devices (switches and diode) and passive devices (size of the capacitor and inductor). Also V_{AB} can be controlled by changing the frequency and the switching pattern in the main buck/boost converter switch. Therefore, V_{AB} can be easily controlled through the control of the current source switching frequency and the switching pattern instant to change the value of passive devices in the current source. The peak value of the V_{AB} is 125 V which is controlled by the generated signal. This signal is designed to step up DC voltage to 125 V from 30 V input DC source. So the V_{AB} DC can be inverted to the AC output (V_{LOAD}) by switching at 50 Hz in the H-bridge switches as shown in Fig 3-9. The output frequency of BBLFI can be varied from 0 to a value 20 times less than the switching frequency of the main buck/boost switch. The reason for the ’20 times’ value is to keep the THD at an

acceptable level. These voltage and frequency variation are depended on H-bridge switching frequency and switching frequency in the current source. The output rms voltage for this simulation is 88.4 volts, which is nearly 3 times higher than the input voltage. The output voltage increases step by step to the peak value. The value of each step is not the same. The value of these steps depends on the duty cycle of the controller, the value of the capacitor, inductor and switching frequency in the current source. The number of these levels depends on the switching frequency in the current source inverter. The number of steps is increased if the switching frequency is increased in the current source main switch.

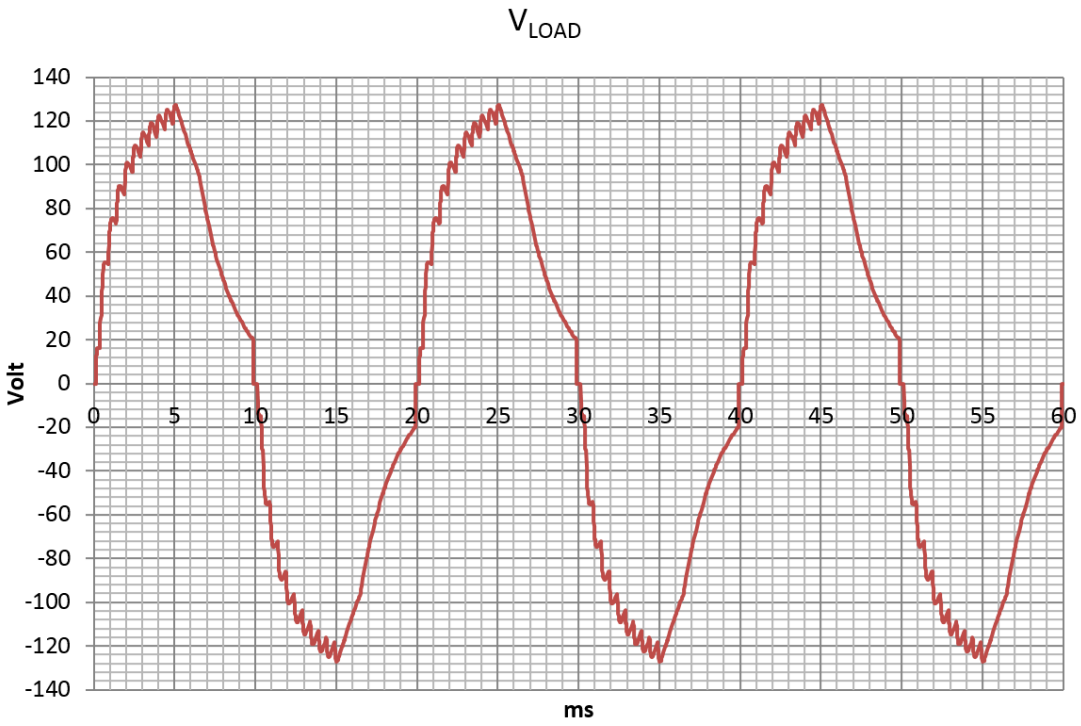


Fig. 3-9 the output voltage of proposed circuit in load side

The voltage at different levels of the output voltage can be controlled from the control signal. These values have a direct effect on the THD and the amplitude of low order harmonic distortion. For example the amplitude of the 3rd harmonic would be increased

if the value of the first step in output increases. Another example, the THD will be decreased if the number of levels increases at the output. Fig.3-10 illustrates the Fast Fourier Transform (FFT) of the generated BBLFI output waveform. The fundamental value of the output voltage is 124.61 volts. The THD is about 7.9% in this simulation. The amplitude of lower order harmonic is quite high in this case. The amplitude of 5^{th} harmonic is 7.9 volts in this simulation. The amplitude of 5^{th} harmonic could reduce to zero by varying the control signal; however, other lower order harmonic amplitudes will be increased. Also the voltage ratio (hence the output voltage) will change if the control signal is varied to eliminate the 5^{th} harmonic. The value of voltage ratio is the main reason in changing the control signal (Fig.3-6).

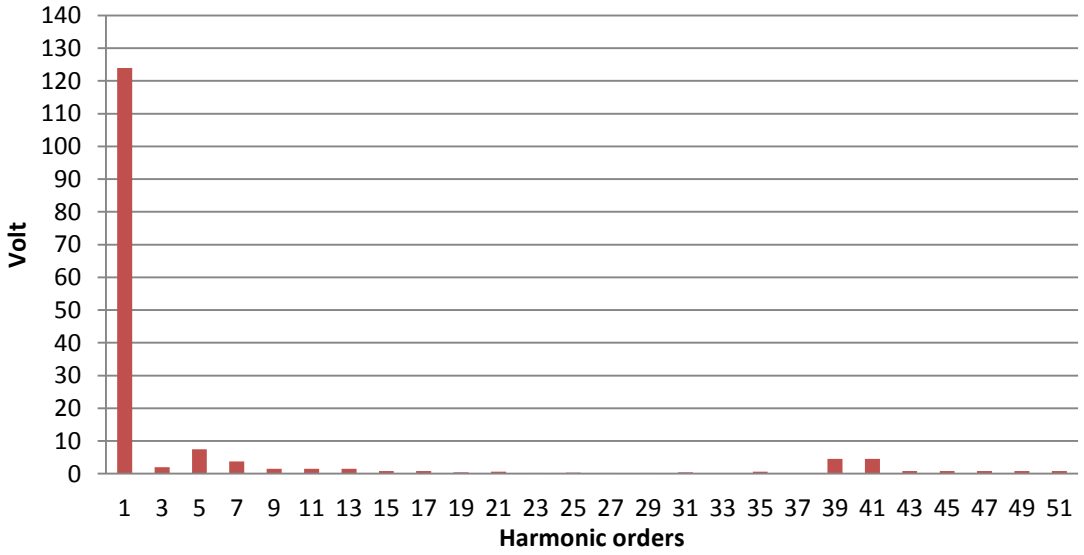


Fig. 3-10 Fast Fourier Transform (FFT) of the output voltage proposed circuit

However, the 5^{th} harmonic can be eliminated by choosing the right value of low pass filter at the load side in order to reduce the THD to less than 2%. Additionally, the THD can be reduced to 5% with no filter if the switching pattern is optimized to eliminate the amplitude of lower order harmonics at the load side. In general, the voltage ratio and THD are the objectives to design signal for controlling the switch in BBLFI with no changes in hard devices (DC sources, inductor and capacitor). This control signal can be

designed for software and programmed to a Micro-controller in practical implementation. Finally, this topology has some advantages and some limitation in comparison to other topologies.

3.2.3 Advantages

- Less switching power loss; the reason is the use of less number of switches in comparison with VS-MLI. Also less switching power loss because of the lower switching frequency in the main switch of the buck/boost BBLFI topology.
- The switching frequency of the buck/boost in BBLFI can control the number of the output voltage levels.
- The size of inductor and capacitor are small at low frequency in comparison with other topologies.
- No need for a transformer to step up or down the voltage.
- This topology can be used as active filter and can also be used in the Maximum Power Point Tracking MPPT (further research need to be carried out).

3.2.4 Possible limitations of BBLFI

1. It requires more complicated control system to reduce the amplitude of the lower order harmonics and to increase and decrease the voltage ratio in BBLFI.
2. The size of the power application for BBLFI is small (less than 1000W for a single phase application).
3. The $\Delta i/\Delta t$ is high in the inductor in boost mode of BBLFI circuit.

Section 3.3.1 introduces a new switching pattern in buck/boost switch which can be a good solution for the first limitation of BBLFI circuit. Chapter 4 describes a new control signal which can sort out the second and third limitations of the BBLFI circuit.

3.3Rectifier Sinusoidal Pulse Width Modulation (RSPWM) to control the buck/boost main switch

3.3.1 Proposed circuit topology with RSPWM controller and analysis

The control signal of the BBLFI circuit becomes very complicated where the control signal width is different in each half cycle. There is a good solution for this problem which is using the proposed Rectifier Sinusoidal Pulse Width Modulation (RSPWM) as a control signal in the main buck/boost switch in the BBLFI circuit. This solution reduces the complication in the control system; where M_a and M_f can be easily varied through the voltage ratio. Also, this method can reduce the amplitude of specific order harmonics in BBLFI only by controlling the value of M_a and M_f in RSPWM. The circuit of this method is the same circuit of BBLFI. The only change of this proposed circuit is in the control signal. This control signal is generated through the comparison of a rectified sinewave and a triangular signal. The proposed circuit has three modes; the first mode is stepping up the voltage from zero to peak value during the first 5ms (0-5ms). The second mode is to step down the voltage from peak value to zero in the second 5ms (5m-10ms). These modes are repeated every 10ms (half cycle) for 50Hz output frequency system. The third mode inverts the positive voltage to negative voltage for the second half cycle in the H-bridge inverter. Fig.3-11 shows the control signal circuit. The firs input voltage to the comparator (op amp) is a rectified 50Hz AC voltage source. The second input voltage of the comparator is a triangular waveform at 1 kHz. Then the output from the comparator needs to be an absolute value zero or 5 volts in the time domain. This control signal can be generated from a Microcontroller as digitised values (high or low). The controller in this case (RSPWM) is not as complicated as the controller in BBLFI (PWM controller).

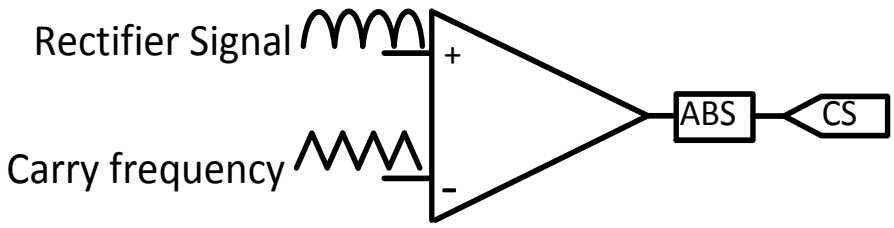


Fig. 3-11 The control signal generator from comparator (SPWM)

The RSPWM controller in BBLFI can easily covert a DC voltage by stepping it up and down into AC voltage in one half cycle. The reason of easily formed waveform is to have different width of each pulse at SPWM. So the output voltage increases to peak value in the first 5ms because the width of the pulses increases during this time. The output voltage decreases to zero because the width of pulses decreases from 5ms to 10ms. Fig.3-12 shows the carrier and rectifier frequencies of the RSPWM. The M_a and M_f of this RSPWM are 0.8 and 20. Also the voltage control signal (0 and 5 volt) is shown in this figure. The control signal controls the main buck/boost switch in the BBLFI circuit.

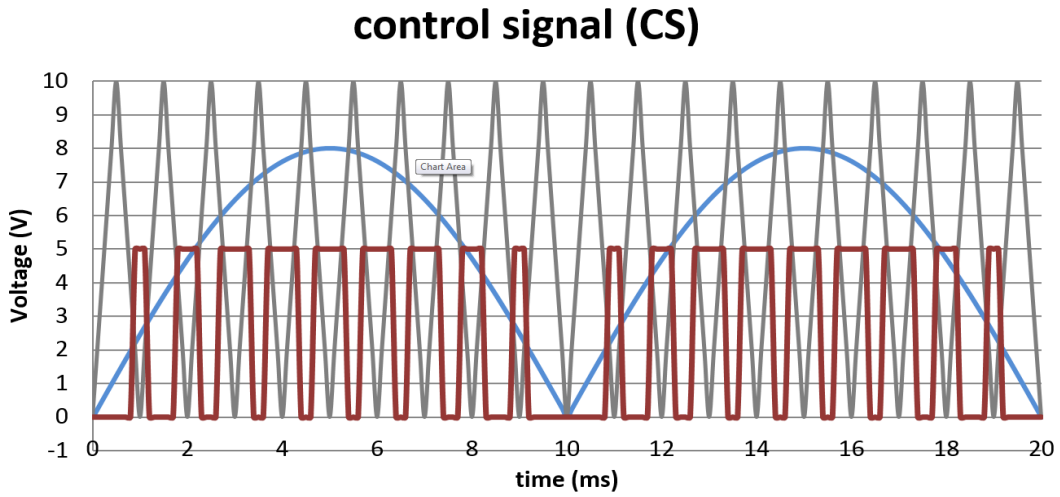


Fig. 3-12 The control signal from SPWM

The control signal with M_f = 40 and M_a = 0.8 is used to control the buck/boost switch of the BBLFI circuit in part (3.3.2). The values have been chosen in order to have a voltage ratio of 3 and small THD.

3.3.2 BBLFI Simulation with RSPWM controller.

The BBLFI circuit simulation with RSPWM controller has the same input and output voltages with the circuit shown in part 3.2.2. The value of inductor, capacitor and the load are 200μH, 50μF and 54Ω. These values are selected in order to have a fair comparison with PWM controller covered in 3.2.2. The switching frequency in the main buck/boost switch is 2 kHz and the switching frequency of H-bridge is 50Hz. Fig.3-13 shows a simulation circuit of BBLFI with RSPWM controller. The simulation circuit includes two main parts, power circuit (BBLFI circuit) and control signal circuit (RSPWM controller). The power circuit includes 5 switches, one diode, one capacitor and one inductor. The value of the inductor in this simulation is two times of the value of the inductor in the simulation part in 3.2.2. The value of the capacitor is half the value of the capacitor in the simulation part in 3.2.2. The controller circuit in this simulation includes a comparator (Op-Amp), AC voltage source, triangle waveform generator and absolute component. The rectifier of AC voltage source is used as the reference signal for the comparator in the controller circuit. The triangle waveform is used as the carrier frequency for the comparator in this circuit. The output pulse from the comparator needs to have absolute value and this is the reason for using the absolute component in this simulation. The absolute value of pulse is a control signal for main switch in BBLFI circuit.

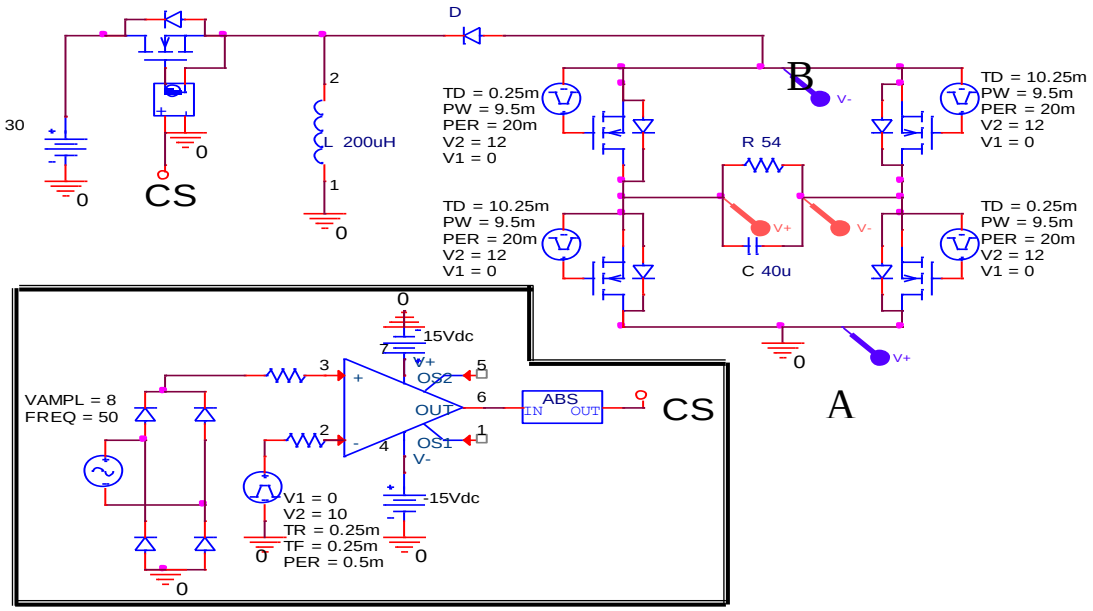


Fig. 3-3-13 circuit of BBLFI with RSPWM controller

The H-bridge inverter operates at 50 Hz in this simulation. The duty cycle of H-bridge switches is 47.5% (instead of 50%) in order to reduce the 3rd and 5th harmonics. So the time of zero level is 500µs in each half cycle. The 500µs at the zero level in each half cycle is shown in the Fig 3-14. This figure shows the voltage waveform across the H-bridge inverter (V_{AB}). The voltage increases from zero to the peak value in 5ms and the voltage decreases to zero in 5ms for each half cycle. The half cycle is repeated every 10ms for 50Hz output frequency.

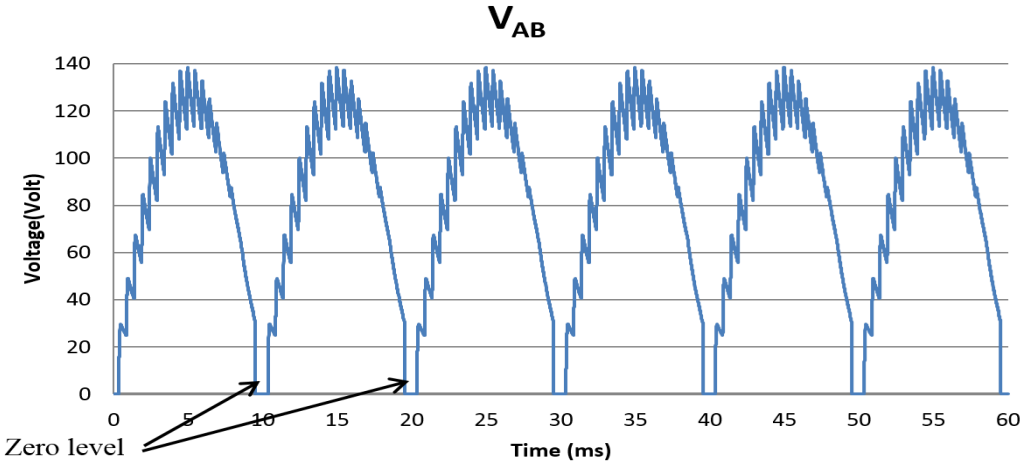


Fig. 3-14 Voltage across H-bridge inverter

However, the peak value of this DC voltage in each half cycle is 127.27 volts with 20% ripple voltage. So the rms output AC voltage at the load is 90volt which is 3 times the input DC voltage. This voltage ratio is varied by controlling M_a and M_f in RSPWM control circuit. Also the voltage ratio can be controlled by programming the microcontroller. The output voltage of this simulation is controlled by choosing the right value of M_a and M_f control-signals (CS). The output voltage of the H-bridge is shown in Fig.3-15 for 3 50Hz cycles. The voltage starts to step up to peak value from 250µs to 5ms. The voltage steps down to zero volts from 5ms to 9.75ms for the positive half cycle. This step up and down is repeated in the negative half cycle as well with 10ms time shift. The time of zero level is essential to reduce the amplitude 3rd and 5th harmonic. THD in this simulation is decreased by reducing the amplitude of both harmonic orders.

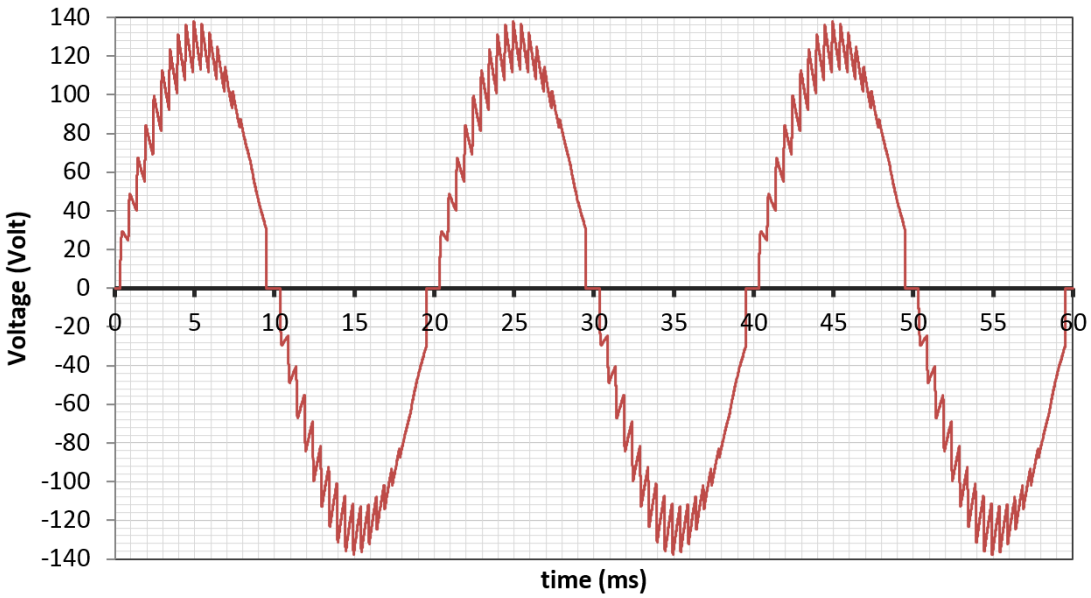


Fig. 3-15 The AC output voltage of H- bridge (load voltage).

The FFT of the AC output voltage is shown in Fig.3-16. This graph shows the amplitude of harmonic from the fundamental to 53rd harmonic voltage. The fundamental amplitude

of the output is 126.844 volts. So THD for this sinusoidal waveform is 8.18%, which is calculated from equation 3-1.

$$THD = \frac{\sqrt{V_{rms\ (output)}{}^2 - V_{rms\ (fundamental)}{}^2}}{V_{rms\ (fundamental)}} \times 100\% \quad (3\text{-}1)$$

Where $V_{rms(output)}$ is the rms AC output voltage of the H-bridge. The $V_{rms\ (fundamental)}$ is the rms value of the fundamental output. The $V_{rms(output)}$ is 90 volts for this simulation and the $V_{rms\ (fundamental)}$ is 89.7 volts. So THD is calculated from equation in below;

$$THD = \frac{\sqrt{90^2 - 89.7^2}}{89.7} \times 100\% = 8.18\%$$

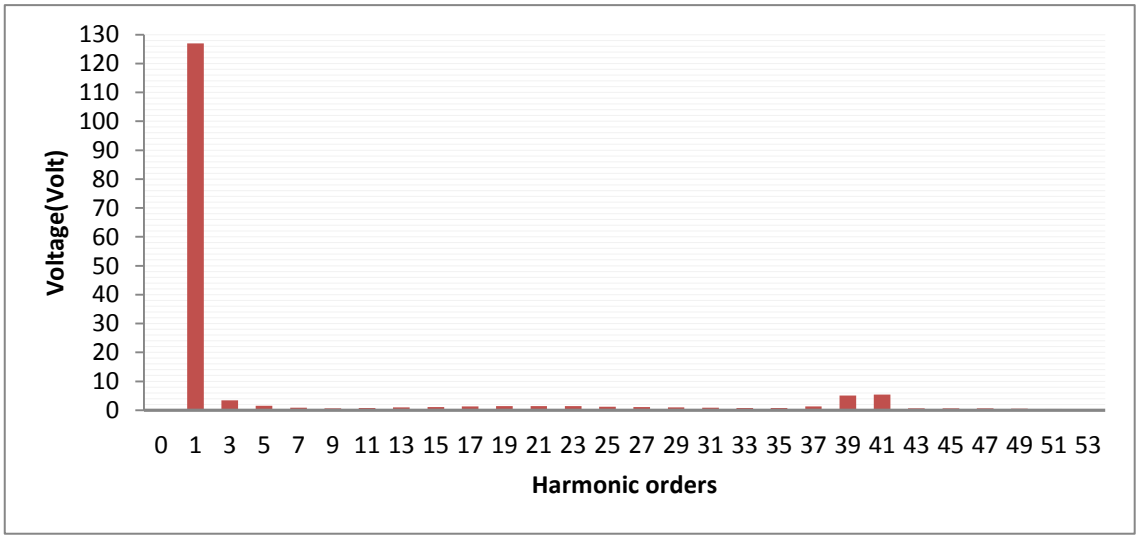


Fig. 3-16 The FFT of AC output voltage of H-bridge.

The amplitude of the lower orders harmonic and switching frequency of the FFT output voltage is listed below.

- The amplitude of 3rd harmonic is 3.67 volts (about 3% of fundamental)
- The amplitude of 5th harmonic is 2.27 volts (less than 2% of fundamental)
- The amplitude of 7 to 37 harmonic is 1.1 volts (less than 1% of fundamental)

- The amplitude 39^{th} and 41^{st} harmonics is 4.44 volts (about 3.5% of fundamental)

These lower orders harmonic amplitude can be eliminated by optimising the switching pattern in the control signal with no adding passive filter at the output. However the THD can be reduced to less than 2% if a passive filter is used at the load side.

In summary, the voltage ratio in this topology is between 0.5 to 8 only by controlling the value of M_f and M_a. THD can be reduced to 5% with no filter on the load side. So this BBLFI circuit with RSPWM controller has all advantages of the topology in section 3-2. RSPWM controller is not complicated as the control circuit used in section 3-2 (previous control topology). Then this controller can be a good solution for limitation of control circuit previous control topology. However, this topology still has other limitations of the circuit in section 3-2. These limitations are high value of $\Delta i/\Delta t$ in the inductor of the circuit and this topology is suitable for low power applications. The current is discontinues mode in the inductor of the circuit. This is the main reason that this topology is not recommended for high power applications. Chapter four introduces a new control circuit to solve these two limitations.

Chapter 4 Double Sinusoidal Pulse Width Modulation (IDSPWM) controller

4.1Introduction of DSPWM controller

The PWM and RSPWM controllers of BBLFI have a couple of limitations, which can be solved by changing the control system in BBLFI circuit. The $\Delta i/\Delta t$ in these controllers is very high in the inductor due to small values of the inductor. A higher value of $\Delta i/\Delta t$ will increase the switching losses. So these types of controllers are not practical for high power applications. There is a limitation to increase the value of inductor in BBLFI circuit. The higher the value of the inductor the more distorted the voltage waveform will be (higher THD). Also by increasing the switching frequency in the BBLFI circuit, the THD will increase.

The sinusoidal shaped output is formed through the multilevel action so that no filter is required. The only changeable parameters are the switching frequency and inductor. The solution for this case is the proposed Double Sinusoidal Pulse Width Modulation (DSPWM) controller. This controller can reduce the $\Delta i/\Delta t$ in the inductor of the BBLFI circuit at low frequency.

Fig 4-1 shows the logic circuit of DSPWM, the circuit includes two comparators, eXclusive OR (XOR) and invert gates. The inputs to this circuit are 2 sinusoidal waveforms at the fundamental frequency with 180-phase shift and a triangular carrier frequency waveform. The main reason in using this type of logic circuit is to have 'near zero crossing' pulses. These pulses can generate early steps at the output voltage. The pervious control signals (in Chapter 3) of BBLFI do not have such pulses. This could be one of the reasons of why the 3^{rd} and 5^{th} harmonic value are higher in these two controllers (PWM and RSPWM) of BBFLI.

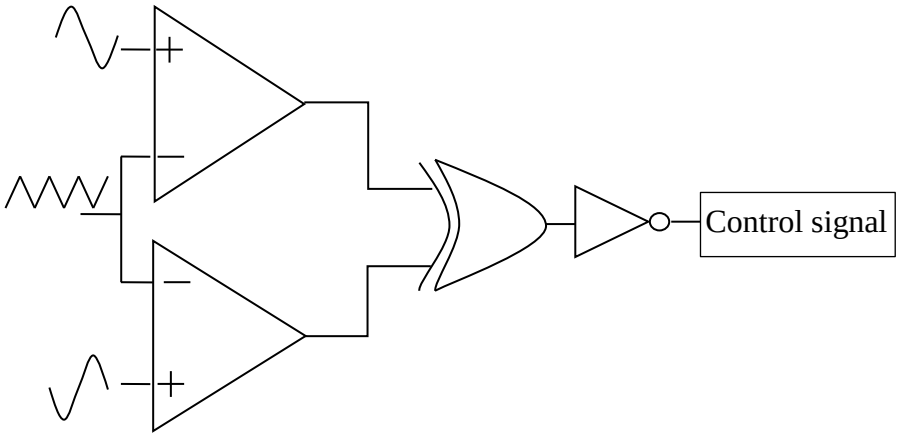


Fig. 4-1 Logic circuit of DSPWM

Fig.4-2 shows the process of generating the control signal of DSPWM for BBLFI. Also the 'near zero crossing' pulses in each half cycle is shown in this figure. These pulses can reduce the 3^{rd} and 5^{th} harmonics at the output voltage, which causes a reduction in the THD.

The BBLFI circuit can operate with larger values of inductance if the DSPWM control main switch of BBLFI. This controller causes the current in inductor to be in the continues mode. This continues current mode reduces the switching losses at the main switch of BBLFI. The higher power application can be used in this BBLFI circuit that has higher efficiency.

The control signal in Fig.4-2 shows the logic pulses (0 and 5 volt). The duty cycle of each pulse decreases until 5ms (¼ of the mains cycle). As a result of that the output voltage increases until 5ms. The duty cycle of the pulses increases from 5ms to 10ms (half cycle). The main switch on BBLFI circuit is operated by DSPWM control signal. The output voltage increases when the main switch is 'OFF' and the output voltage decrease when the main switch of BBLFI is 'ON'.

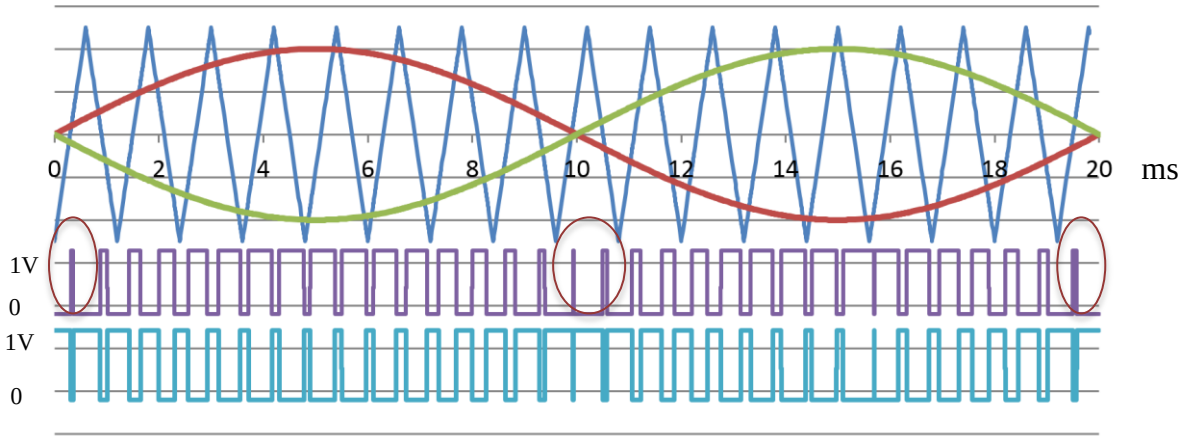


Fig. 4-2 Control signal of BBLFI

The frequency modulation ratio of the controller in this topology is assigned as M_f. M_f can be calculated from equation 4-1 where f_s and f_{out} are the carrier frequency and the fundamental frequency of the H-bridge inverter. The reason to use two carrier frequencies in this equation is because of using XOR gate. So the switching frequency of the main switch in BBLFI circuit is two times the carrier frequency.

$$M_f = \frac{2\ f_s}{f_{out}} \tag{4-1}$$

The main idea is to create a sinusoidaly modulated waveform through controlling the charging and discharging times of the inductor current and the capacitor voltage in the current source converter. The output voltage can also be selected by controlling the amplitude modulation ratio (M_a) Where M_a is the ratio between the amplitudes of the sinusoidal and triangular controller waveforms and can be expressed by the following equation:

$$\frac{2}{\sqrt{2}\,M_a} = \frac{V_{load}}{V_{Dc}} + 1 \tag{4-2}$$

Where V_{DC} and V_{load} are the input voltage and output voltage of BBLFI circuit.

In basic buck-boost converter the relation between the input and output voltages can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{D}{D-1} \quad (4\text{-}3)$$

Where 'D' is the switch duty-cycle. In the case of the BBLFI the output voltage of the buck-boost converter is sinusoidaly modulated. In this case a '√2' factor is used to express the maximum value of the sinusoidaly modulated waveform. The factor of '2' is mainly to express the full wave rectification of also the sinusoidaly modulated waveform (double the output frequency). Fig. 4-1 illustrates the logic generation of equation (4-2). The proposed BBLFI (fig. 4-3) circuit consists of 5 semiconductor switches (one of the buck-boost and four for the H-bridge inverter). The main losses associated with these switches are conduction losses and switching losses. The switching losses are in direct proportion to the operating switching frequency. Since only one switch is operating at 'relatively' high frequency (S), the switching losses are limited in this proposed configuration. The inverter switches (S_1-S_4) operate at the mains switching frequency (50/60 Hz) and therefore the switching losses are also limited.

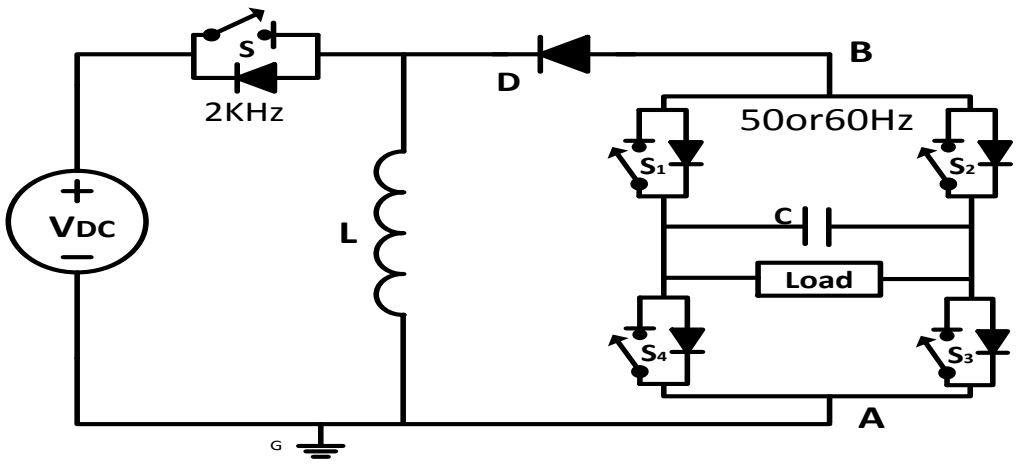


Fig. 4-3 the proposed BBLFI circuit

Conduction losses are very similar in other inverter topologies as the average 'ON' time in the inverter configurations is directly proportion to the desired output voltage. The

switching and conduction losses for the proposed BBLFI circuit are analysed in the section 4.1.1.

4.1.1 Switching losses**:**

The switching losses in the semiconductor switch (S) can be expressed by the following equation:

$$P_{sw} = \frac{1}{2}\, I_{on} \times V_{off} \times (t_{on} + t_{off}) \times f_s \quad (4\text{-}4)$$

$$P_{conductor\ loss\ in\ switch\ when\ is\ on} = (I_{on})^2 \times R_{on} \quad (4\text{-}5)$$

$$P_{conductor\ loss\ in\ switch\ when\ is\ off} = (V_{off})^2 \times G_{off} \quad (4\text{-}6)$$

Where:

t_{on}: Time for switching ON of MOSFET

t_{off}: Time for switching OFF of MOSFET

I_{on}: Average current in a switch when is on

V_{off}: The average voltage across the switch when is off

R_{on}: Resistance of the switch when is on

G_{off}: The conductance of switch when is off

$I_{switch\ when\ is\ off}$: Leakage current in switch when is off

Fig4-4 shows an example of MOSFET 44N50P, which details are from the data sheet.

MOSFET 44N50P:

Turn on delay time =Td (on) =28ns

Rise time=Tr =29ns

Turn off delay time = Td (off)=85ns

Fall time =Tf =27ns

VGs =20v , VDs =0.5 VDss RG =3 ohm's (external) ID = ID25

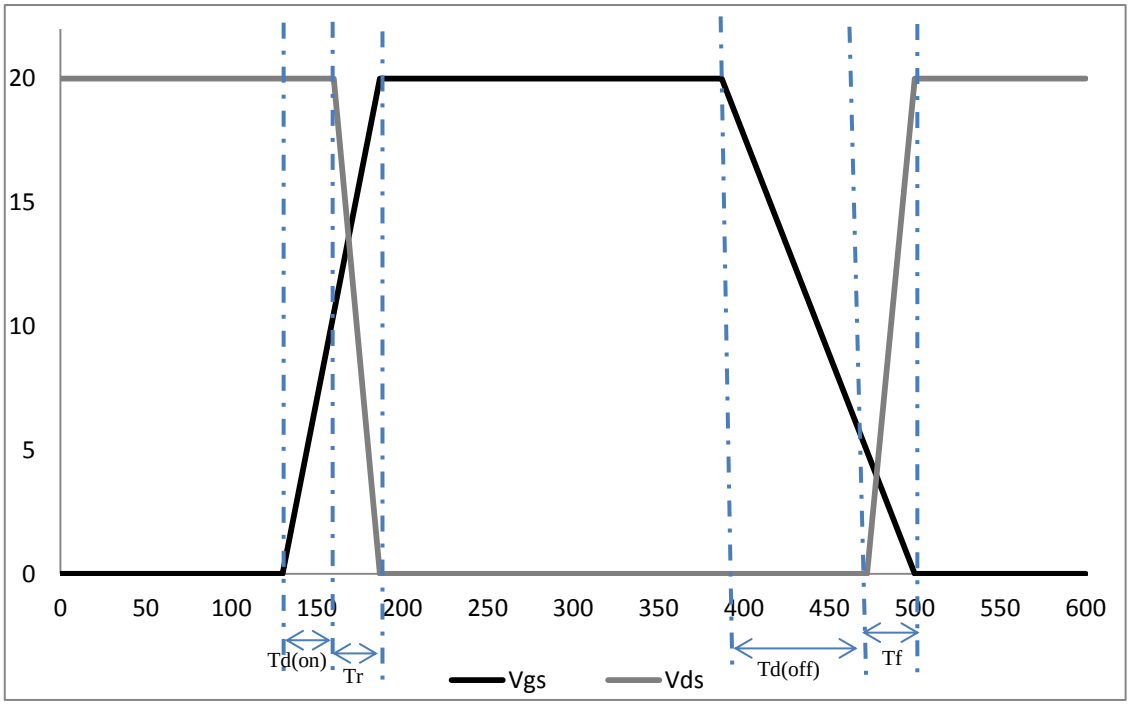


Fig. 4-4 the switching voltage gain and voltage drain of MOSFET 44N50P

4.1.2 Diode losses

The switching losses in a diode depend on the switching frequency and the reverse recovery times of the diode. Such losses are too small in comparison with the conduction losses and are neglected in this topology. The conduction losses depend on the forward slope resistance at maximum diode current and can be expressed as:

$$P_{conductor\ loss\ in\ diode} = (I_{on})^2 \times R_{on} \quad (4\text{-}7)$$

The DSPWM can also control the Boost-based Low Frequency Inverter (BLFI) in section.4.3 and Flyback-based Low Frequency Inverter (FLFI) in section.4.4. The DSPWM is designed to control the main switch of the buck/boost-based low frequency inverter.

4.2Buck/Boost-based Low Frequency Inverter controlled by DSPWM

The BBLFI circuit (Fig. 4-3) with DSPWM controller operates same as BBLFI with PWM and RSPWM controller. The differences of the DSPWM controller with other two controllers are output voltage with improved THD and higher efficiency.

The operation of the BBLFI circuit, shown in Fig.4-3, can be described as follows:

1. The BBLFI behaves as an integrated current source with full H-bridge inverter.

2. Varying the frequency and amplitude modulation ratios in S can control the output voltage of the BBLFI.

3. The output frequency of BBLFI can be controlled in the same way as conventional DC/AC inverters. This is achieved by selecting the appropriate the fundamental frequency.

4. V_{dc} used in the BBLFI can be increased if the output voltage is required to be stepped up or down in large steps. The buck/boost converter operates as a current source in the proposed configuration.

The circuit includes a DC voltage, a resistance (load) an inductor, a capacitor, a diode, a microcontroller (DSPWM pulse generator) and five MOSFETs. This circuit is simulated on MATLAB (for system modelling) and PSPICE (for component modelling). The PSpice simulation and the practical results are both presented in chapter 5 and chapter 6.

The value of the inductor and capacitor in this proposed circuit can be calculated by selecting an appropriate the frequency and amplitude modulation ratio (M_f & M_a) and acceptable rate of change of the inductor current (which is directly linked to the THD). M_a can also be expressed as the ratio between the load current and the DC current:

$$L = \frac{2V_{dc}}{2\times\Delta I_{L(Dc)}\times M_a\times f_s} \quad (4\text{-}8)$$

$$\frac{2}{\sqrt{2}\,M_a} = \frac{I_{in(Dc)}}{I_{Load}} + 1 \quad \textbf{(4-9)}$$

$$\Delta I_{L(Dc)} = \%\ of\ I_{in(Dc)} \quad (4\text{-}10)$$

Substituting (4-9 and 4-10) into (4-8):

$$L = \frac{\sqrt{2}\,V_{Dc}}{\%\times(2I_{load}-\sqrt{2}\,M_a I_{load})\times M_f \times f_{out}} \quad (4\text{-}11)$$

$$C = \frac{\sqrt{2}I_{load}\times M_a}{\Delta V_{out}\times(1-M_a)\times M_f \times f_{out}} \quad \textbf{(4-12)}$$

The derivation of Eqs.4-8, 4-11 and 4-12 are given in Appendix A.

$$I_{load} = \frac{V_{load}}{Z} \quad \textbf{(4-13)}$$

Z: load impedance.

ΔV_{out}: Ripple voltage across 'C'

$\Delta I_{in(Dc)}$: Ripple current in main switch BBLFI circuit (S)

f_{out}: Output Frequency of H-bridge

The THD of V_{out} can be calculated from the following equation 3-1. There is an example of a BBLFI circuit with DSPWM controller. This circuit is simulated in Pspice software with different value of inductance, different amplitude modulation ratio (M_a). There are 3 graphs, which show the voltage ratio, efficiency and THD of proposed circuit. The inductor assumes as ideal in the proposed circuit of this simulation example. The input voltage is 60 volts and the load is 20Ω in this simulation. Fig 4-5 shows the output voltage ratio function of M_a of BBLFI circuit with DSPWM controller with different inductors. The voltage ratio is about 19 where the inductance value is 80mH and M_a is 0.1. The voltage ratio decreases to 0.6 where the M_a is one. The BBLFI circuit operates as boost where the M_a is less than 0.85. The voltage ratio of these circuits is similar to the theoretical voltage ratio. The higher value of inductance causes the higher voltage

ratio in the BBLFI circuit. Charge and discharge energy is higher in bigger inductor so that is reason the higher value of inductance has a higher voltage ratio in BBLFI. The discharge energy in inductor has a higher level in the output voltage. However the higher voltage ratio in BBLFI circuit reduces efficiency in the circuit. The reason is more switching losses in the main switch on BBLFI circuit. The conduction losses and switching losses in this circuit are about 10% when the voltage ratio is about 19.

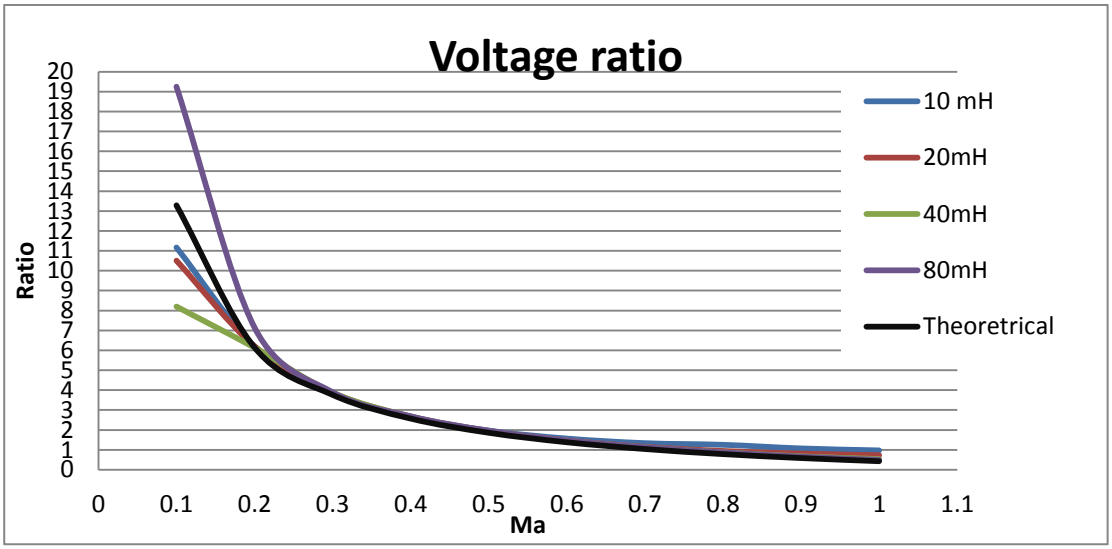


Fig. 4-5 Voltage ratio of different inductor of BBLFI in different M_a

Fig 4-6 shows the efficiency function of the amplitude modulation ratio of BBLFI with different value of inductance with 20Ω load. The input voltage in this circuit is 60 volts. The switching losses in this main switch on BBLFI circuit are less than 1% where the amplitude modulation ratio (M_a) is more than 0.3 in inductance 10mH, 20mH and 40mH. The switching losses in these circuits can be neglected where the M_a is higher than 0.3 in the BBLFI circuit.

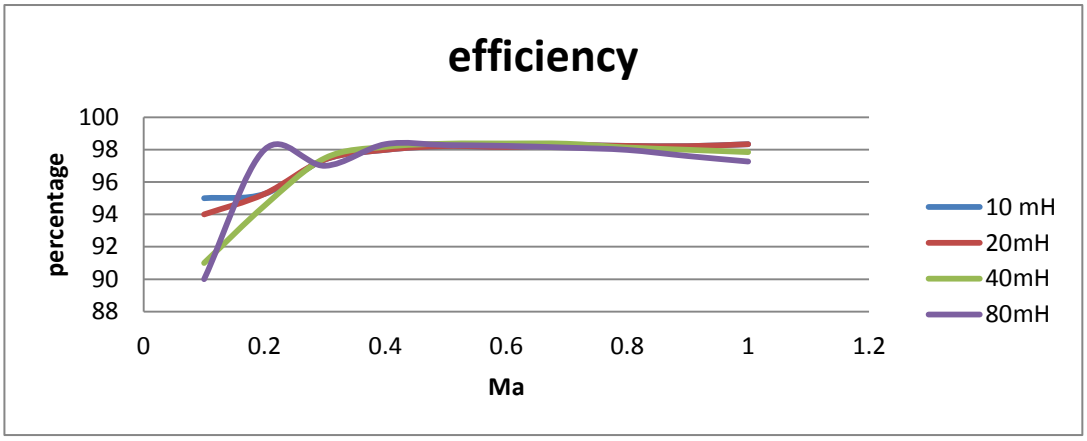


Fig. 4-6 Efficiency of different inductor of BBLFI in different Ma

Fig.4-7 shows the THD function of the amplitude modulation ratio at the output proposed circuit with different value of inductance. The current mode in inductor would be discontinuous if the THD is more than 30%. The current mode is discontinuous in 10mH inductor when the M_a is more than 0.55. Also the current mode in inductors 20mH and 40mH are discontinuous when the M_a is more than 0.7 and 0.9. The current mode is continuous in 80mH inductor when the M_a is 1. So If the current is a discontinuous mode in inductor the shape of output voltage is not close to sinusoidal waveform. The lowest THD is 10% of circuit with 40mH when the M_a is 0.6. However, the voltage ratio of the proposed circuit with 40mH is 1.5 when the M_a is 0.6 in fig. 4-5. So the voltage ratio or THD can be objective for this proposed circuit.

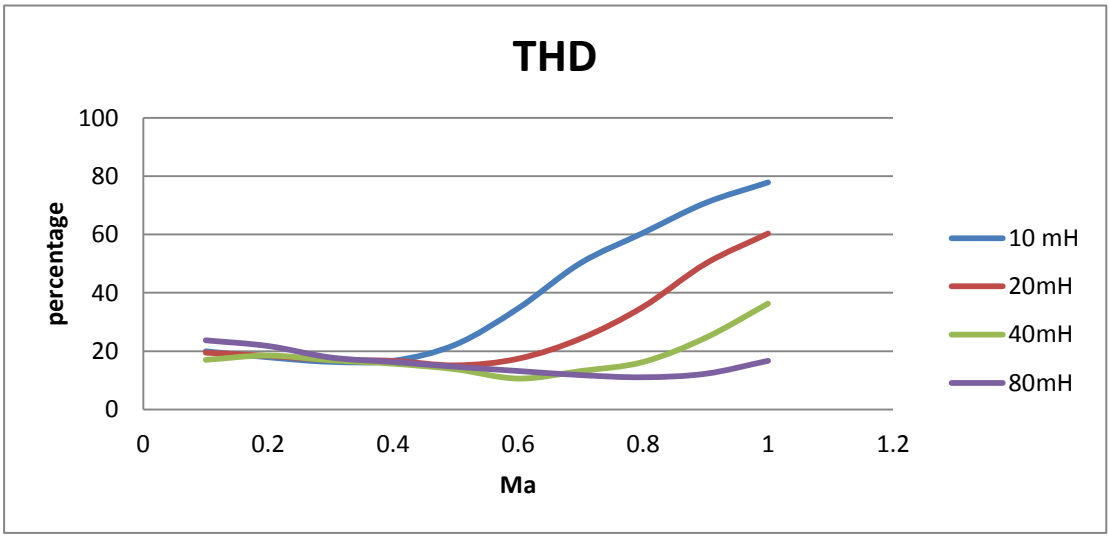


Fig. 4-7 THD of different inductor of BBLFI in different M_a

The proposed circuit can be designed with equations (4-8 to 4-12) to determine value of R, L and C in BBLFI circuit. The control signal can vary the output voltage by changing M_a and M_f in main switch of BBLFI circuit where no need to change passive components (R, L and C). THD can be reduced by an optimising switching pattern of control signal. There is a code of MATLAB which is written to minimise the lower order harmonics in BBLFI. This code analyses the output voltage to Discrete Fourier Transform (DFT), where the harmonics are determined as the number of samples. The next code reduces the lower order harmonics to minimum 20%, which causes to reduce THD to 6%. This code generates a new control signal to have less THD in output voltage. The programmed MATLAB code is explained in appendix B.

The switching losses for this topology are very small which is less than 1% for 2.5 kW power applications. These semiconductor-switching losses can be neglected at this stage. But the conductive losses can be less than 2%. These losses depend on the power application, which could be more or less. There is a simulation example (in chapter 5) of this topology in 2.5 kW power applications, which is designed for a photovoltaic to house consumer (residential application).

The photovoltaic voltage needs to step up with transformer or DC-to-DC boost converter. Then it needs to use a DC to AC inverter component. There are some limitations to this type of connection between photovoltaic to residential application, which are low efficiency, and poor THD. However, the proposed circuit can easily step up and invert DC to AC output voltage with high efficiency and lower THD. Also, this proposed topology can track the maximum power point by varying M_a and M_f in control signal when the sun radiation is changed. Also, there is an example of simulation of 2.5kW applications with 60-volt input DC source instead of photovoltaic cell in chapter5.

4.2.1 Design Example & Parameter calculation of BBLFI circuit

It is required to design a BBLFI with following specifications.

P_{load} =2500 W, V_{Dc}=60V, V_{load}= 250 V (rms)

In order to achieve the above specifications, the voltage ΔV_{out}, the current $\Delta I_{L\ (DC)}$ and the switching frequency of the buck/boost converter need to be set. These values are selected at:

ΔV_{out}= 25% of load voltage (the smaller the V_{out}, the larger capacitor value is used). $\Delta I_{in(Dc)}$= 50% of inductor current (the smaller the $\Delta I_{in\ (DC)}$, the larger inductor value is used). The selection of the switching frequency is a trade-off between the switching losses and the inductor & capacitor sizes. For a fair comparison between the proposed topology and other inverter topologies, the sizes of L and C are chosen to be the same. Therefore the switching frequency of the buck/boost converter is selected at 2 kHz, taking into consideration that the inductor current is continuous. The parameters R, L and C in this design example are: 25 Ω, 5.23mH and 55.7 μF. These values are calculated from equations 1, 2 and 3.

$$I_{Load(rms)} = \frac{P_{Load}}{V_{Load(rms)}} = \frac{2500}{250} = 10$$

$$R = \frac{V_{Load}}{I_{Load}} = \frac{2500}{10} = 25\Omega$$

$$\frac{2}{\sqrt{2}\,M_a} = \frac{V_{Load}}{V_{DC}} + 1 \Rightarrow M_a = 0.275$$

$$L = \frac{\sqrt{2}\,V_{Dc}}{\%\times(2I_{load}-\sqrt{2}\,M_a I_{load})\times M_f \times f_{out}} = \frac{\sqrt{2}\times 60}{0.5\times(20-3.88)\times 2000} = 5.23\text{mH}$$

$$C = \frac{\sqrt{2}I_{load}\times M_a}{\Delta V_{out}\times(1-M_a)\times M_f \times f_{out}} = \frac{14\times 0.33}{0.25\times 0.67\times 250\times 2000} = 55.7uF$$

These parameters will put on a simulation circuit in PSpice and Matlab software in the simulation part (section 5-1).

Additionally, the DSPWM controller can be applied for other type of current source such as boost-based and flyback-based low frequency inverter. The section 4.3 has more explanation about this proposed control signal for boost-based inverter.

4.3 Boost-based low frequency inverter controlled by DSPWM.

The proposed Boost-based Low Frequency Inverter (BLFI) is shown in Fig.4.8. It consists of a boost converter and an H-bridge inverter. The boost switch S_1 is controlled by a sinusoidal modulated DSPWM signal as shown in Fig.4.2. This control signal can be applied to BLFI circuit as well. The input DC voltage is formed too much close to AC output voltage by controlling main switch of boost inverter (S_1). The frequency of switch in this case is 2 kHz. User can choose the switching frequency of boost, which could be from 1 kHz to 5 kHz. The high switching frequency is not recommended because more switching losses. The switching frequency of H-bridge is same as fundamental frequency that is 50 Hz square wave with 48.5% duty cycle. The zero level in output voltage can reduce the amplitude of 3rd and 5th harmonics

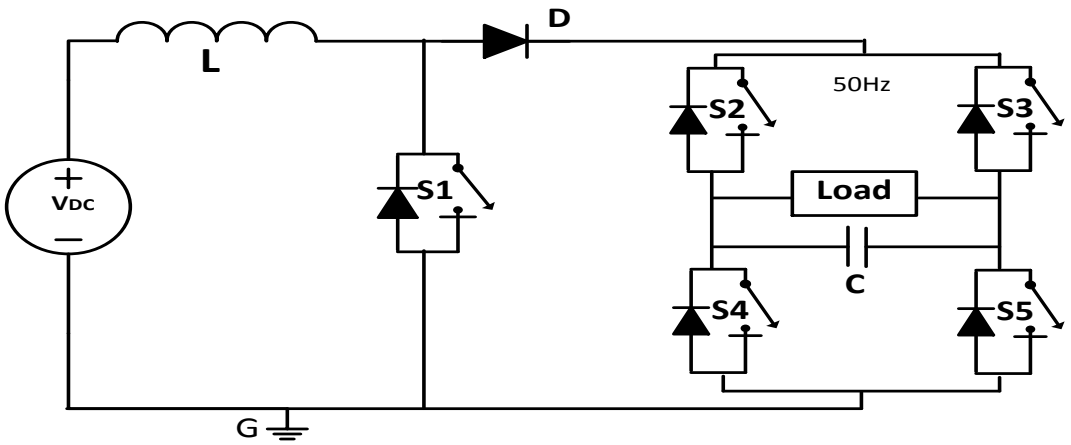


Fig. 4-8 proposed circuit of BLFI.

The value of the inductor and capacitor can be optimised by selecting an appropriate switching frequency (f_s) and acceptable rate of change of the inductor current (which is

directly linked to the THD). The amplitude modulation ratio can control the output voltage and the value of inductor and capacitor in proposed circuit.

$$\frac{2}{\sqrt{2}\,M_a} = \frac{V_{load}}{V_{Dc}} \qquad (4\text{-}14)$$

The M_a is controlling the output voltage that can be chosen by the voltage amplitude of the fundamental frequency over carrier frequency in controller system. Fig 4-9 shows the comparison output voltage ratio of the BLFI circuit with different value of inductor and theoretical in PSpice software results. The voltage ratio is decrease where the value of M_a increases. The maximum voltage ratio in this simulation circuit is about 12 and the minimum voltage ratio is 1.4, which shows the proposed circuit operates as boost DC to AC inverter.

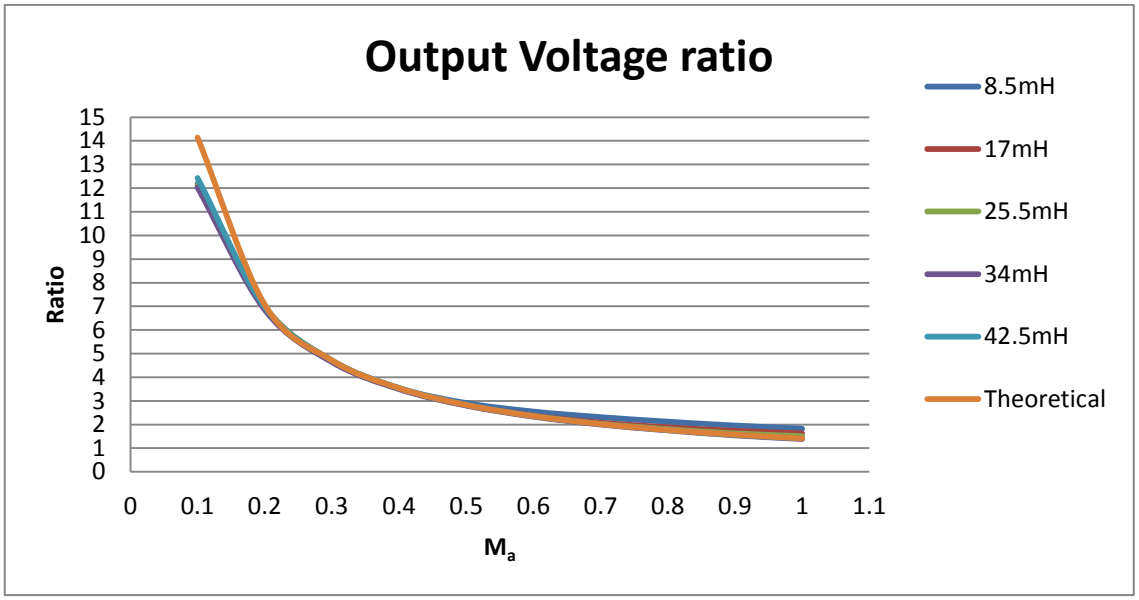


Fig. 4-9 Output voltage ratio function of amplitude of modulation ratio

The value of the inductor can be calculated from equation 4-15 that depends of Ma, switching frequency, input voltage and ΔI_L (ΔI_{In}). This proposed circuit is working as continuous mode in the inductor. So the minimum inductor in this equation is the highest value of ΔI_L in inductor (100%) of BLFI circuit. The minimum value of the capacitor is

applied where the maximum value of voltage ripple (ΔV_{output}) in output of H-bridge. The capacitor value can be calculated from equation 4-19.

$$L = \frac{2V_{dc}}{\Delta I_{in(Dc)} \times M_a \times f_s} \quad (4\text{-}15)$$

M_a can also be expressed as the ratio between the load current and the DC current:

$$M_a = \frac{\sqrt{2}\, I_{load(rms)}}{I_{in(dc)}} \quad (4\text{-}16)$$

$$\Delta I_{in(Dc)} = \%\ of\ I_{in(Dc)} \quad (4\text{-}17)$$

Substituting (equation 4-16, equation4-17) into (equation 4-15):

$$L = \frac{2V_{dc}}{\% \times \sqrt{2} I_{load} \times f_s} \quad (4\text{-}18)$$

$$C = \frac{\sqrt{2} \times I_{load} M_a}{f_s \Delta V_{out}} \quad (4\text{-}19)$$

The derivation of Eqs.14-14, 14-15 and 14-18 are given in Appendix A.

I_{load}: Current of the load

ΔV_{out}: ripple voltage across 'C'

$\Delta I_{in(Dc)}$: ripple current in S_1 (current in inductance)

f_s: Frequency of switch (S_1)

The values of inductor and capacitor have a direct effect on total harmonic distortion, voltage ratio and efficiency BLFI circuit. Fig 4-10 shows the THD of BLFI circuit function of M_a, which is simulated in PSpice software. The current mode in inductor becomes discontinues where the THD is more than 30%. So this graph shows the current mode is discontinuous in 8.5mH, 17mH and 25.5mH. However, the THD of BLFI circuit has a direct relationship with load, capacitor, switching frequency, inductor and M_a. There will be more discussion about THD in the simulation section (chapter5).

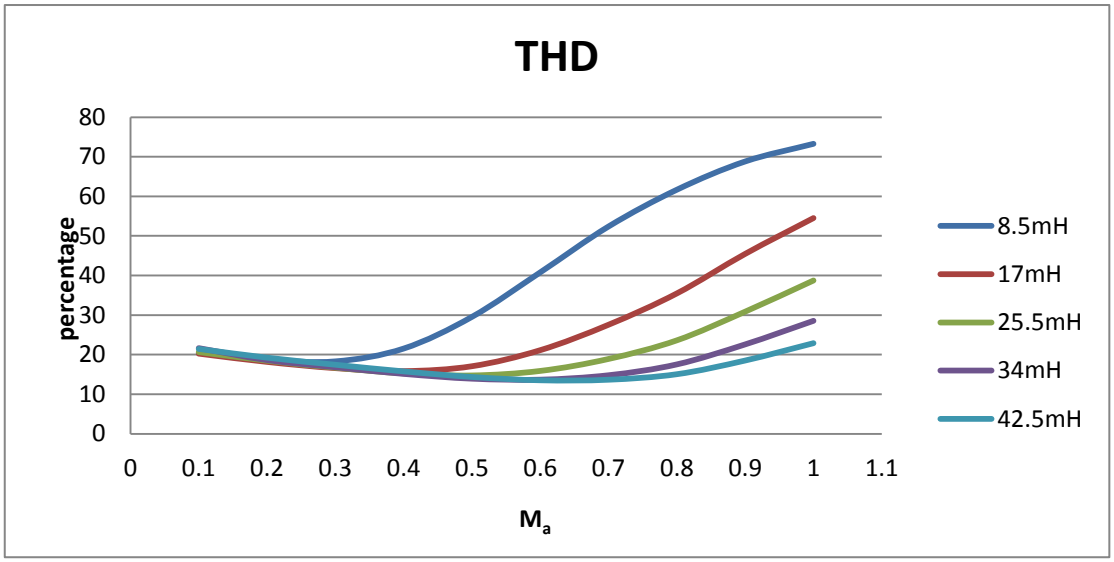


Fig. 4-10 Total harmonic distortion of BLFI circuit with different value of inductor.

There is a design example of the proposed circuit for 2500W for connecting to photovoltaic cell in section 4.3.1.

4.3.1.1 Design Example and Parameter calculation for BLFI circuit

It is required to design a BLFI with following specifications.

P_{load} =2500 W, V_{Dc}=60V, V_{load}= 250 V (rms)

In order to achieve the above specifications, the voltageΔV_{out}, the current $\Delta I_{in\,(Dc)}$ And the switching frequency of the boost converter needs to be set. These values are selected at:

ΔV_{out}= 25% of load voltage (the smaller the V_{out} , the larger capacitor value is used).

$\Delta I_{in(Dc)}$= 50% of inductor current (the smaller the$\Delta I_{in\,(Dc)}$, the larger inductor value is used).

The selection of the switching frequency is a trade-off between the switching losses and the inductor & capacitor sizes. Therefore the switching frequency of the boost converter is selected at 2 kHz, taking into consideration that the inductor current is continuous.

The parameters R, L and C in this design example are: 25 Ω, 8.5mH and 27.2μF. These values are calculated from equations 1, 2 and 3.

$$I_{Load(rms)} = \frac{P_{Load}}{V_{Load(rms)}} = \frac{2500}{250} = 10$$

$$R = \frac{V_{Load}}{I_{Load}} = \frac{2500}{10} = 25\Omega$$

$$M_a = \frac{2\ V_{Dc}}{\sqrt{2}\,V_{load}} = \frac{2\times60}{\sqrt{2}\times250} = 0.34$$

$$L = \frac{2V_{dc}}{0.5\times\sqrt{2}I_{load}\times f_s} = \frac{2\times60}{0.5\times\sqrt{2}\times10\times2000} = 8.5mH$$

$$C = \frac{\sqrt{2}\times I_{load}\times M_a}{\Delta V_{out}\times f_s} = \frac{14.14\times0.34}{0.25\times250\times2000} = 38.5uF$$

The power losses of switches and passive components depend on the load current and voltage across of each component. The switching losses and diode switching losses is not more than 1% in this design example that could be neglected at this stage. The power losses of the capacitor and inductor is not too much in this case which can be assumed ideal for simulation part, but the total power losses in practical is about 2% to 15% which depends on the current in the component.

THD can be optimised by DFT the code that was explained in section 4.2. This code can reduce the amplitude of lower order harmonic by controlling width of control signal. So this programmed code can be applied to other topology to minimised lower order harmonic by varying the width of switching pattern. There are more details of the DFT method in section 4.5. Also, there is program code how to reduce THD of this design example in appendix B.

This proposed BLFI circuit has potential to use as DC to AC inverter for high power application, especially renewable energy, which is not reliable output voltage in comparison to other energy sources. This proposed circuit needs to have more future work for 3 phase power applications. There is a limitation of this proposed BLFI circuit for high power application, which is the size of the inductor. Inductor in BLFI circuit to have higher power applications can replace a transformer. So a boost converter becomes flyback converter.

4.4 Flyback-based low frequency inverter controlled by DSPWM

The inductor of the BLFI replaces to a transformer in the circuit, and then the DSPWM control signal is applied to the main switch. The BLFI circuit becomes a Flyback-based Low Frequency Inverter (FLFI), which is controlled by DSPWM. This proposed circuit could be applied for high power application with higher efficiency in comparison to previous topologies. This topology inverts the DC voltage to AC output voltage by controlling switch, which is connected in series with primary winding of the transformer and DC voltage source. The DSPWM control signal is applied only on one switch in FLFI and DC voltage is formed DC input in order to closed-sinusoidal waveform in output voltage by connecting to the H-bridge inverter. The H-bridge inverter frequency is 50 or 60 Hz. Fig4-11 shows the proposed circuit with 5 switches. The main switch on FLFI circuit operates at 2 kHz frequency and other 4 switches operate 50 Hz and 48.5% duty cycle to reduce the amplitude of lower order harmonics. The THD of this proposed circuit could be optimised by programmed code to eliminate amplitude of lower order harmonics. This programmed code operates same as previous programme code, which is explained in appendix B.

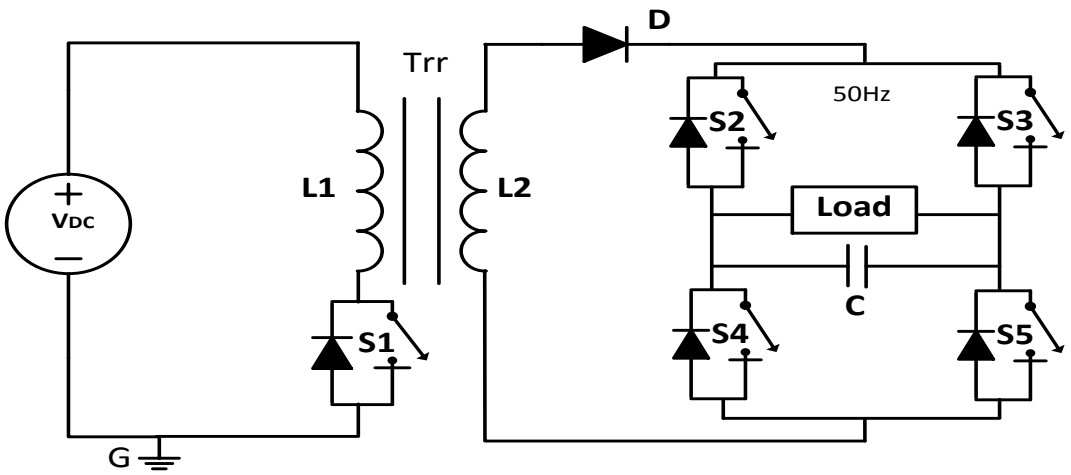


Fig. 4-11 Proposed flyback-based low frequency inverter circuit

The DSPWM control signal is applied to main switch (S_1) of proposed circuit. This control signal can control rms output voltage and THD by varying M_a and M_f in switch S_1. The THD can reduce to less than 8 %, but the output voltage ratio will be more or less. So the THD and voltage ratio can be chosen by the user and to choose these values, which are more important for the application. The value of the inductor and capacitor can be optimised by selecting an appropriate amplitude and frequency modulation ratio of DSPWM control signal in main switch S_1. Also, it is an acceptable rate to change the inductor current (which is directly linked to the THD) before the discontinuous current mode. The voltage ratio of this proposed circuit depends on M_a and the transformer ratio (Trr). The equation 4-20 determines the voltage ratio of FLFI that is can be controlled by varying M_a.

$$\frac{2}{\sqrt{2}\,M_a} + (T_{rr} - 1) = \frac{V_{load}}{V_{Dc}} \qquad (4\text{-}20)$$

The passive component (inductor) size is smaller at the BLFI circuit in comparison with FLFI by replacing transformer to inductor in BLFI. So the size of transformer in FLFI is smaller than the inductor in comparison in previous topologies at same output voltage. The reason is that the inductor becomes saturated in BBLFI and BLFI circuit. Then it requires having a bigger size of inductor's core in BBLFI and BLFI circuit. So bigger size of the inductor's core does not have saturation. The bigger size of inductor makes some limitation for the size of these two topologies. However, the transformer can be a good solution for this limitation. Also the transformer ratio can help proposed circuit to have higher voltage ratio and lower THD with higher value of M_a. The value of primary winding (L_1) and secondary winding (L_2) can be determined from equation 4-21 and 4-22.

$$L_2 = \frac{2V_{dc}\times(T_{rr}-1)}{\Delta I_{L2}\times M_a \times f_s} \qquad (4\text{-}21)$$

$$L_1 = L_2 \times \frac{1}{T_{rr}{}^2} \quad (4\text{-}22)$$

M_a and transformer ratio (T_{rr}) can also be expressed as the ratio between the load voltage and the DC voltage source.

The capacitor value of proposed circuit can be determined from equation 4-19.

T_{rr}: Transformer ratio

I_{load}: Current of the load

ΔV_{out}: ripple voltage across 'C'

ΔI_{L2}: Ripple current in L_2 (current in inductance of secondary winding)

f_s: Frequency of switch (S_1)

The section 4.4.1 is design example of flyback-based low frequency inverter, which the application is the same as previous design examples in section 4.2.1 and section 4.3.1.

4.4.1 Design Example and Parameter calculation for FLFI circuit

It is required to design a FLFI with following specifications.

P_{load} =2500 W, V_{Dc}=60V, V_{load}= 250 V (rms)

The transformer ratio is 2 in this case.

In order to achieve the above specifications, the voltage ripple ΔV_{out}, the current ripple ΔI_{L2} and the switching frequency of the flyback converter need to be set. These values are selected at:

ΔV_{out}= 25% of load voltage (the smaller the V_{out} , the larger capacitor value is used).

ΔI_{L2}= 50% of inductor current (the smaller the ΔI_{L2}, the larger inductor value is used).

The transformer ratio is 2 then the $\Delta I_{L2} = 2 \times 50\% = 100\%$. So the size of premier inductor is smaller than the size of the inductor in comparison to BLFI circuit.

The selection of the switching frequency is a trade-off between the switching losses and the inductor & capacitor sizes. For a fair comparison between the proposed topology

and other inverter topologies, the sizes of L and C are chosen to be the same. Therefore the switching frequency of the flyback converter is selected at 2 kHz, taking into consideration that the primary and secondary inductor current is continuous.

The parameters R, L_1, L_2 and C in this design example are: 25Ω, 4.75mH, 19mH and 3.923 μF. These values are calculated from equations 4-19, 4-21 and 4-22.

$$I_{Load(rms)} = \frac{P_{Load}}{V_{Load(rms)}} = \frac{2500}{250} = 10$$

$$R = \frac{V_{Load}}{I_{Load}} = \frac{2500}{10} = 25\Omega$$

$$M_a = \frac{2\ V_{Dc}}{\sqrt{2}\,(V_{load} - V_{in}(T_{rr} - 1))} = \frac{2\times 60}{\sqrt{2}\times(250-60)} = 0.4465$$

$$L_2 = \frac{2V_{dc}\times(T_{rr}-1)}{\Delta I_{L2}\times M_a \times f_s} = \frac{2\times 60}{0.5\times\sqrt{2}\times 10\times 0.4465\times 2000} = 19mH$$

$$L_1 = L_2 \times \frac{1}{{T_{rr}}^2} = 19 \times \frac{1}{2^2} = 4.75mH$$

$$C = \frac{\sqrt{2} I_{load}\times M_a}{\Delta V_{out}\times f_s} = \frac{\sqrt{2}\times 10\times 0.4465}{0.25\times 250\times 2000} = 50.5uF$$

The switching losses of main switch S_1 in FLFI circuit can be neglected in this power application, which the switching losses is not more than 1% of total input power. The transformer is assumed as an ideal transformer in this design example. However, the transformer loss in simulation and practical is about 3%. The conductivity losses of switches and diodes in FLFI circuit for this power application are about 2% of total input power. The capacitor is assumed as the ideal component for this design example and simulation part. However the power losses in transformer and switches in practical implement is about 9% of total input power. THD can be optimised by DFT the code that was explained in section 4.3. This code can reduce the amplitude of lower order harmonic by controlling width of control pulse.

There are simulation results for these 3 different proposed circuits in chapter 5 and also there is a comparison between these topologies. Also, there is practical to implement in chapter 6, which shows the different between these topologies.

4.4.2 Summarised DSPWM control methodology

The DSPWM control signal can be applied for different type of current source such as BBLFI, BLFI and FLFI circuit. Each circuit has some advantages and limitation, which depends on power application, power supply and switching frequency. In general, these proposed circuits have high efficiency and low THD in comparison to other topologies. The BBLFI and BLFI circuit has limitation on size of inductor's core, which can be solved by replacing the inductor with transformer at FLFI circuit. The THD of these proposed circuits can be about 5% of the optimising width pulse of DSPWM control signal. The filter can reduce THD to less than 2% if the filter is connected to a load. The amplitude of lower order harmonics can be eliminated by optimising switching pattern by DFT method. The chapter 5 is simulated design examples of these proposed circuits in Simulink and PSpice softwares. Also, there are more comparison results of these proposed circuits in chapter 5.

4.5 DFT method

The Discrete Fourier Transform (DFT) method is applied to the output voltage or current of BBLFI, BLFI or FLFY circuits. So DFT methods find the amplitude of each harmonic order from the equation;

$H_k = \sum_{n=0}^{N-1} y_n \left(e^{-\frac{j2\pi kn}{N}} \right)$

Value of the signal at time $y_n = \frac{1}{N} \sum_{n=0}^{N-1} H_k \left(e^{\frac{j2\pi kn}{N}} \right)$

Where:

H_k = Harmonic order amplitude frequency k in the signal

y_n = Value of the signal at time n

N= number of time samples

n = current sample (from 0...N-1)

k = current frequency (from 0… N-1 Hertz)

The amplitude of H_k can be zero for all lower harmonic orders from both sides of DFT. For example 3rd and 5th harmonics can be cancelled from H_{k3}, H_{k5}, H_{kN-5} and H_{kN-3}. This DFT method can be programmed in MATLAB or other programmed softwares. The appendix B shows the programmed DFT method in MATLAB for this thesis. This DFT programmed is applied for different topologies in chapter 5.

Chapter 5 Simulation

5.1Simulation of current source

The circuit is simulated by using the evaluated R, L, C and f_s in PSpice software. The circuit of a current source-based low frequency inverter is simulated in PSpice and MATLAB software which includes two main parts. The first part is the power circuit and the second part is the control circuit of the main current source switch S_1. That produces DSPWM signals to control S_1. The output rms voltage of this circuit is 250V and the output frequency is 50Hz.

The frequency of S_1 is controlled and as a result of that the voltage level at the input of the H-Bridge (Voltage at point A) is also controlled. The amplitude of V_a is controlled through the control of M_a (Amplitude modulation ratio of the control circuit). They are inversely proportion to each other due to the final inverting stage of the control circuit in design examples of chapter 4. The value of M_a, M_f, L, C and R in the simulation are chosen from design examples in chapter 4 for BBLFI, BLFI and FLFI circuits.

The magnitude of the voltage ripple of V_A can also be controlled through the selections M_f (Frequency modulation ratio of S_1). The larger M_f causes to have the smaller ripple voltage at V_a. Hence the smaller the THD, which imply is a compromise between M_f and THD. In this part emphasis on low M_f is the main task. Also a larger M_f Results in a smaller L and C in the circuit. The number of up and down steps of V_a depends on M_f. However, the M_a of DSPWM controls the output voltage ratio and THD in load. The pulse width of control signal for each step can have direct effects on output voltage and THD. So the pulse width can be chosen by programmed code, which optimises switching pattern to minimise the amplitude of low order harmonics.

The simulation circuits are built in two different softwares with the same parameters of design examples and compare the results of these two softwares. Also the optimised switching pattern of DSPWM control signal is applied in PsPice and MATLAB

simulation circuits. The discussion of the results of different circuit can help to understand the advantages and limitation of these proposed circuits in this chapter.

5.2Simulation of Buck/Boost-based Low Frequency Inverter controlled by DSPWM

The BBLFI circuit is simulated in two different softwares PSpice and Simulink (MATLAB). The output results of these two softwares are 98% the same. The value of components is chosen from design example of section 4.2.1. Also the frequency and amplitude modulation ratio (M_f and M_a) of the main switch of the circuit is chosen from that design example.

This circuit is first simulated in Simulink software with the same value of inductance, capacitor, resitance, same input voltage, same amplitude and frequency modulation ratio (M_a & M_f) in section 4.2.1.

5.2.1 Simulation of BBLFI circuit

The proposed circuit is simulated at both PsPice software and MATLAB software to compare simulation results in the next sections. The first simulation circuit is in Simulink and the second simulation circuit is in PsPice software. The last part is to optimise output voltage to optimise low order harmonic in output voltage.

5.2.1.1Simulink MATLAB Simulation circuit

Fig.5-1 shows the simulation of BBLFI circuit in Simulink which includes two main parts control signal circuit and power circuit. The control signal includes two AC voltage generators; these two AC generators operate in the 180 phase shift. The amplitude of these two AC generator is 1.375V. This amplitude voltage is chosen by multiplying M_a to the amplitude of carrier frequency, which is 5 volts for this example. The M_a is chosen from design example which is 0.275 in section 4.2.1. Also, this control signal includes two comparators to compare between amplitude of fundemental frequency and amplitude of carrier frequency and add two outputs of comparators together to make

control signal. The control signal needs to inverse at this point and to gain control signal to 12volt for driving main switch on BBLFI circuit. This control circuit connects to S_1 (MOSFET) in the power circuit. The power circuit includes DC voltage source where the voltage is 60volt. The inductance value of BBLFI circuit is 5.23mH and capacitance value for this circuit is 55.7µF. The load is resistance which the value is 25Ω and 250volt. This load connects to H-bridge as an inverter and a capacitor to reduce voltage ripple at output voltage. The switching frequency of H-bridge switches (MOSFET) is 50Hz and 49% duty cycle. The 49% duty cycle can reduce the amplitude of low order harmonics at the output voltage.

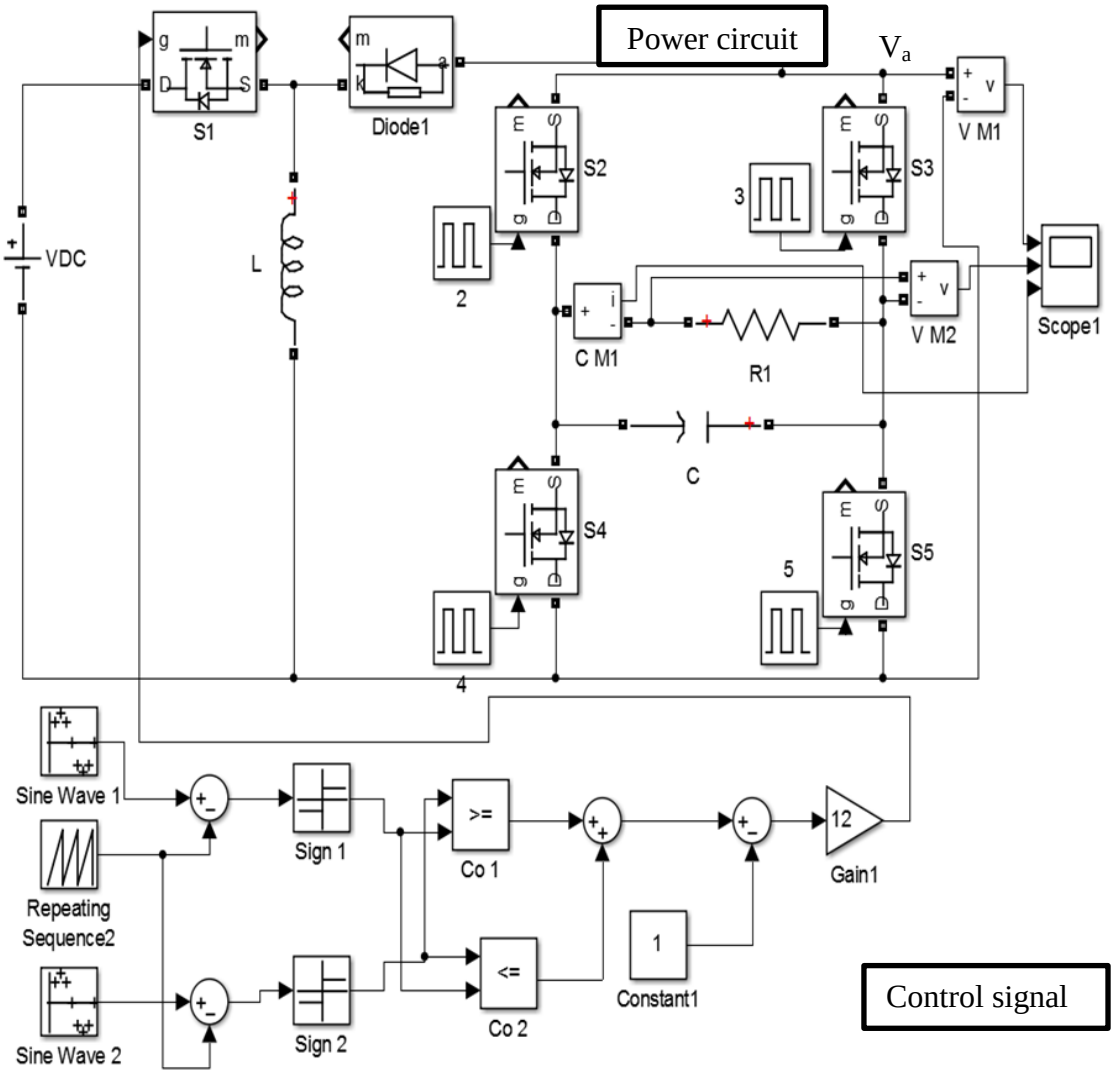


Fig. 5-1 simulation of BBLFI circuit in Simulink MATLAB

5.2.1.2 Simulation results of BBLFI in Simulink

Fig 5-2.a shows voltage across H-bridge (V_a). The voltage across of H-bridge is the output DC volt of BBLFI circuit. This voltage has zero, stepping up and down levels, which are caused by operation of DSPWM control signal in S_1. The peak value is 400 volts with 25% voltage ripple. Fig5-2.b shows the output voltage across of load which is caused from inverting of V_a in H-bridge inverter. The rms output voltage is 242 volts as load requested. Fig5-3.c shows the current of the load which rms value of current is 9.68A. So the total power load for this design example is 2342.5 W. This power can be increased 2500W by reducing 3% of the M_a in DSPWM control signal.

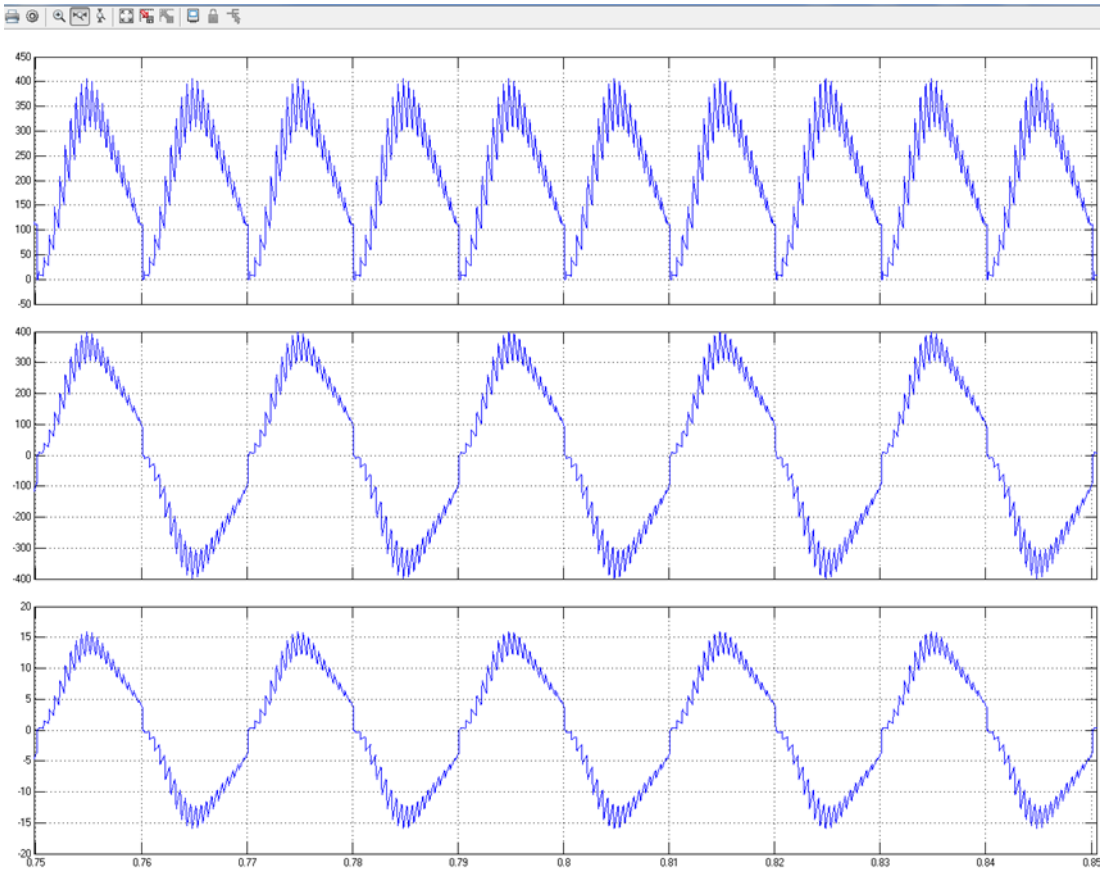


Fig. 5-2 Simulink results of BBLFI circuit a)Voltage across of H-bridge, b) Output voltage, c)current of load

Fig.5-3 shows the FFT output voltage of BBLFI circuit. The THD for this case is 11.61%. The highest amplitude harmonic orders are 39th and 3rd harmonics which are

about 6% of fundamental value voltage. The amplitude fundamental value of the output voltage is 340.3 volts.

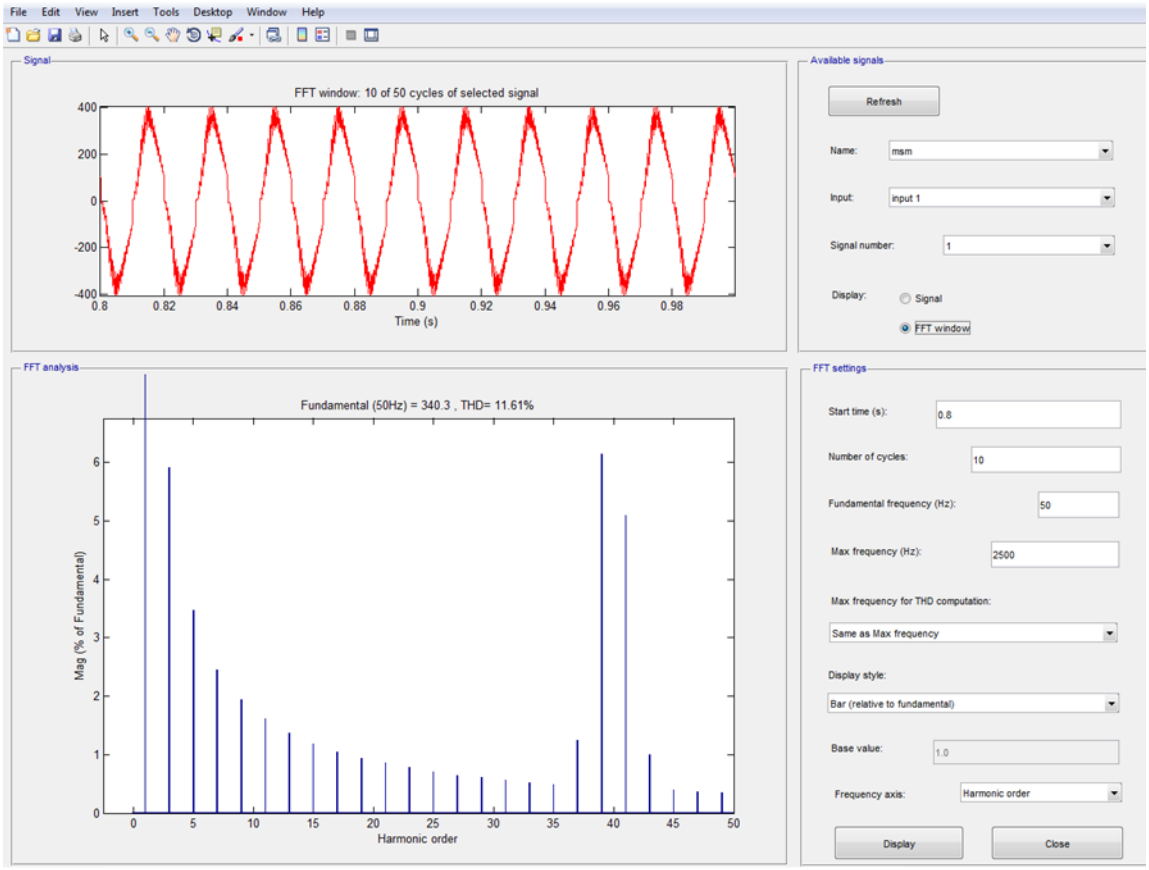


Fig. 5-3 Fast Fourier transform analysis of BBLFI output voltage

The section 5.2.1.3 explains the PSpice simulation of same circuits in this section. The section 5.2.2 is a comparison between results of these two simulation results.

5.2.1.3 PSpice simulation circuit of BBLFI

The parameter values of PSpice simulation circuit are chosen same value of Simulink simulation section 5.2.1.1. This simulation circuit includes 2 main parts control signal circuit and power circuit. The circuit of Simulink and PSpice simulations are exactly the same. The reason for the same simulation circuit is to compare theoretical results with two different simulation circuit. Fig 5-4 shows the PSpice simulation circuit on the BBLFI circuit with 60 volt DC input and 250Volt output with 2500W load.

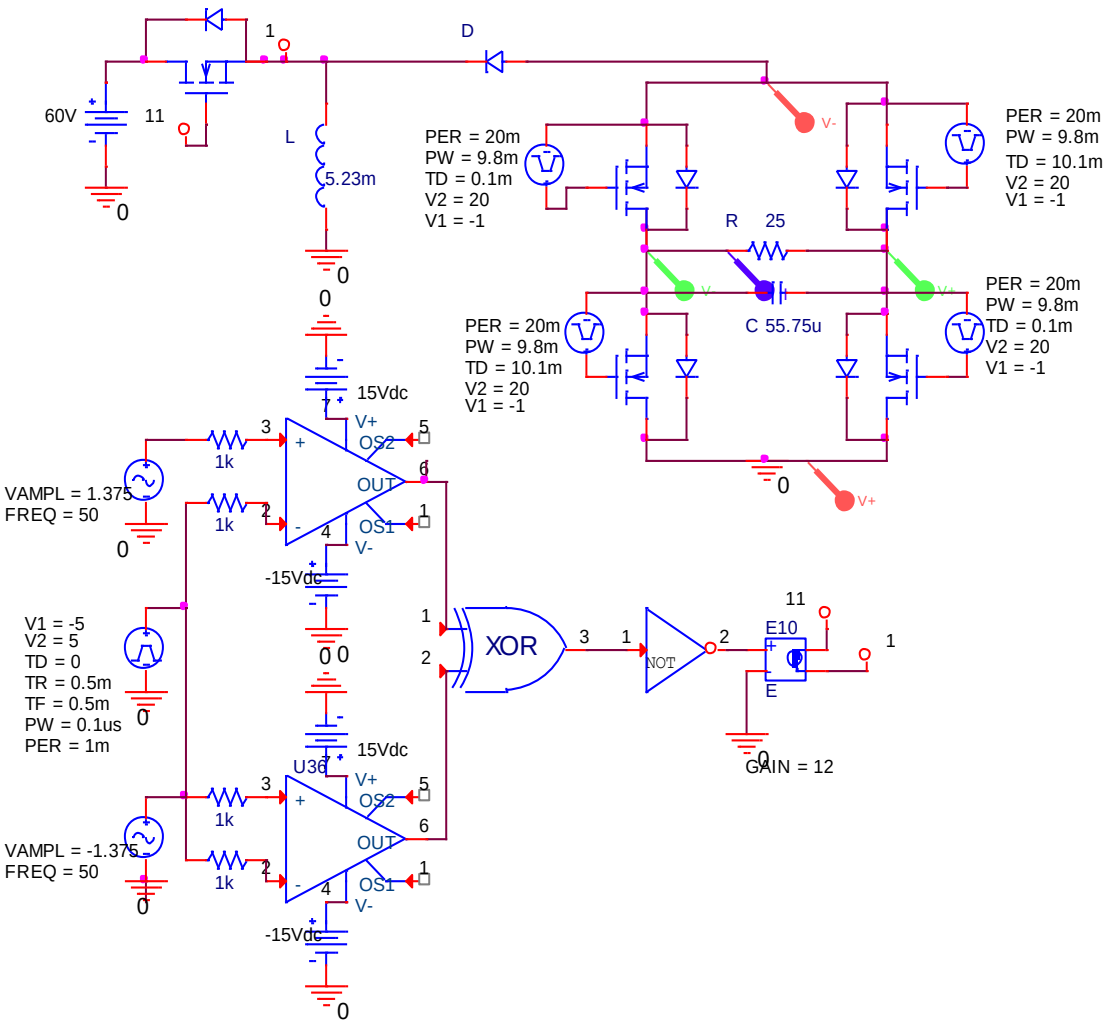


Fig. 5-4 PSpice simulation of proposed BBLFI circuit with DSPWM

5.2.1.4 PSpice results of BBLFI circuit

Fig.5-5 shows the control signal, the voltage across of H-bridge, output voltage and current in the load. These results are similar to the results of the Simulink simulation in section 5.2.1.2. The rms output voltage for this case is 246 volts and rms current is 9.8A. So the output power is 2410.8W which is a 3.5 % difference from the calculation. This deference is from voltage drop in switches and diode of proposed circuit. The resistance of each MOSFET is 0.14Ω and current at each switch at H-bridge is 10A. Also the average current in main switch on BBLFI circuit is about 40A. The switching losses of these MOSFETs are too low which is less than 1% of total input power.

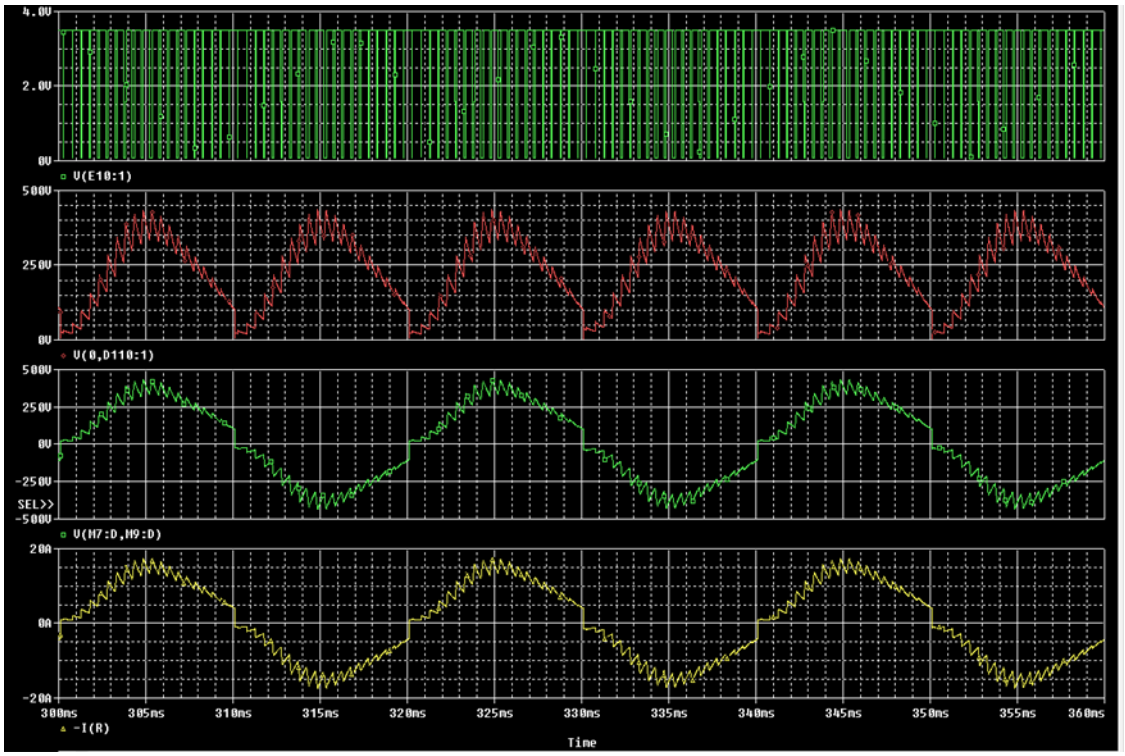


Fig. 5-5 PSpice results of BBLFI circuit a) Control signal, b) Voltage across of H-bridge, c) Output voltage, d) Current of the load

The average input power for this circuit is about 2650W, which the efficiency of the BBLFI simulation circuit is 91%. The most loss is from conductive losses of the switches which is about 280W. This loss can be reduced by adding parallel switch in main switch of BBLFI circuit. The THD of the output voltage is 11.83% for this case. Fig5-6 shows the FFT of output voltage of proposed circuit. The amplitudes of 3^{rd} and 5^{th} harmonics are 19 volts and 17volts which are about 5.5% and 5% of the output fundamental amplitude. The switching frequency of proposed circuit is 2 kHz so the 39^{th} and 41^{st} harmonics order are about 6% of fundamental value in this circuit. The lower order harmonic can be minimised by optimising switching pattern which section 5.2.3 is explained optimised output voltage of the same circuit with different control signal.

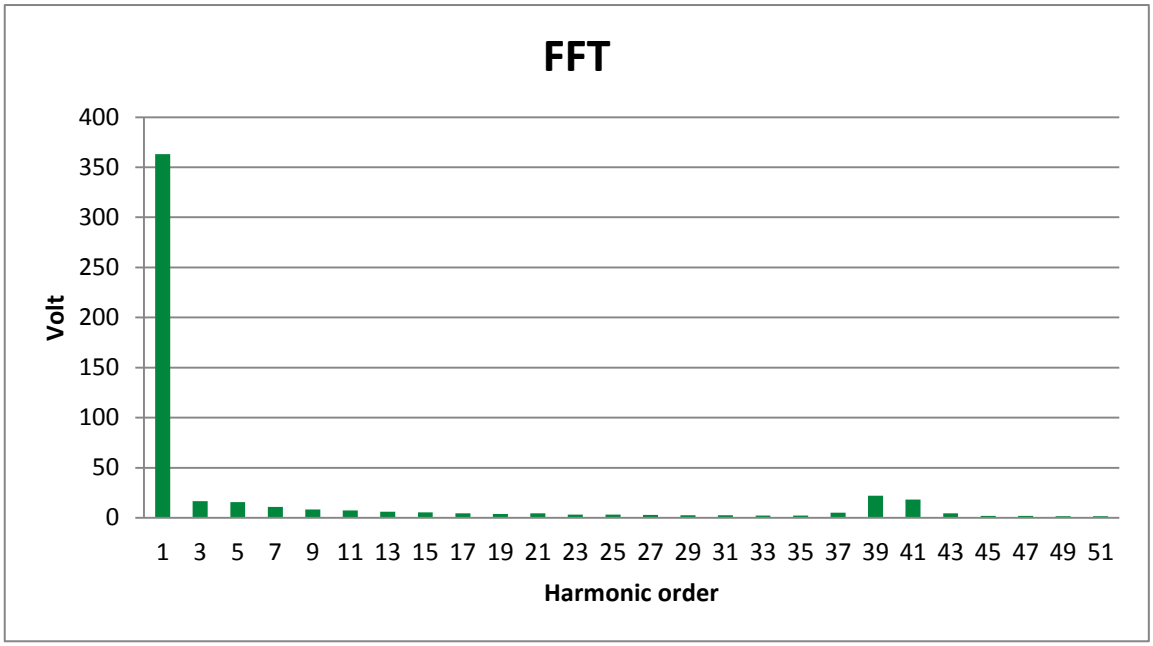


Fig. 5-6 Fast Fourier transform analysis of BBLFI output voltage in PSpice

5.2.2 Discussion of comparison results of two softwares in BBLFI circuit.

The results of Simulink and PSpice almost are the same which can be compared with theoretical results in table 5-1. This table shows the comparison results from these two softwares. The comparisons are between voltage ratio, efficiency, THD and amplitude of lower order harmonics.

Table 5.1 the comparison between results of Simulink and PSpice softwares with theoretical results from design example.

Software	Input voltage	Output voltage	Input power	Output power	Voltage ratio	Efficiency %	THD %
Simulink	60	241.98	2603W	2342.7W	4.033	90%	11.61
PSpice	60	246	2650W	2411.5W	4.1	91%	11.83
Theoretical	60	250	2500W	2500W	4.166	100%	12.2%

This table shows the simulation results and theoretical results almost the same. The PSpice software results are good for circuit analysis and Simulink software is good for systemic circuit especially for connecting to different loads. The control system of

proposed circuit is open loop so it is better to use PSpice software for analysis of each component which is more reality for finalise proposed circuit. The THD is quite high for this application so the section 5.2.3 has some explanation to reduce THD in this proposed circuit.

5.2.3 Reducing THD by optimising switching pattern in BBLFI circuit

The first method to reduce THD is to increase M_a in proposed circuit which can reduce lower order harmonics, but the voltage ratio decreases with increasing M_a. Also, there is limitation to increase M_a which cause discontinuous mode in the current of the inductor. The discontinuous current mode in the inductor can change the shape of output voltage to nonlinear. Another way to increase the value of the inductor in the proposed circuit which has some advantages and limitations. The advantages are more stable output voltage when the load size is changed and another advantage is to reduce THD. The limitations of increasing value of the inductor are size and cost. So the best way to reduce THD and keep the voltage ratio in the same is to optimise switching pattern of DSPWM. The switching pattern can be optimised by using DFT (section 4.5) to minimise amplitude of lower order harmonics. This method needs first to simulate circuit in software and import data in MATLAB. Then the written programmed code runs in MATLAB to minimise amplitude of low order harmonics of output voltage for optimising results. Then it needs to compare optimised results with original results from PSpice software. It needs to find the time difference between original output and optimised results. The time difference makes a new switching pattern of control signal which calls optimised control signal. The optimised control signal applied to main switch of the BBLFI circuit to reduce THD. Fig.5-7 shows the difference output voltage from the original DSPWM control signal and the optimised control signal which are applied to main switch of BBLFI.

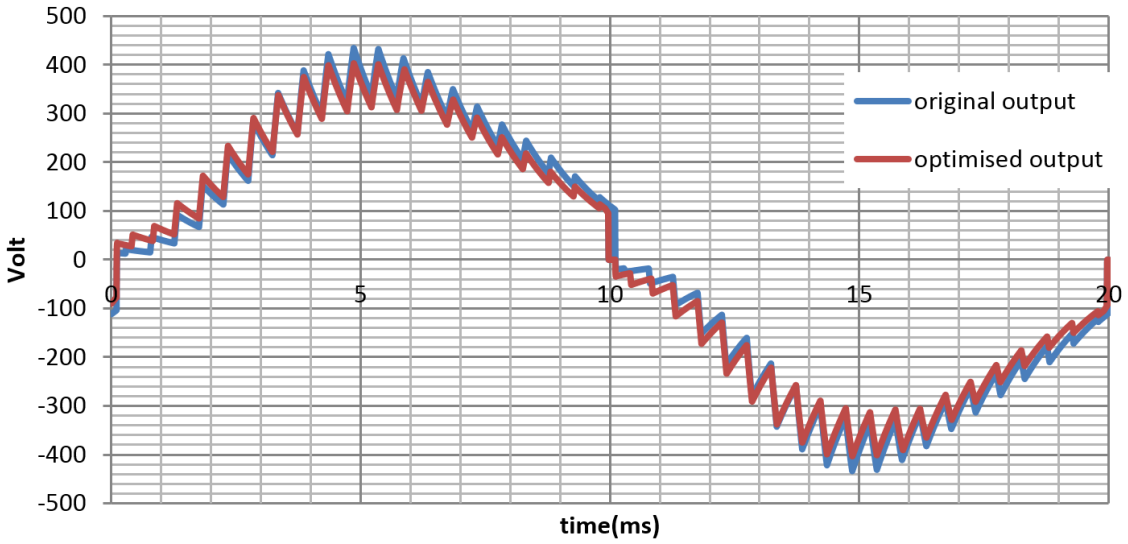


Fig. 5-7 Comparison results of original output and Optimised output voltage of BBLFI

The rms output voltage for both circuits is the same, but the difference in optimised output voltage and original output is shifted to the left and change switching patterns of original output. Fig 5-8 shows the comparison of FFT between two different output voltages. The amplitude of low order harmonic of optimised output is reduced 80%, which is programmed code required. The amplitude of lower order harmonics can reduce 100%, but the rms output voltage would be change. However, some harmonic orders are increased in comparison to original output voltage such as 15^{th}, 17^{th}, 21^{st} and 37^{th}. The THD in optimised output is reduced 3% in comparison to the original output voltage which are 8.9%. The THD can reduce to 6%, but the optimised rms output voltage is not the same as the original rms output voltage. The THD can be reduced by adding a series inductance to resistance and capacitor in BBLFI circuit. The THD can reduce less than 2% by adding inductance at the output of H-bridge.

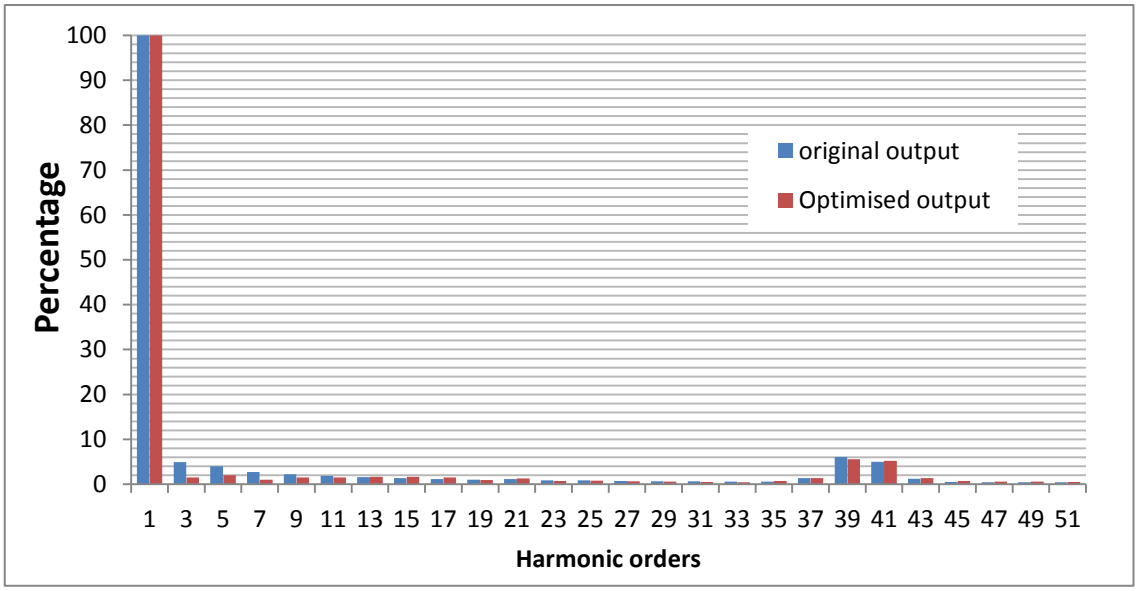


Fig. 5-8 The comparison of FFT between original and optimised output voltage of BBLFI circuit

There is an example of induction motor simulation in section 5.2.4 with 2.3kW and 0.9% power factor.

5.2.4 Induction motor drive

The BBLFI circuit can be applied as an induction motor drive in this chapter. The voltage and frequency can be increased at the same time on motor drive to speed up induction motor. The simulation of BBLFI motor drive circuit in PSpice software is shown in fig5-9. The simulation circuit is applied for constant speed in induction motor in this case. The voltage and frequency of this induction motor are 250 volts and 50Hz. The control signal for this proposed circuit is the same control signal of optimised in section 5.2.3. The value of inductance and capacitance is the same as previous proposed BBLFI circuit. The value of resistance in inductive load is 25Ω and an inductor is 40mH which is assumed as induction motor 2.3kW with 0.9 power factor.

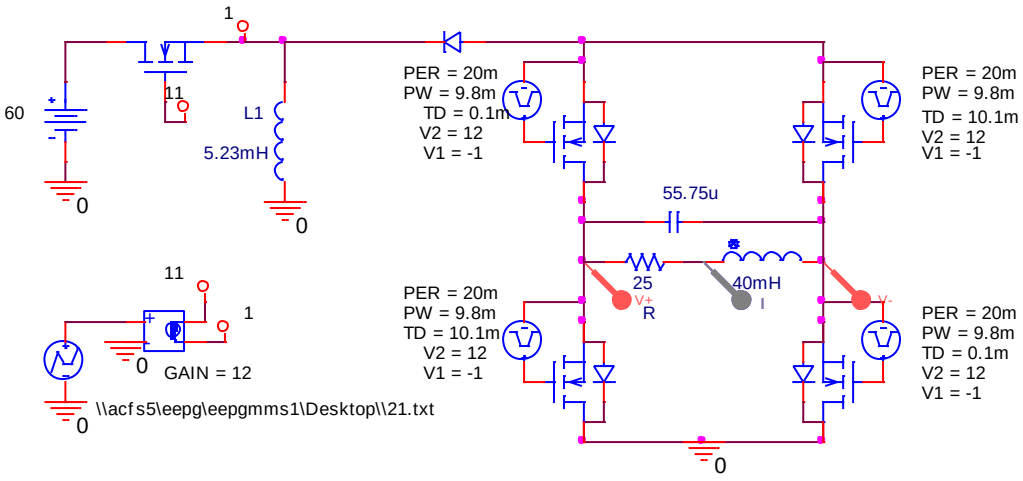


Fig. 5-9 The BBLFI circuit with induction motor

Fig.5-10 shows the voltage (red) across of the induction motor and current (blue) of induction motor. The phase shift between voltage and current is about 26%, which the power factor of this induction motor is 0.9.

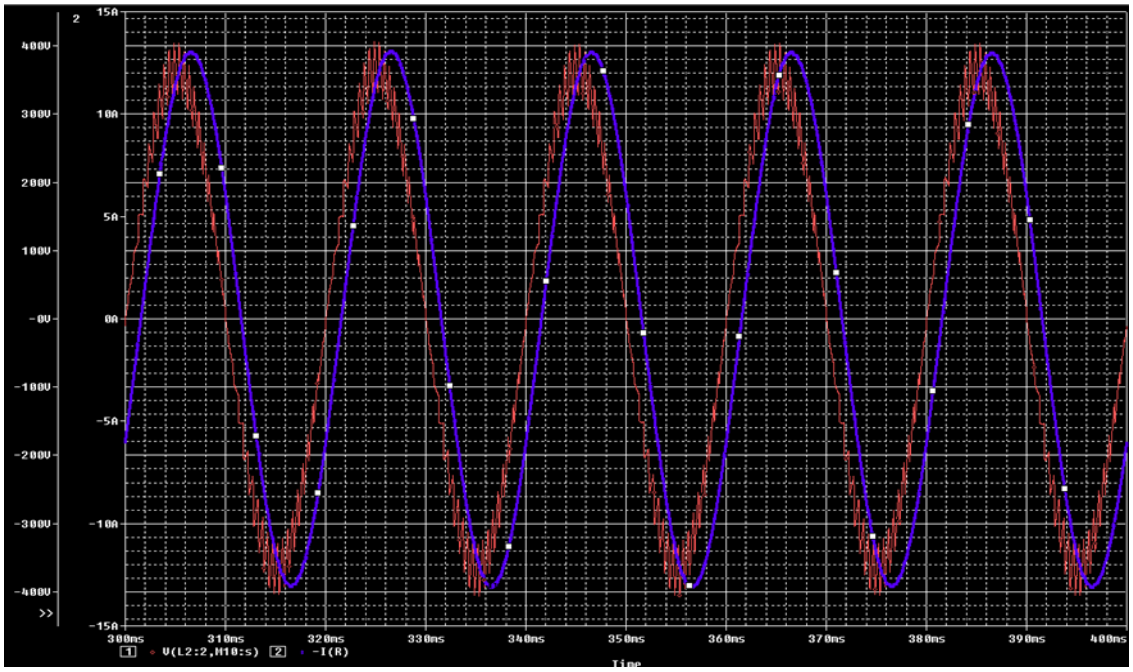


Fig. 5-10 Output voltage and output current of BBLFI circuit for induction motor driver.

The efficiency of this simulation proposed circuit is about 91%. The most power losses are conductive losses in devices. The THD of output voltage is 4%, which means the induction motor operates as a passive filter in this proposed circuit. However, the

proposed circuit steps up DC voltage and invert to AC output voltage. The speed of induction motor can easily control by varying M_a and M_f in switches of the proposed circuit with no change devices in proposed circuit. The DSPWM signal can control the output voltage and frequency of BBLFI circuit, which can be designed as application required. Also the DSWPM signal can control the output voltage and frequency boost-based low frequency in section 5.3.

5.3 Simulation of Boost-based Low Frequency Inverter controlled by DSPWM

The DSPWM is applied to the BLFI circuit to simulate at PSpice and Simulink softwares. The parameters of the component in the simulation circuit of these two softwares are chosen from design example of section 4.3.1. The M_a and M_f for this proposed simulation circuit are 0.34 and 40. This simulation section has 3 different simulations, first simulate BLFI circuit in Simulink with 2.5kW resistive load, and second simulate BLFI in PSpice with 2.5kW resistive load and finally simulate BLFI circuit as an induction motor drive in constant power 2.5kW and 0.9 power factor.

5.3.1 Circuit Simulation of Boost-based Low Frequency Inverter

BLFI circuit is simulated in two different softwares with same case studies. Also, this simulation case study is optimised to reduce low order harmonic. The BLFI circuit is simulated as an induction motor driver in this section

5.3.1.1 Circuit Simulation of BLFI topology in Simulink

Fig.5-11 shows the simulated circuit of the BLFI in Simulink which includes 2 main parts. The first part is a control signal generator (DSPWM signal) to control switches, and the second part is a power circuit to invert DC voltage from 60 volts to 250 AC output voltages. The power circuit of the BLFI includes 5 MOSFETs as switches, an

inductor, a capacitor, a diode, a resistance, a scope, a volt meter, a current meter and DC power supply. The control circuit is the same as control circuit as section 5.2.1.1. But the difference between this control circuit and control circuit in section 5.2.1.1 is the M_a which is 0.34 for BLFI circuit. However the value of L and C for BLFI circuit is same as design example in section 4.3.1 which is 8.5mH and 38.5µF.

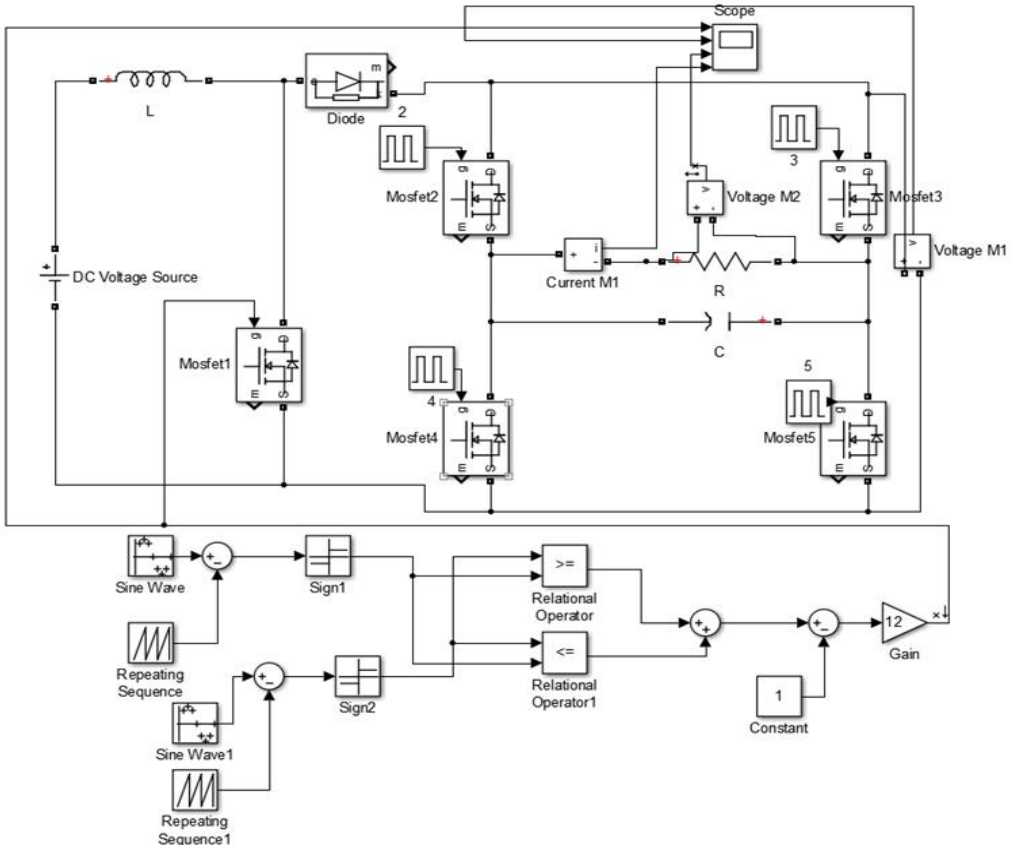


Fig. 5-11 Simulink simulation of proposed BLFI circuit with DSPWM

5.3.1.2 Simulink results of BLFI circuit

Fig.5-12 shows the simulation results of BLFI circuit in Simulink software. The fig5-12a shows the control signal of the main switch BLFI circuit that is 0 and 5V signal. The fig.5-12b shows the voltage across of H-bridge, which is stepping DC voltage. Fig.5-12c shows the output voltage of proposed circuit which rms value is 241V output. The current of resistive load in this proposed circuit is 9.64A, which is shown in fig.5-12d.

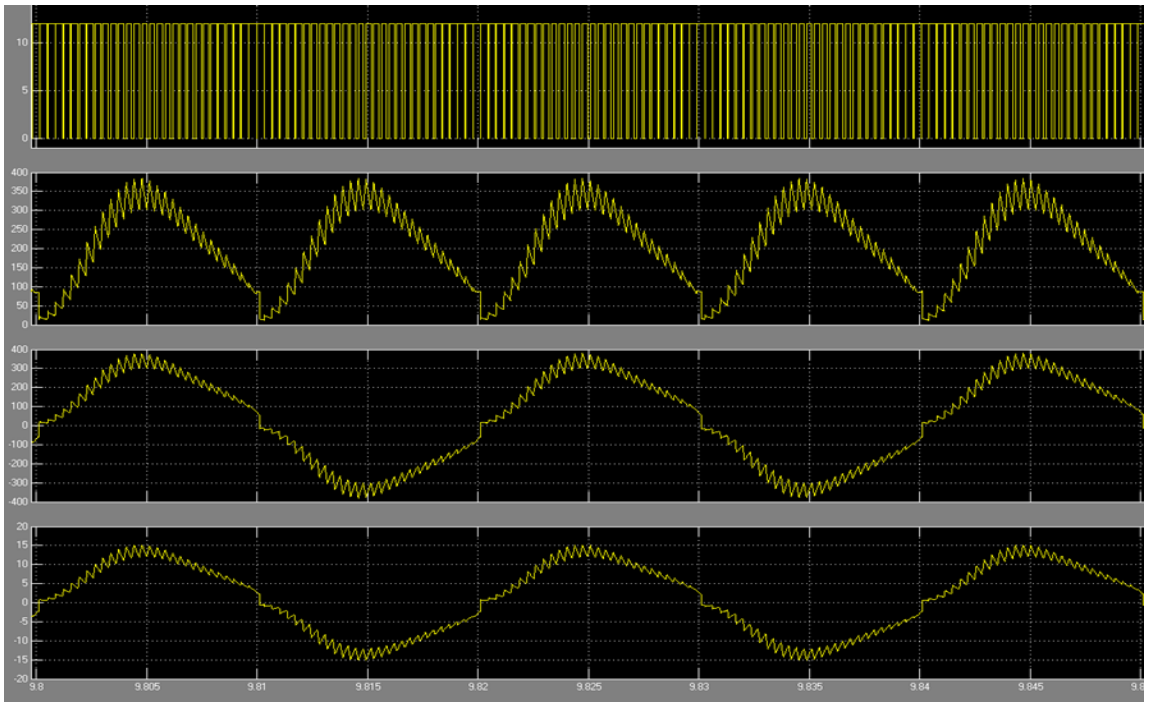


Fig. 5-12 Simulink simulation results of proposed BLFI circuit

The Fast Fourier transform of BLFI output voltage is shown in fig.5-13. The highest amplitude of harmonic orders is 39^{th} and 41^{st} which are about 7.3% and 7% of the output fundamental voltage. The amplitude of low order harmonics is less than 5% of output fundamental voltage. The THD of the output voltage for proposed circuit is 12.07%.

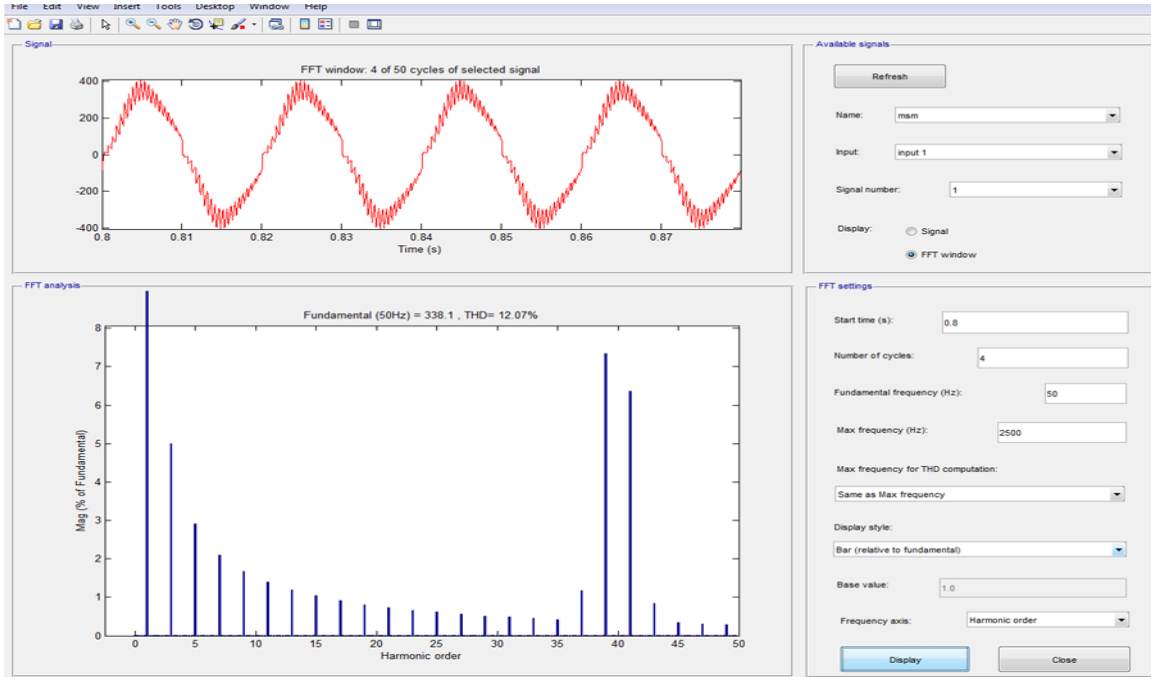


Fig. 5-13 The FFT of BLFI simulation circuit

This proposed circuit is simulated in PSpice software which is in section 5.3.1.3. The all parameters of BLFI circuit are repeated at PSpice simulation circuit.

5.3.1.3 PSpice simulation circuit of BLFI topology

The proposed circuit is simulated at PSpice which is shown in fig.5-14. This simulation circuit includes 2 main parts control circuit and power circuit. The control circuit of this simulation is the same of the control circuit of simulation at section 5.3.1.1. The power circuit of this simulation includes current source (boost converter) and H-bridge circuit. The switching frequency of the main switch of the boost converter is 2 kHz and amplitude modulation ratio is 0.34. All parameters of component are chosen from design example from section 4.3.1.

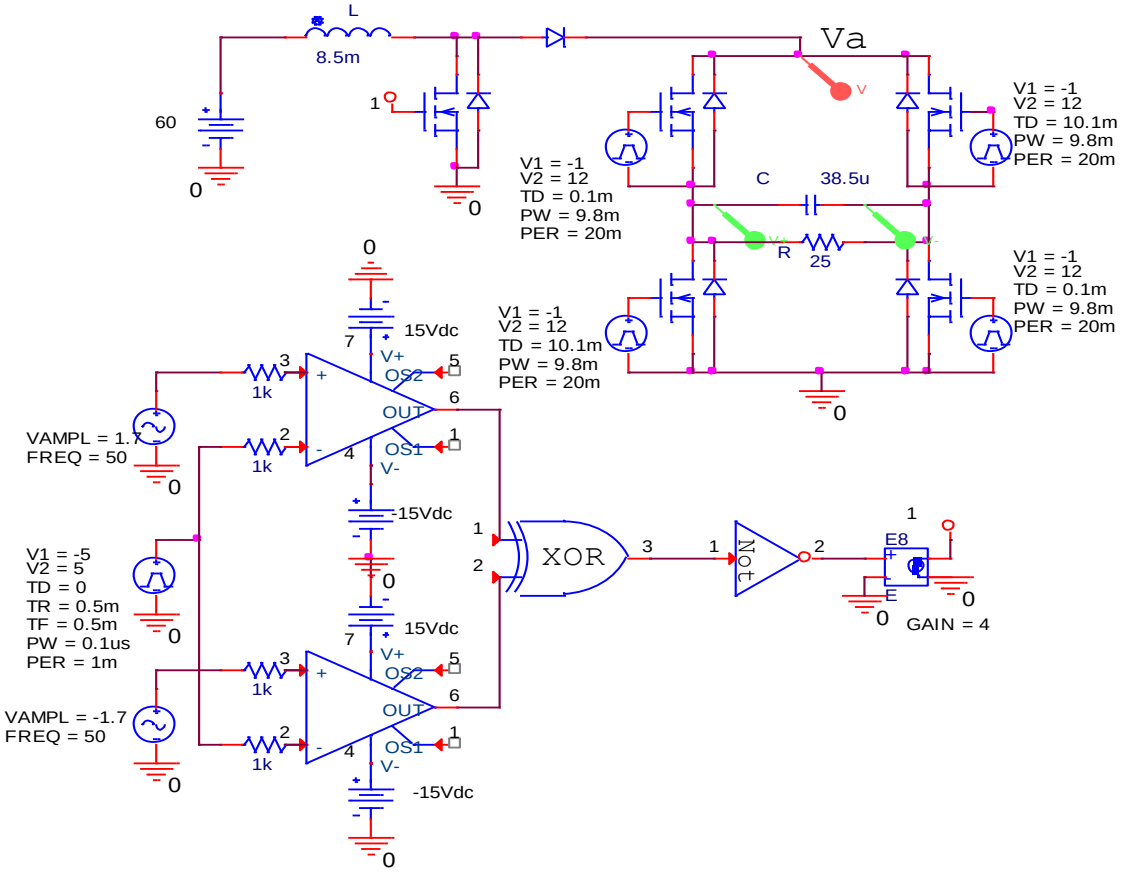


Fig. 5-14 The simulation circuit of the BLFI topology

5.3.1.4 PSpice simulation result of BLFI circuit

Fig.5-15 shows the DSPWM control pulses, the voltage across H-bridge (V_A), the output voltage and the output current of BLFI circuit. The rms output voltage is 250 volts and the rms output current is 10A. The output power of BLFI circuit is 2.5kW and efficiency of proposed circuit is 92%. The most power losses are from the resistance of components and switching losses can be neglected, which is less than 1%.

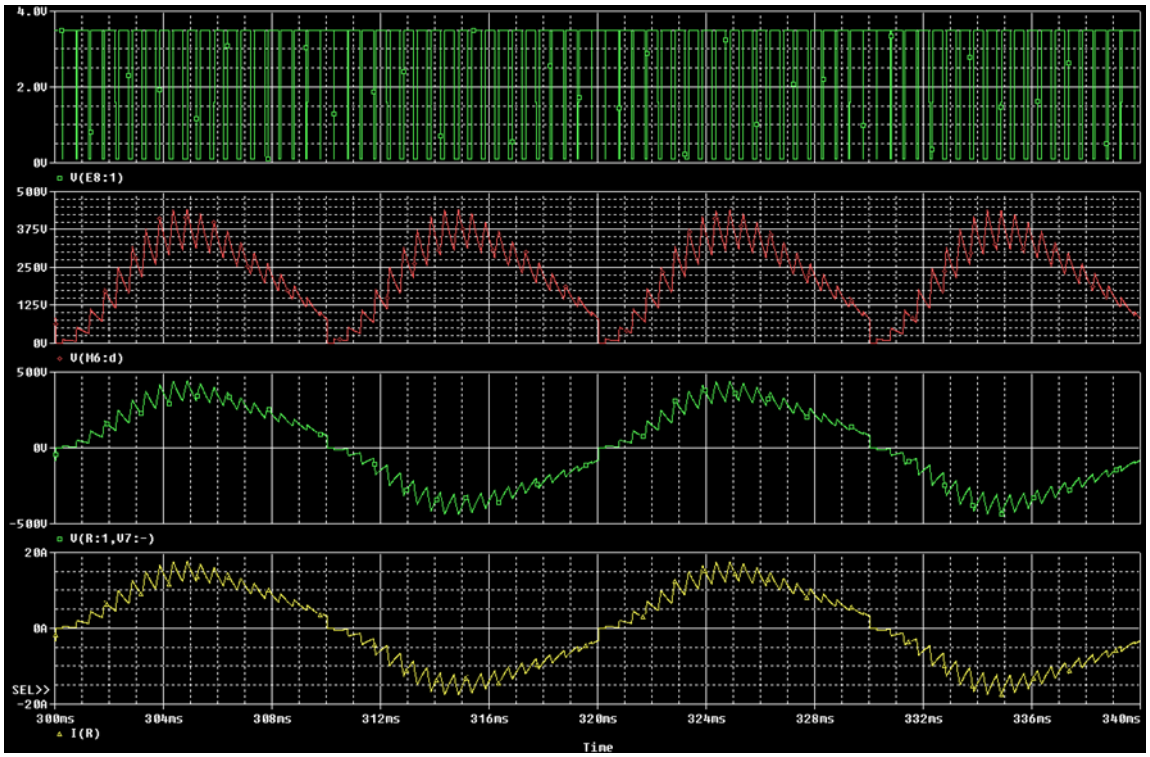


Fig. 5-15 PSpice results of BLFI simulation circuit; a) control signal, b) voltage across H-bridge, c) output voltage, d) output current

The harmonic distortions of the output voltage are shown in fig.5-16. The highest amplitude of harmonic orders is 39^{th} and 41^{st} which is swinging frequency of the circuit. The amplitude of these harmonic orders is 7% and 8% of fundamental value. The amplitude of 3^{rd} and 5^{th} harmonic orders is 6% and 5% of fundamental value. The THD of output voltage for BLFI circuit is 12.34%. This THD can reduce to 8.7% by the optimising switching pattern of DSPWM control signal in section 5.3.3.

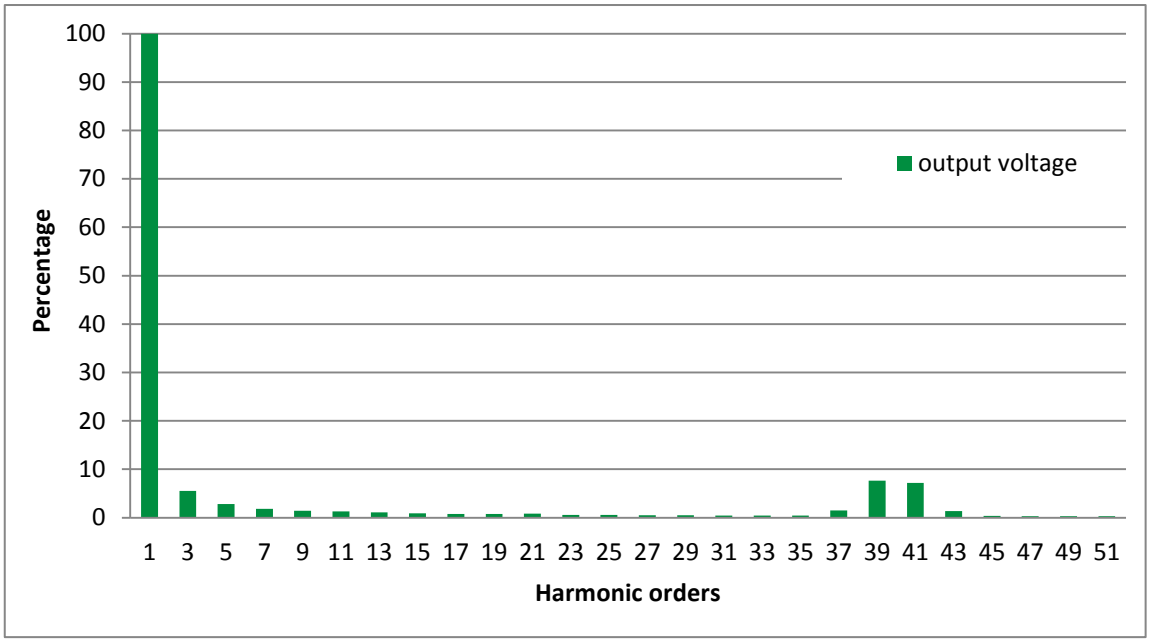


Fig. 5-16 FFT of output voltage from proposed circuit (BLFI)

5.3.2 Discussion of comparison results of BLFI circuit in two softwares simulation.

These two softwares simulation results are almost the same. Table5.2 shows the comparisons between BLFI voltage ratio, efficiency and THD in these softwares simulation and theoretical results.

Table 5.2 The comparison between results of BLFI circuit in Simulink and PSpice softwares with theoretical results from design example.

Software	Input voltage	Output voltage	Input power	Output power	Voltage ratio	Efficiency %	THD %
Simulink	60	241	2553W	2323.24W	4.016	91%	12.07
PSpice	60	250	2717.4W	2500W	4.166	92%	12.84%
Theoretical	60	250	2500W	2500W	4.166	100%	12.24%

Table5.2 shows that the comparison results of BLFI circuit in two softwares and theoretical almost are the same, especially the result of PSpice and theoretical. The output voltage of Simulink can be increase to 250 volt by decreasing M_a from 0.34 to 0.327 in simulation circuit. The comparison between results from PSpice and Simulink

softwares in section 5.2.2 and section 5.3.2 shows that the result of PSpice software is more close result to theoretical. So the PSpice software is used for the next simulation for FLFI circuits. The THD of BLFI simulation circuit can reduce 8.7% of optimising control signal to minimise lower order harmonics in section 5.3.3.

5.3.3 Reducing THD of BLFI circuit by optimising switching pattern.

The optimised switching pattern can reduce THD of BLFI output voltage. Fig.5-17 shows the differences between original output voltage and optimised output voltage across of load in BLFI circuit.

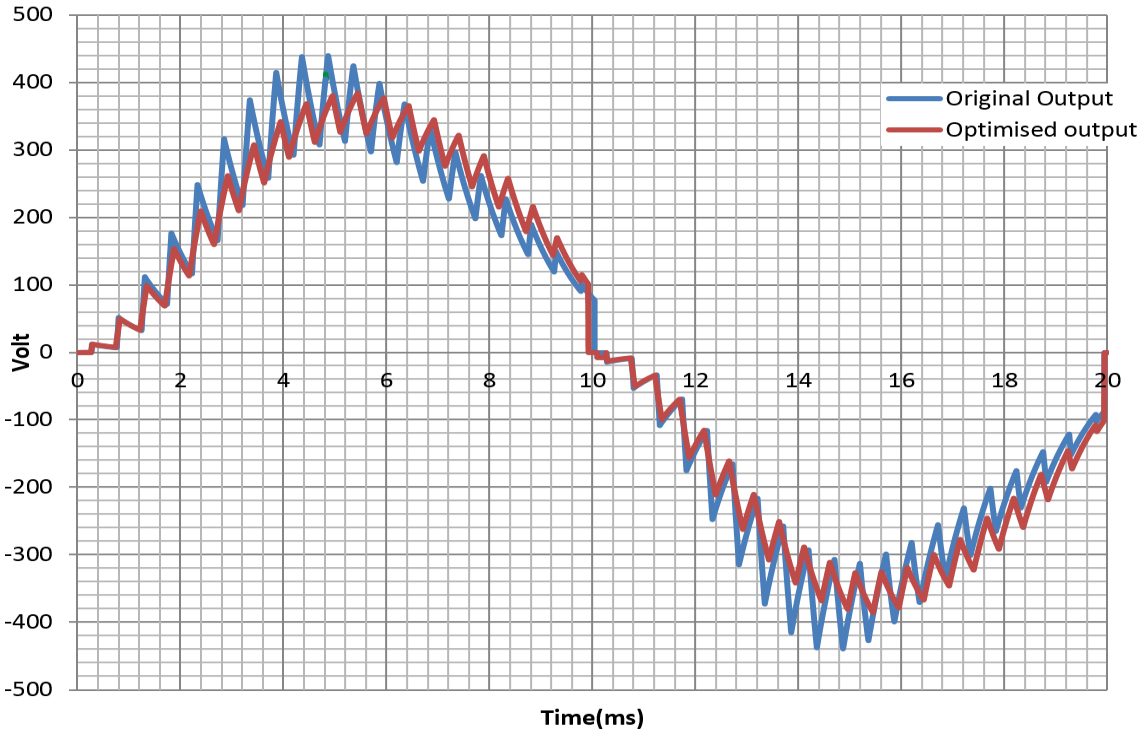


Fig. 5-17 The original and optimised output voltage of BLFI circuit

Fig 5-18 shows the differences between harmonic orders of original and optimised output voltage. The amplitude of low order harmonics is less than 2% of fundamental value. The THD of optimised output voltage is 8.7%, which can reduce less than 2% by adding filter at the output of H-bridge to eliminate amplitude of switching frequency harmonics.

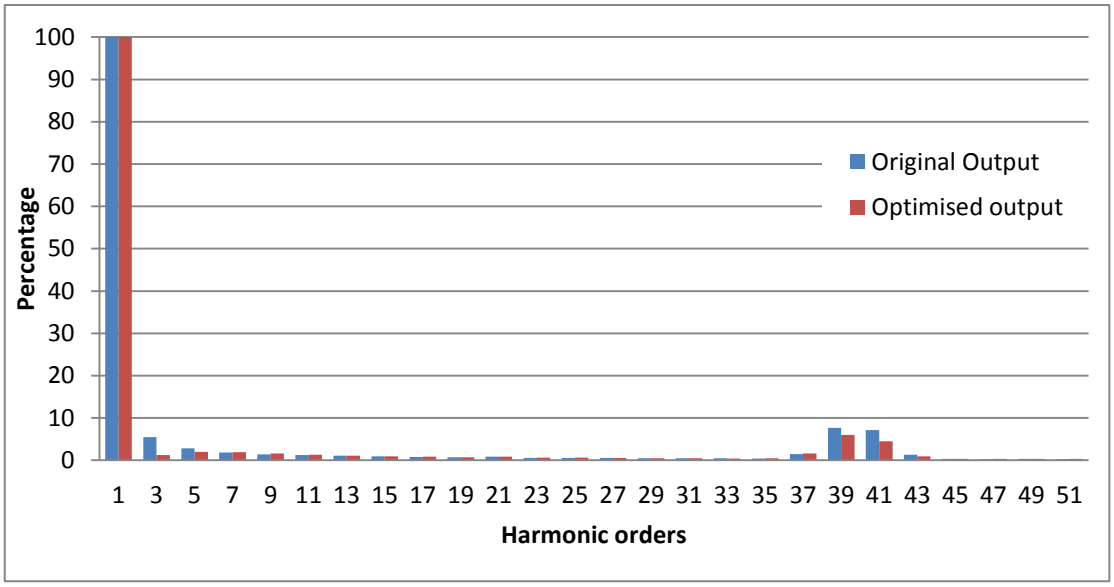


Fig. 5-18 The FFT of BLFI original and optimised output voltage

The optimised switching pattern is done by programming code in MATLAB. This program code runs DFT method to reduce amplitude of low order harmonics which is the same program code in section 5.2.3. The optimised control signal is applied to control main switch of the BLFI circuit to minimise lower order harmonics. This optimised DSWPM signal is applied for induction motor drive for constant load in section 5.3.4.

5.3.4 Induction Motor drive

This section is simulation of the BLFI circuit to be induction motor drive in PSpice software. The induction motor is chosen same as the induction motor in section 5.2.4. The output power of inductive load is 2.5kW and 0.9 power factor. The power of this load assumes constant in this simulation. Fig.5-19 shows the motor drive of BLFI power circuit and control signal circuit. The control signal is chosen the same control signal from optimised output voltage to minimise lower order harmonics.

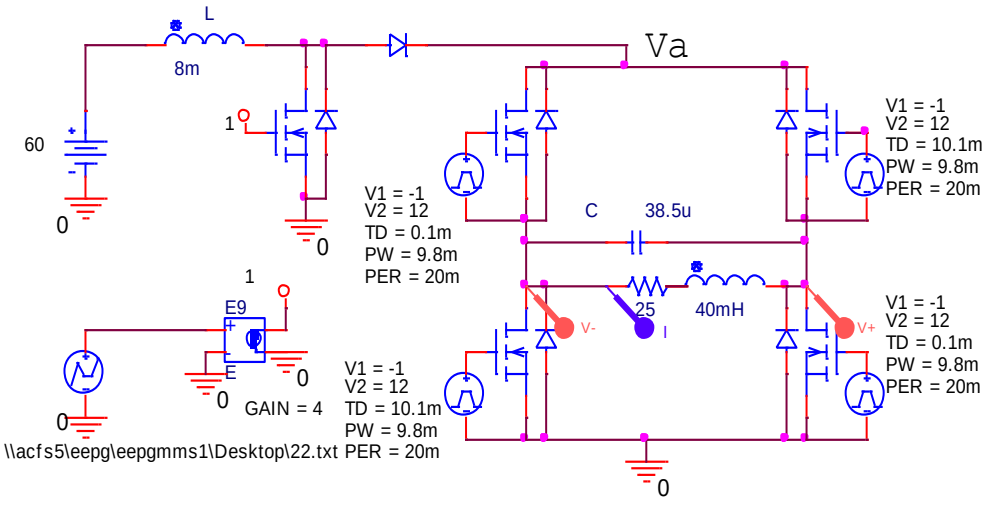


Fig. 5-19 BLFI Simulation circuit for induction motor drive

Fig 5-20 shows the output voltage of the BLFI circuit across of induction motor also it shows the current of induction motor. The terminal voltage (rms value) of induction motor is 248.218 volts and the rms current value is 8.84A. The voltage across of resistance is 220volt which can be increase to 250volt by decreasing M_a value to 0.297 in DSPWM control signal. The THD of output current is increased from 1.5% to 13% by decreasing value of M_a in DSPWM control signal. This limitation can be solved by optimising again switching pattern of DSPWM control signal. However, the electrical output power of this induction machine is 1.944kW and power factor of this induction machine is 0.9 lagging. The phase shift between current and voltage is 25.84 degree (1.43ms). The efficiency of this proposed circuit is 92% where the average input power is 2.11kW. The most power losses of this proposed circuit are from conductive losses of switches, especially main switch on BLFI circuit which is about 2% of average input power.

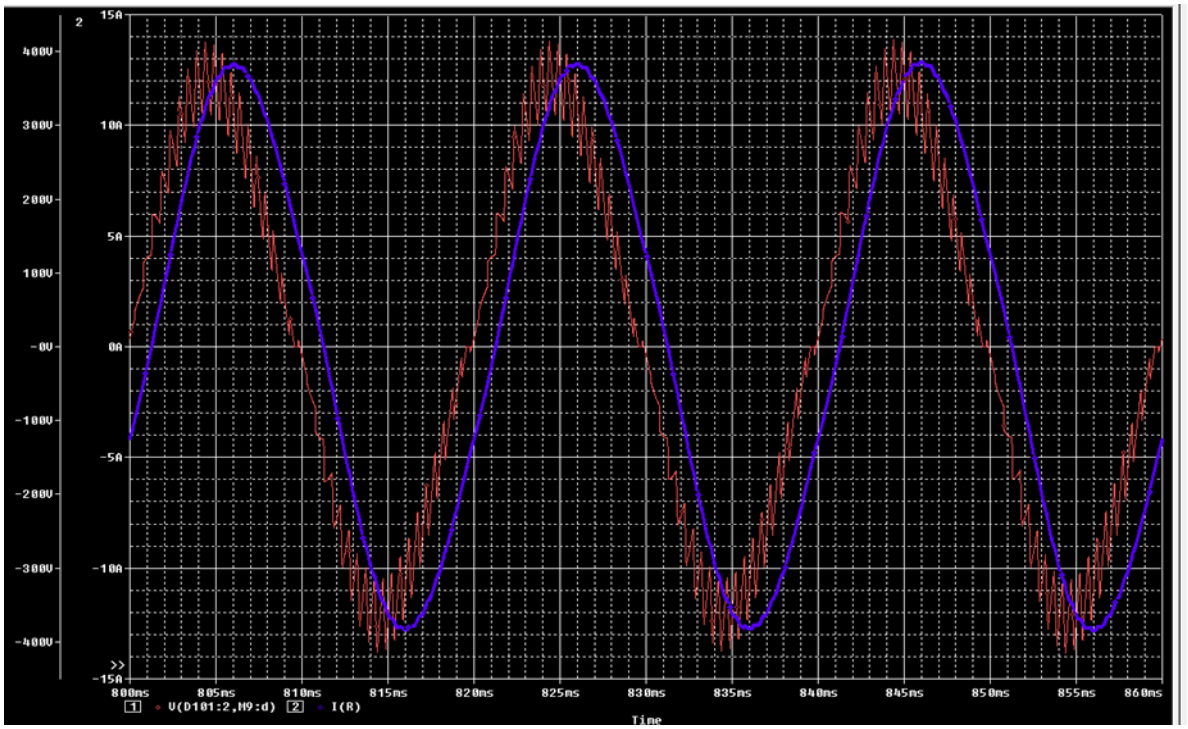


Fig. 5-20 Voltage across of induction motor and resistance current of induction motor

The simulation results of BLFI circuit show proposed circuit can be applied as motor drive which can easily to control speed of induction machine. The speed of the motor is varied by controlling M_a and M_f in main switch of BLFI circuit. Also the H-bridge switching frequency should change to control speed of the motor, which depends on speed required of induction motor.

5.4 Simulation of Flyback-base Low Frequency Inverter.

The FLFI circuit can simulate at different softwares, which is simulated in PSpice in this section. The all parameters of component are chosen from design example in section 4.4.1. The output voltage and the input voltage of this circuit are chosen the same previous simulations. The main difference between this simulation circuit with previous simulation circuits is to replace transformer to inductor in power BLFI circuit. The control circuit of BLFI and FLFI circuit is the same, but only the M_a with this simulation circuit increase to 0.448 in comparison to M_a in simulation BLFI control signal. Fig.5-21

shows the simulation of FLFI circuit with an input DC source (60 volt), a transformer (ratio 2), 5 switches, a resistive (load 25Ω), a capacitor and control circuit.

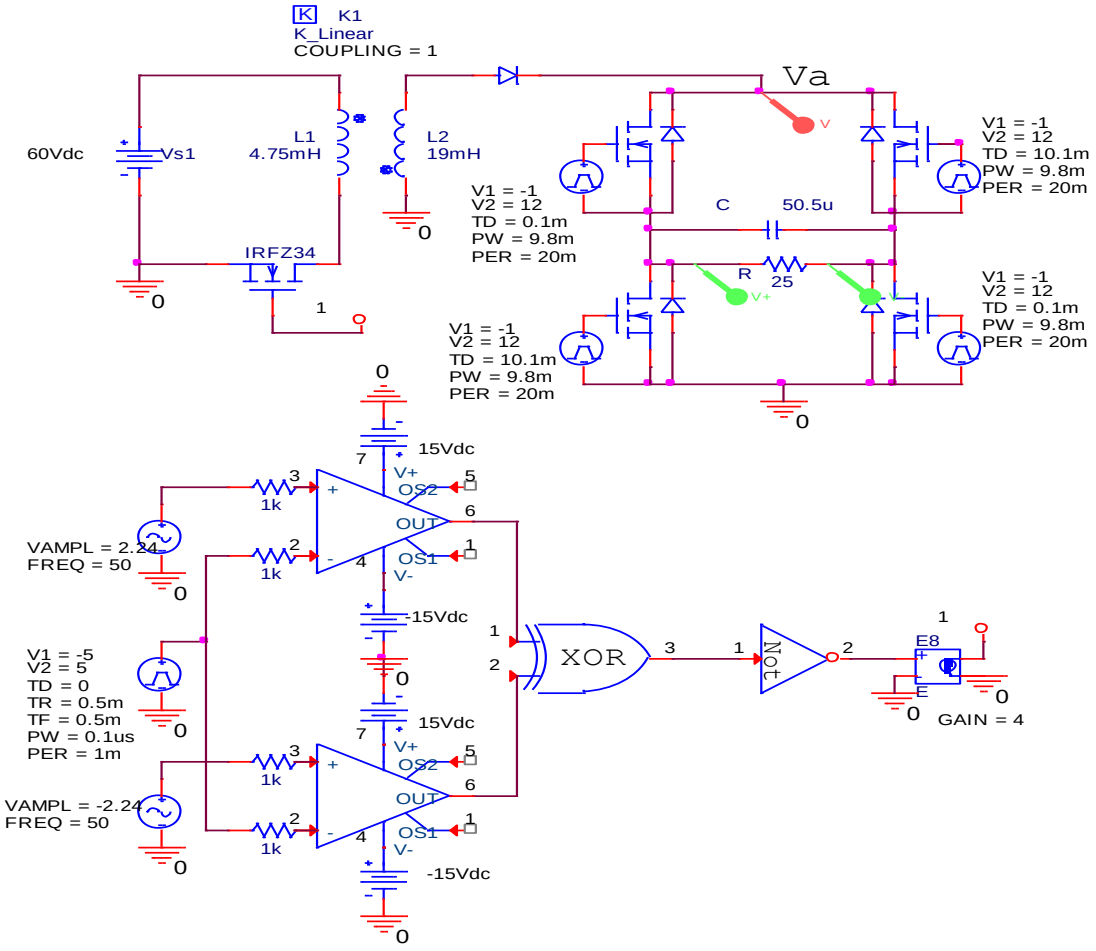


Fig. 5-21 simulation of FLFI circuit

5.4.1 PSpice Simulation results

There are 2 different modes of operation during the first 10 ms of this circuit. Mode 1 (Fig.5-22.b): the voltage rises from zero to 405 volt at the first 5ms with maximum 25% ripple volt at peak value. S_1 operates at 2 kHz; in this mode the capacitor (50.5μF) and transformer operates in the boost converter mode during the first 5ms. In mode 2 the voltage decreases to zero for the next 5ms during the first half cycle of V_a.

The two switches S_2 and S_4 direct the current into the load from 0 to 10 ms during the positive half cycle. In the negative half cycle the operation of the circuit is similar but switches S_3 and S_5 replace the operation of S_2 and S_4 (Fig.5-21).

The DSPWM pulses shown in Fig.5-22.a) are for M_f=40 and M_a=0.4465. Fig.5-22.c shows the impact of the DSPWM on the inverting output voltage and fig.5-22.d shows the current of resistive load of H-bridge.

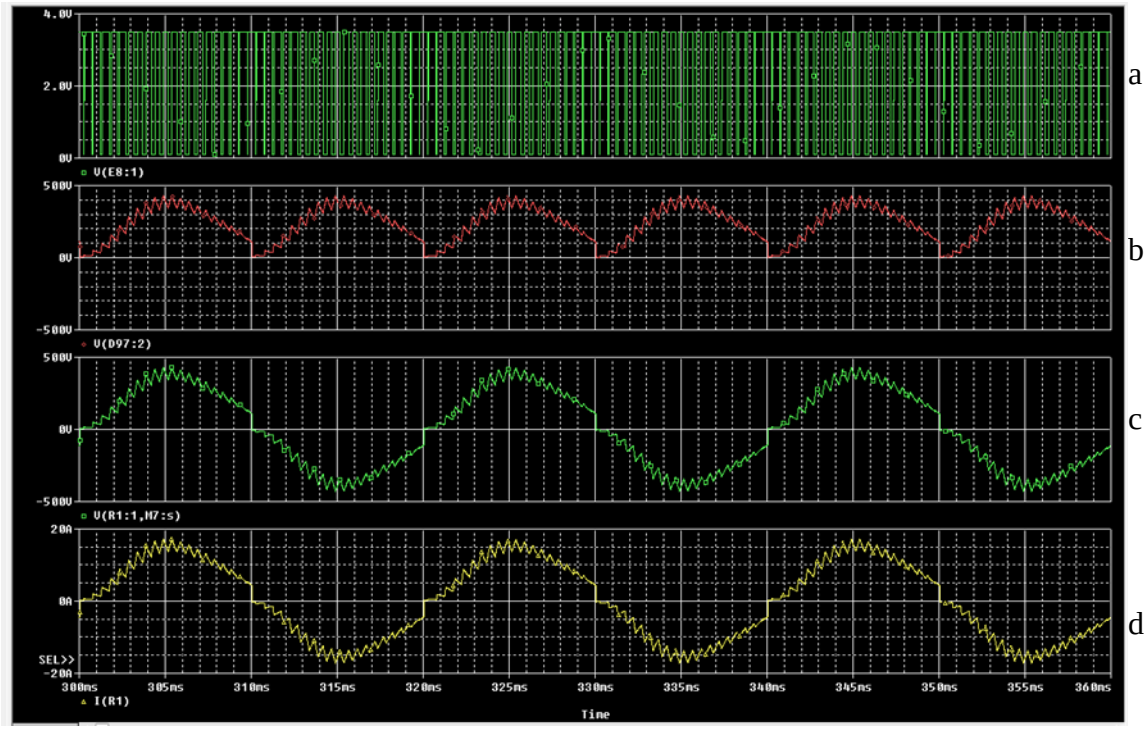


Fig. 5-22 FLFI simulation results a) control signal, b) voltage across H-bridge, c) output voltage, d)output current

The rms output voltage of this simulation circuit is 252volt and the output current is 10.08A. The output power for this simulation circuit is 2.54kW and efficiency is 92% of PSpice software simulation.

Fig.5-23 illustrates the FFT of the waveform of Fig.5-22.c. The value of M_f controls the amplitude of harmonic generated. The T.H.D of FLFI circuit is 10.8% in this example. The harmonic factor of the lowest order harmonic is reduced by selecting high value of M_f. This is achieved through a single DC source and a single capacitor. The amplitude value of fundamental voltage is 354.33 Volt. In this figure the 39th and 41st harmonics are the highest value which are about 8% of the fundamental voltage. The 3rd, 5th and 7th

harmonics are less than 5% of the fundamental voltage. The total harmonic distortion can be reduced to less than 1% by using filter.

The r.m.s of the output voltage is:

V_{rms} = 252 V, $V_{rms\,(1)}$=250.55 V

$$\text{THD}=\frac{\sqrt{V^2_{rms}-V^2_{rms(1)}}}{V_{rms(1)}}\times 100\% = \frac{\sqrt{252^2-250.55^2}}{250.55}\times 100 = 10.8\%$$

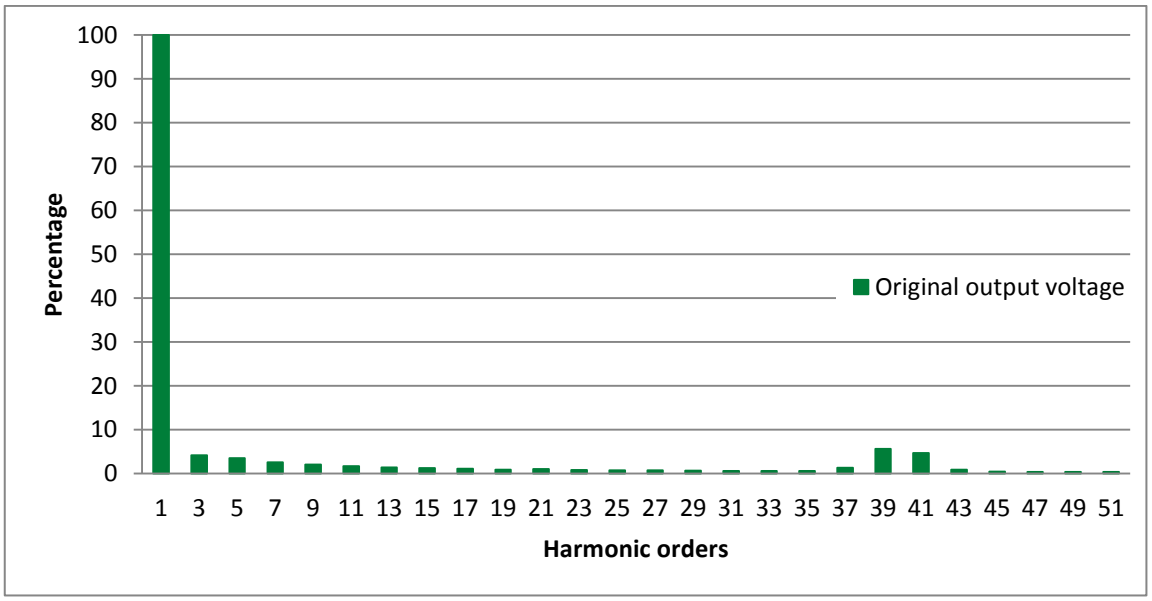


Fig. 5-23 The FFT of original output voltage of FLFI circuit

The THD of this simulation circuit can reduce less than 10% by optimising switching pattern in section 5.4.2

5.4.2 Reducing low order harmonics

The DSPWM control signal is being optimised to reduce THD where the amplitude of low order harmonics is reduced by DFT programmed code. There is limitation to eliminate all amplitudes of lower order harmonics. This limitation is to change rms value of output voltage, which changes output power. So the user can choose which object is important for application voltage ratio or THD. Fig 5-24 illustrates the differences between original and optimised output voltage of FLFI circuit which the rms output voltage for both them is 252volt.

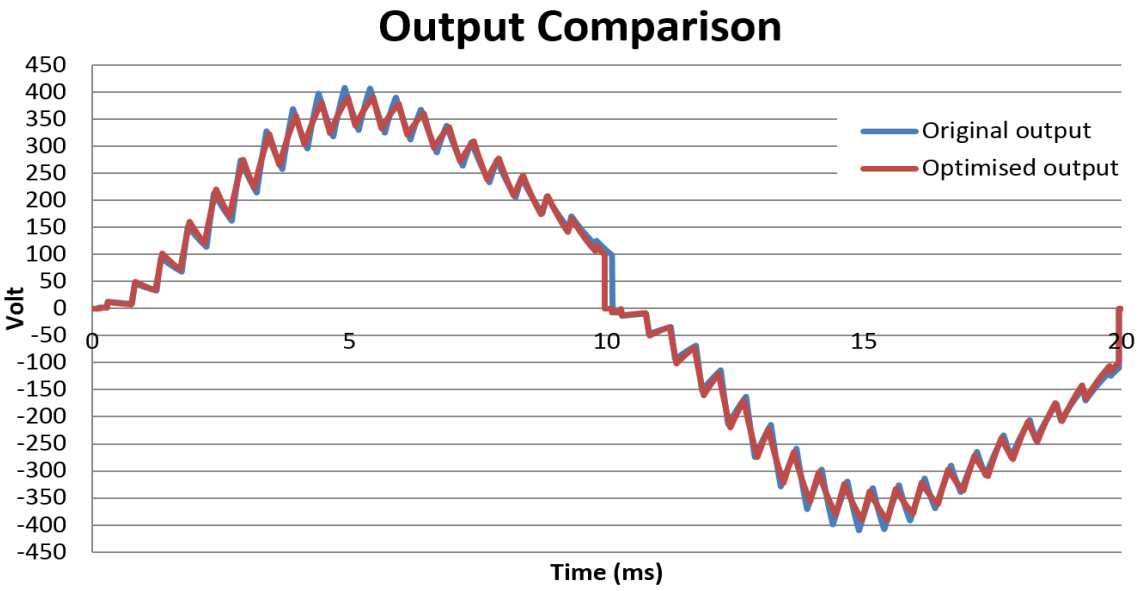


Fig. 5-24 comparison original and optimised output voltage of FLFI circuit

The FFT of optimised output voltage is shown in fig 5-25. The amplitude of lower order harmonics is less than 2% of fundamental value. In this figure the 39^{th} and 41^{st} harmonics of optimised output are not changing too much which is reduced to 7% of the fundamental voltage. So the THD of optimised output reduces to 7.5% in this proposed circuit.

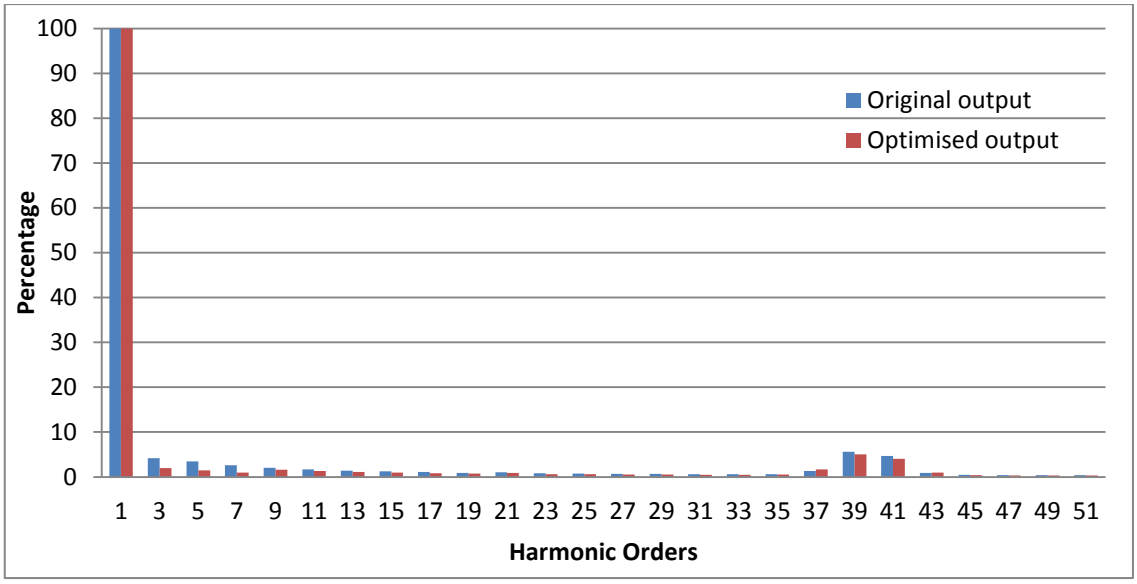


Fig. 5-25 The FFT of original and optimised output voltage of FLFI circuit.

5.4.3 Discussion of simulation FLFI result

The rms output voltage of FLFI circuit can easily control by changing M_a in main switch of the proposed circuit with no change the transformer. Also the THD of FLFI circuit can reduce to 5% with no filter required by the optimising switching pattern. The FLFI circuit has a couple of advantages in comparison to BBLFI and BLFI circuit. The first advantage of FLFI circuit is smaller size component in comparison to both proposed circuit. The THD of FLFI circuit is lower than THD of BBLFI and BLFI circuits in same voltage ratio. However the THD of BBLFI, BLFI and FLFI circuits can reduce with increasing switching frequency of the main switch of proposed circuits. Also the inductor or transformer size of these proposed circuits can decrease with increasing switching frequency. But the switching losses are increased by increasing switching frequency. The section 5.4.4 shows an example of switching losses from simulation of FLFI circuit.

5.4.4 Switching losses in the proposed circuit

The MOSFET and diode used in the simulation are 44N50P and 30EPF.

For the MOSFET to operate at 2 kHz at average input voltage of 60V and 42A current, the switching power loss can be evaluated from equations (4-4 to 4-7):

For the 'on' and 'off' states of the 44N50P MOSFET, R_{on}=140 mΩ, and $G_{off} = 1 \times 10^{-6} s$.

Where the rising and falling times of the current and voltage waveforms are:

$t_{ri} = 200ns,$ $t_{d(on)} = 32ns,$

$t_{rv} = 90ns\,,$ $t_{d(off)} = 37ns$

$t_{on} = t_{ri} - t_{d(on)}$= 200-32=168ns

$t_{off} = t_{rv} - t_{d(off)}$= 85-27=58ns

The losses in the S_1 power MOSFET (44N50P) can be evaluated from the following equations:

From equation (4-4)

$$P_{sw(s1)} = \frac{1}{2} \times 42A \times 60V \times (226ns) \times 2000 = 570mW$$

From equation (4-5)

$$P_{conducting\ loss\ (s1)} = 42^2 \times 0.14 = 247W$$

From equation (4-6)

$$P_{switch\ when\ is\ off(s1)} = 60 \times 1 \times 10^{-6} = 0.060m\text{W}$$

The total losses in the inverter, four switches (S_2-S_5) can be calculated from equations (4-4 to 4-6). The rms output voltage and current are 250V and 10A.

$$P_{sw(s2\ to\ s5)} = 4 \times \frac{1}{2} \times 10A \times 250V \times (226ns) \times 50 = 57mW$$

$$P_{conducting\ loss\ in\ switch(s2\ to\ s5)} = 4 \times 10^2 \times 0.14 = 56W$$

$$P_{switch\ when\ is\ off(s2\ to\ s5)} = 4 \times 250 \times 1 \times 10^{-6} = 1mW$$

It should be noted that the frequency used in (S_2-S_5) is 50Hz compared to 2 kHz used in S1.

The total power loss in the diode (30EPF) of the boost converter at 2 kHz on this simulation is 1.25W in this case study from equations 4-4 and 4-5. The averaging voltage and current in this diode are 233 volts and 10A. The resistance of the diode is 12.5 mΩ when the diode is on. All this information is obtained from data in PSpice software of fast soft recovery rectifier diode (30EPF).

From equation (4-7).

$$P_{conductor\ loss\ in\ diode} = 10^2 \times 0.0125 = 1.25W$$

The simulated total power losses in semiconductor switches and the diode is about 304.878W, which includes all loss in switches and diode. So the efficiency of this topology in simulation is about 88%.

The total power loss in semiconductor (P_t).

P_t=0.570+247+0.00006+0.057+56+0.001+1.25 =304.878W

The switching loss of main switch (S1) of FLFI circuit is 570mW which is very small compare to output power (2500W). So if the switching frequency in main switch is increased two times the switching loss of S_1 is two times (1.14W) which is still very small in comparison with output power. The switching frequency of H-bridge still 50 Hz and switching losses is no change in H-bridge switches. However, the most loss is conductive losses in main switch (S_1) that is 247W. This power loss is very high for this proposed circuit which is nearly 10% of output power. So the main switching losses does not depend on switching frequency, then the power losses can reduce by adding one more MOSFET in parallel with S_1 in FLFI circuit. The conductive resistance of MOSFET in proposed circuit assumed 70 mΩ which half times of conductive resistance of MOSFET (44N50P). The conductive power loss in S_1 is 123.5W for the FLFI simulation circuit in section 5.4. So the total power losses of the FLFI simulation circuit are about 8% of input power. Furthermore, the switching frequency can increase two times in FLFI, BLFI and BBLFI circuit to reduce THD. Also the switching losses increase two times which are still very small in comparison to power conductive losses of switch which is 123.5W. So proposed circuits can operate at 3 kHz or 4 kHz with a same power circuit which causes to reduce THD. There is a simulated example of FLFI circuit to the same circuit of section 5.4 with 3 kHz switching frequency. The control signal is optimised by DFT code.

The DFT code can reduce THD for this case to 6% with no changing the passive components. The changes are only switching pattern of the main switch of the flyback converter circuit. Fig5-26 shows the FFT graph of output voltage after optimised the switching pattern for 2 kHz and 3 kHz switching frequency. The amplitude of the 3rd, 5th and 7th harmonic of 3 kHz switching frequency example is reduced less than 1%.

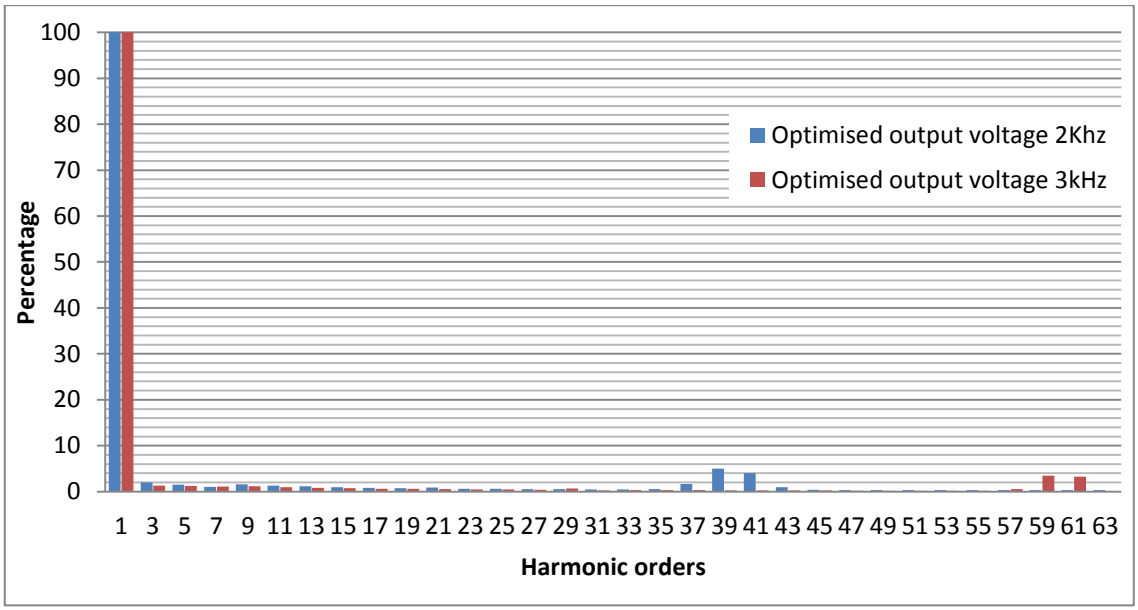


Fig. 5-26 The comparison between FFT of optimised output voltage (2kHz) and FFT of optimised output voltage (3kHz).

The THD of optimised output voltage with 3 kHz switching frequency on S_1 of FLFI circuit is 6% that is reduced 1.5% in comparison to optimised output voltage with 2 kHz switching frequency on S_1. The switching loss has increased 50% where frequency increases 50%. So the switching loss is less than 1W in the FLFI circuit with 3 kHz switching frequency. These proposed circuits are tested in practical implement in different loads and conditions in chapter 6.

Chapter 6 Practical setup

6.1 Introduction practical experiment

The DSPWM control signal is applied to BBLFI, BLFI and FLFI practical implement circuits. The circuit of these proposed topologies is almost the same and controller circuit of them is the same as well. The main difference in these proposed power circuits is the connection between components of these circuits. The M_a of DSPWM control signal depends on voltage ratio, which is chosen by power application situation. The practical result of these proposed circuit is compared to other topologies practical results such as PWM, NPC and cascading H-bridge.

6.2 Practical setup of proposed circuit

The circuit is built with 10 time's smaller loads which is used in the simulation section (chapter 5). The reason to use smaller load is power limitation on an implement of the laboratory. The DC power supply detail is 0-340V and maximum current is 4A. The maximum resistive load is 320W with 240volt. A Microcontroller UNO 32 is used in proposed circuit as controller. The Microcontroller is programmed in the Arduino software with original and optimised switching pattern for proposed circuits (BBLFI, BLFI and FLFI circuits). An example programmed code is described in appendix B. This programmed code can control the output voltage and the output frequency by varying potential meter from the input of the Microcontroller. The pulse width modulation of the Microcontroller output can control by changing the input voltage of the Microcontroller. The programmed code of each proposed circuit is different to eachother. The load is 177 Ω and the frequency in inverter is 50 Hz and the values of C and L in the current source converter are 2.35 μF and 58 mH. There is lab limitation to

use the exact values of R, C and L, which are used in simulation part. A 2.35 µF is used instead of 2.7 µF. A 58 mH is used in the practical instead of the calculated 40 mH. A fixed value of 177 ohm resistance is used instead of the calculated 250 ohm. The switching frequency of main switch (S_1) at proposed circuits is 4 kHz, which the frequency is twice of switching frequency of simulation section (chapter 5).

The implement of proposed circuits (BBLFI and BLFI circuit) are the same and only differences between these two proposed circuits is switching pattern (Difference Ma). A transformer is replaced to inductor in FLFI circuit. The transformer primary winding inductance is 7.9mH and secondary winding inductance is 24.5mH. The H-bridge of proposed circuits is built of 4 MOSFETs and drivers. The capacitor is a series of two capacitors of 4.7 µF. This chapter includes 5 parts which are different case study for proposed circuits.

6.3 Buck/Boost-based Low Frequency Inverter practical implement

This proposed circuit is designed for two different loads in different the rms output voltage 100V as buck converter and 252V as boost converter. The input DC voltage is 150 volts for these two case studies. This section describes practical built circuit, practical results and finalising results.

6.3.1 Practical implemented circuit of BBLFI topology

Fig 6-1 shows the built practical proposed circuit for two different case studies with the same components. The output voltage is changed in these two case studies by changing the pulse width in programming code from Arduino software. Table 6-1 shows the component's value for this proposed circuit.

Table 6.1 components parameter of proposed circuit

	Component	**Value**
1	Resistance (parallel 3 different resistances with 532Ω per each)	177Ω
2	Voltage probe	100X
3	DC voltage source	150V
4	Current probe	100mV/1
5	Capacitor (series two capacitors of 4.7µF)	2.35µF
6	H-bridge (4 MOSFTEs and 4 drivers)	44N50P
7	Microcontroller Arduino	UNO 32
8	Single MOSFET (Main switch of BBLFI circuit)	IXFH 44N50P
9	Diode	30EPF
10	Inductor	58mH

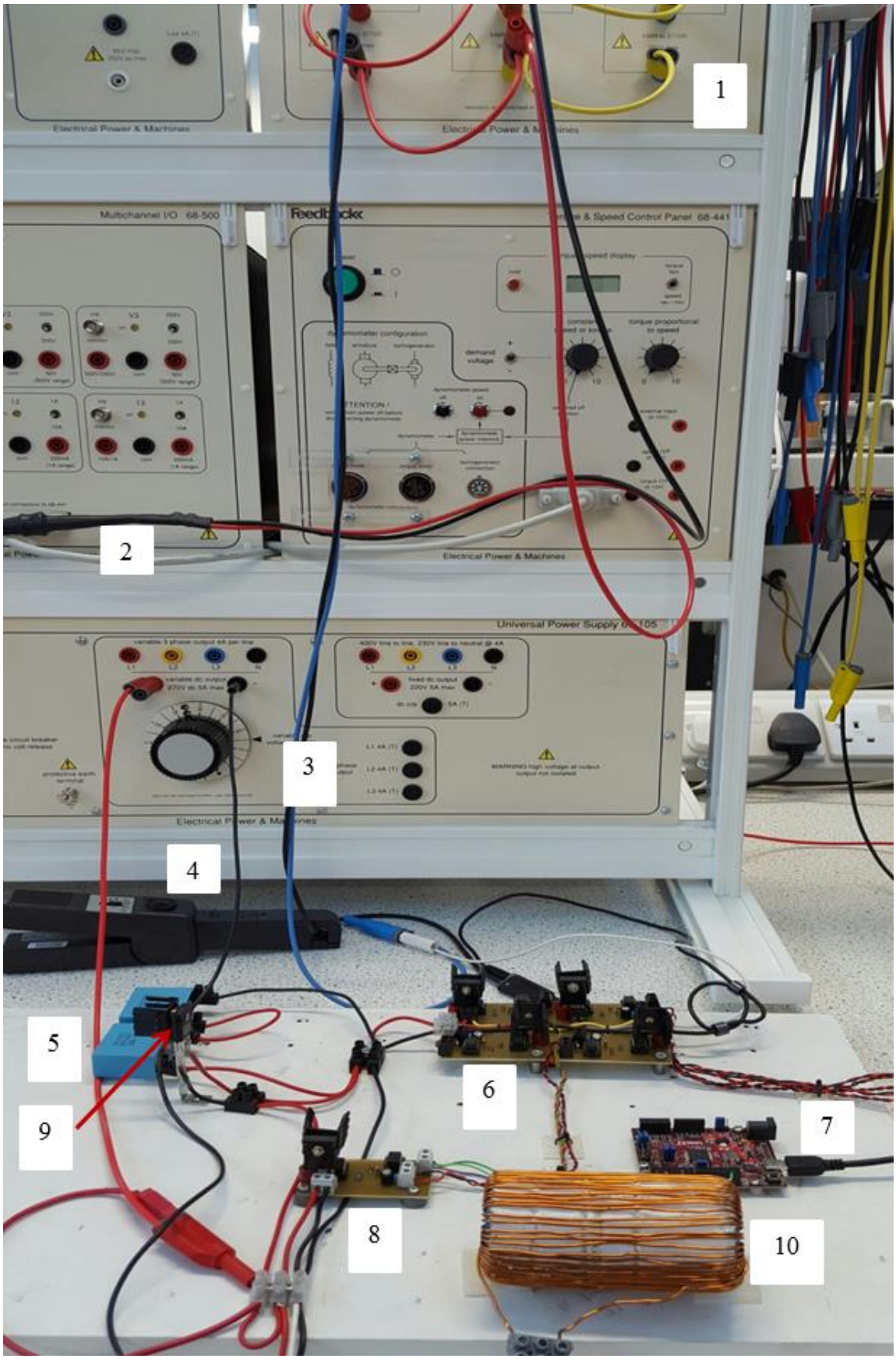


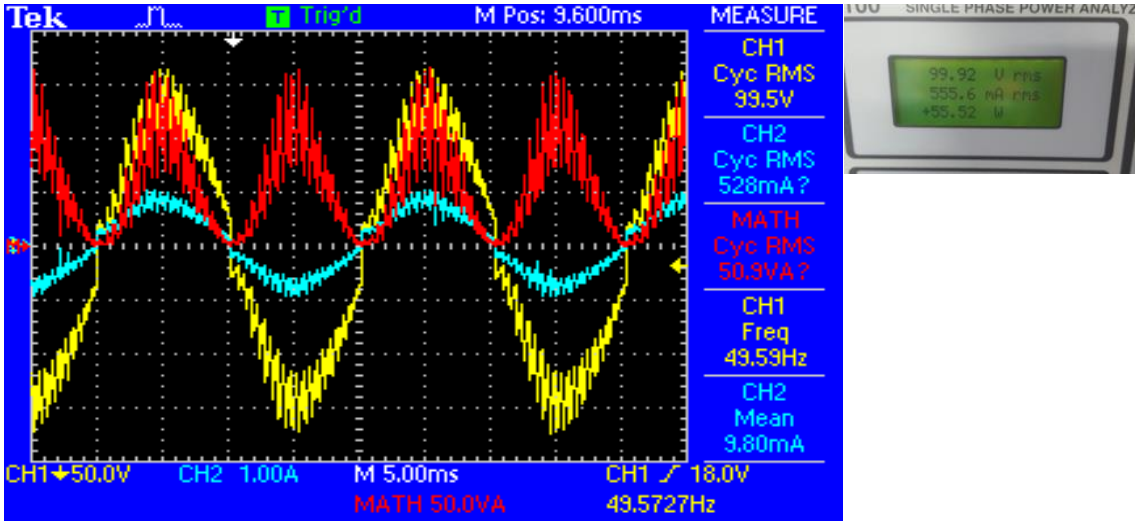
Fig. 6-1 The practical BBLFI circuit

6.3.2 Practical results

There are two different case studies for BBLFI circuit which are explained in this section. Also, there is finalising these two case studies in this section.

6.3.2.1 Case study 1 for BBLFI

Fig.6-2. Shows that the output voltage across the load is 300 volt peak to peak in case study1 from oscilloscope and single phase power analyser. The rms value of output voltage is 99.5 volts. The ripple voltage at peak value of the output is about 25 volts. The current in the output load is 2A peak to peak, the rms value is 528mA. The output power load is 50.9 W. The input power is about 55W, and then the efficiency of the circuit is 92.5%.



a b

Fig. 6-2 Output voltage across the load, load power and load current waveforms from BBLFI circuit. a) Oscilloscope results, b) power analyser results

Fig. 6-3 shows the FFT of the generated BBLFI waveform. The total harmonic distortion of the waveform is about 14.7%, the highest value of harmonic is 79^{th} and 81^{st} of FFT, which is the switching frequency of the boost converter. The value of fundamental voltage is 99.52V. The 5^{th}, 7^{th}, 9^{th} 11^{th} and 15^{th} Harmonics are less than 5% volt. The total harmonic distortion can be reduced to less than 1% if only the right value of inductance is applied to load side.

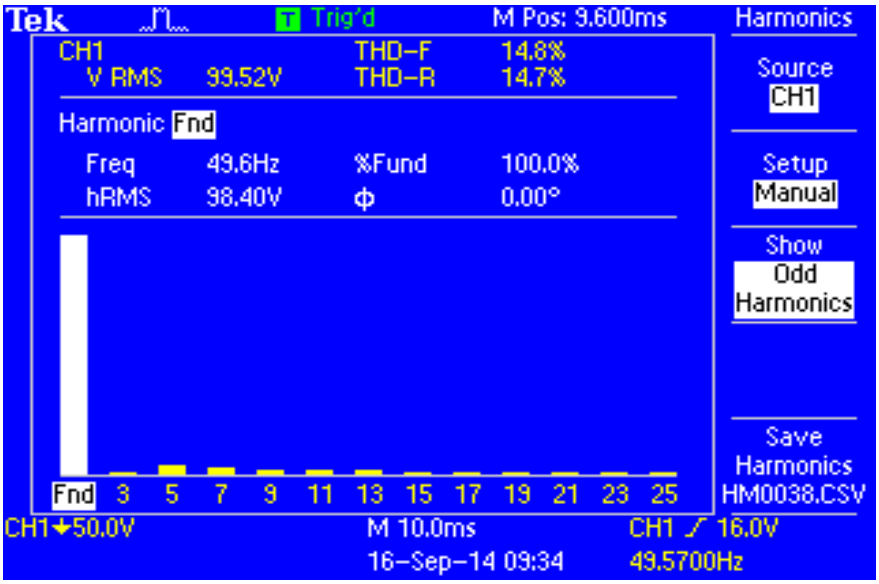


Fig. 6-3 The Fast Fourierr Transform of output voltage of BBLFI in case study1

6.3.2.2 Case study 2 for BBLFI

The case study 2 is to increase the voltage ratio of the proposed circuit from 0.66 (in case study1) to 1.66. The rms output voltage is 252 and the load current is 1.41A as shown in fig. 6-4. The voltage across of load is 800 peak to peak and current of the load is 4A peak to peak in this case. The voltage ripple for this case is 63 volts at maximum voltage. The output frequency is 50Hz which is same as H-bridge switching frequency.

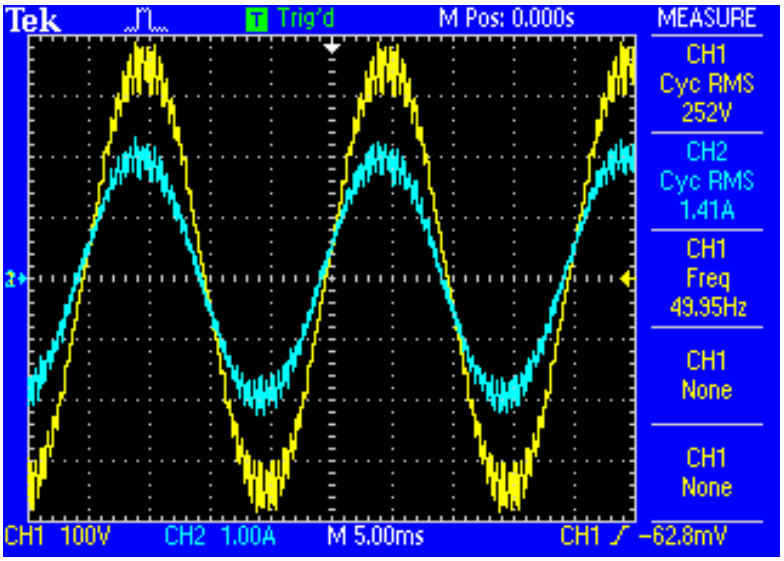


Fig. 6-4 The output voltage across of load and load current in BBLFI circuit

Fig.6-5 shows the FFT of H-bridge output voltage for case study 2. THD for this case is 7.26% of fundamental amplitude. All amplitude of low order harmonic are less than 1.5%.

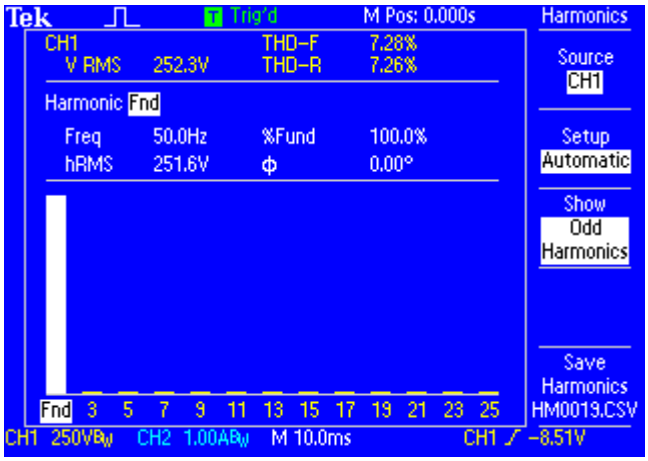


Fig. 6-5 FFT of output voltage of BBLFI circuit in case study 2.

6.3.2.3Finalising practical results of both case studies in BBLFI circuit

The switching frequency of main switch on BBLFI circuit 4 kHz for both cases. The first case BBLFI circuit operates as buck converter and voltage ripple is 25 volt at peak value. Also the switching pattern of this case is not optimised to reduce the amplitude of low order harmonics. However, the switching pattern of case 2 is optimised to reduce the amplitude of low order harmonic, which can reduce THD to 7.26%. The circuit of these two case studies is the same, the only differences between circuits of these cases is the value of capacitor which is increased two times in case 2 in comparison to case 1. The reason is to have voltage ripple 62.5 volts, which is 25% of the rms output voltage. The switching pattern of case study 2 is optimised to reduce 3^{rd}, 5^{th} and 7^{th} harmonic orders by DFT method. This method has three processes; first step is to increase output voltage by controlling M_a in Microcontroller by changing voltage in potential meter. Second step is to put output voltage in MATLAB and use DFT programmed code to optimise switching pattern of the controller. Last step is to apply a new optimised control signal to Micro controller. This method takes time to optimise which is a limitation of this case.

6.4Practical implemented of Boost-based Low Frequnecy Inverter

The practical components of BLFI circuit are the same with components of BBLFI circuit. The differences are switching pattern of DSPWM controller and connection of an inductor and diode in the current source power circuit. The H-bridge, capacitor and DC power supply are the same connection for both BBLFI and BLFI circuits.

6.4.1 Practical BLFI circuit

Fig 6-6 shows the built BLFI circuit, all parameters of this circuit is the same parameters which is shown in table 6-1. The DC voltage source connects to the inductor and inductor connects to diode and main switch (S_1) of the BLFI power circuit. The direction of the diode is changed in comparison to BBLFI circuit also the input direction of H-bridge is changed as well in BLFI circuit. The control signal of BLFI circuit is programmed in Arduino software and upload programmed code to Microcontroller UNO32.

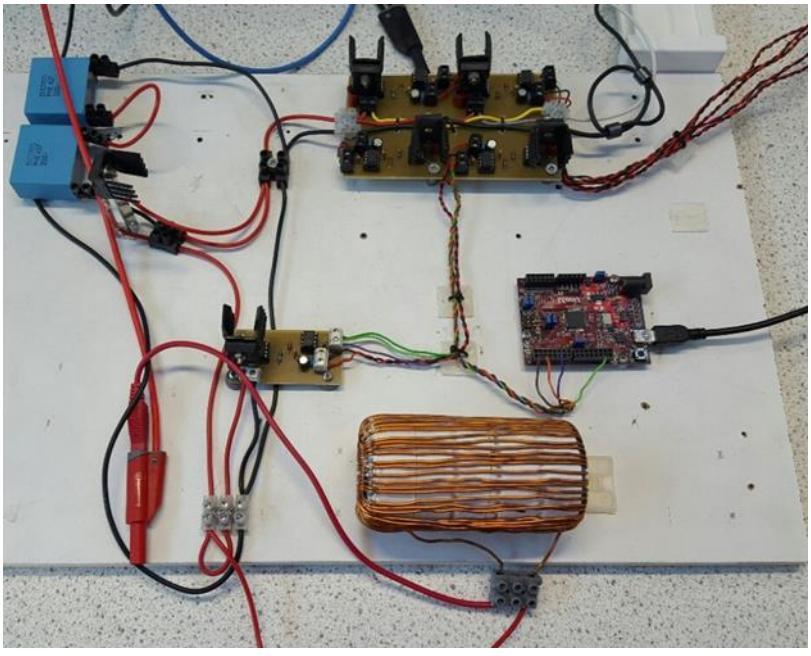


Fig. 6-6 Built BLFI circuit

6.4.2 Practical results of BLFI circuit

There are two case studies for BLFI circuit which are original output voltage and optimised output voltage.

6.4.2.1 Case study 1 for BLFI

Fig.6-7 shows the 50Hz output voltage of BLFI circuit which rms value is 254 volts. The voltage ratio for this case study is 1.7 which current source operates as boost converter. The voltage ripple for this case study is 130 volt and output voltage across of load is 780 volts peak to peak.

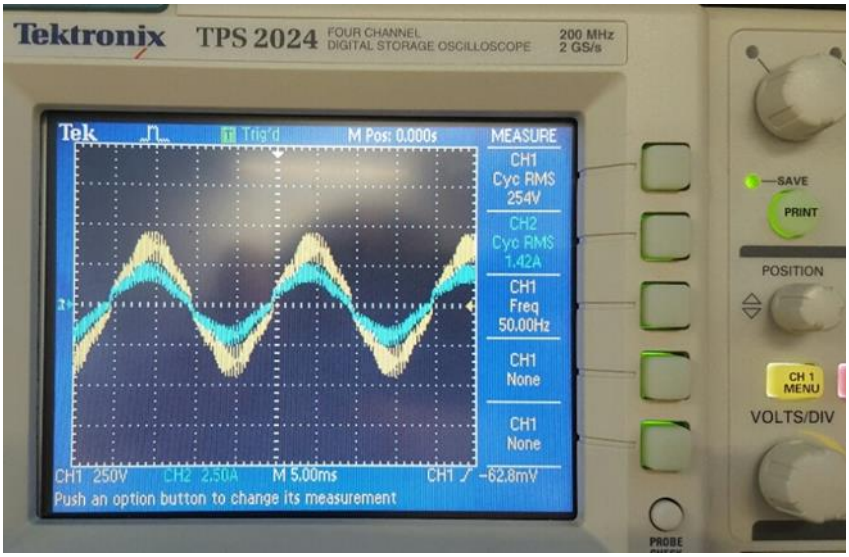


Fig. 6-7 Output voltage and current of BLFI circuit

Fig.6-8 shows FFT of original output current of BLFI circuit. The THD of output current is 14.7% of amplitude fundamental. The highest amplitude of harmonic orders is 79th and 81st, which are switching frequency (4 kHz) of main switch in BLFI circuit. The amplitude of low order harmonics is quite high in this case. The amplitudes of 5th, 7th and 13th harmonic order are 6.5%, 8% and 4% of fundamental value. These amplitudes of low order harmonics can be reduced to less than 1% by the optimising switching pattern of DSPWM control signal by the DFT method in MATLAB software.

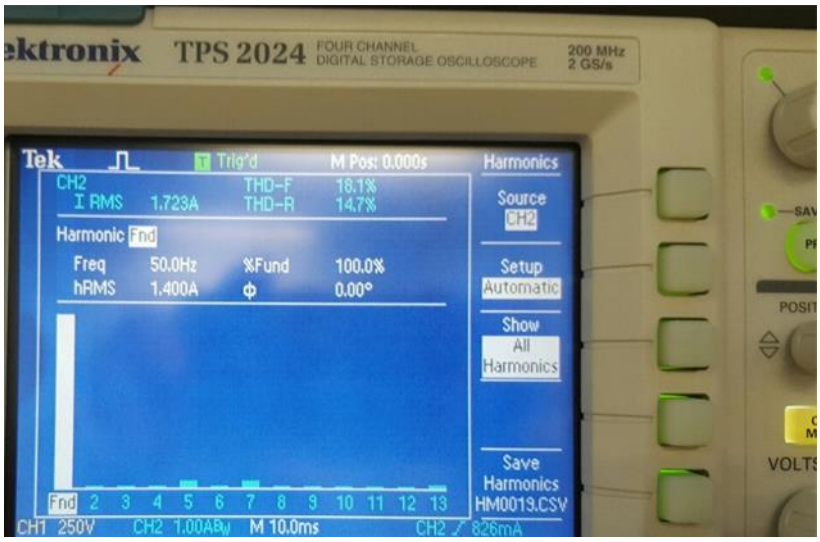


Fig. 6-8 FFT of load current of BLFI circuit

6.4.2.2 Prctical result of BLFI circuit in case study 2

Fig.6-9 shows the optimised output voltage and current of proposed circuit. The rms value of output voltage and current is 267volt and 1.5A in this case. The frequency of output is 50 Hz and voltage ripple is 70 volts at the peak value of the out voltage.

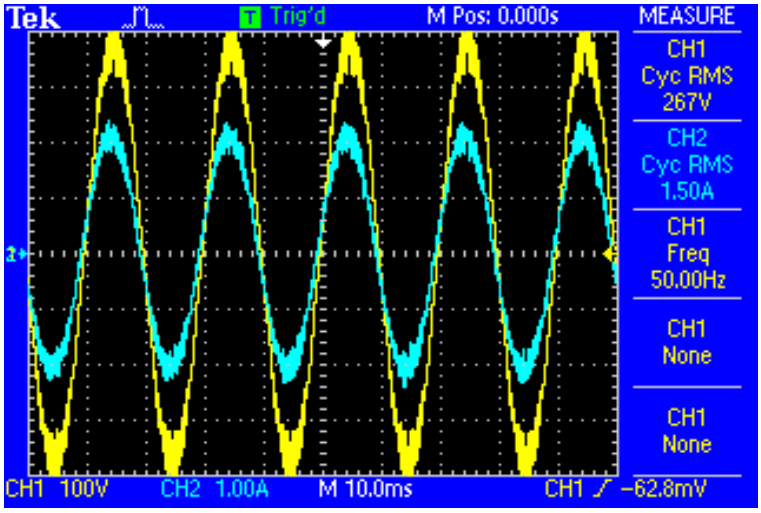


Fig. 6-9 Optimised output voltage and current of BLFI circuit

The FFT of optimised the output current in BLFI circuit is shown in fig. 6-10. This figure shows that amplitude of all low order harmonics is less than 1.5% of fundamental value. THD for this case study is 5.5%.

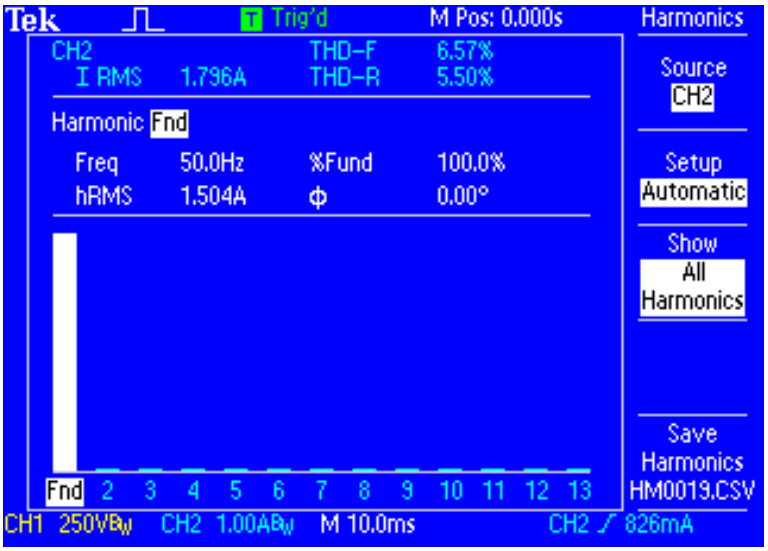


Fig. 6-10 FFT of optimised output current of proposed circuit

6.4.2.3Finalising practical results of BLFI circuit

The result of these two case studies shows the output voltage of BLFI circuit can easily control by DSPWM control signal. The output voltage ratio can be controlled by varying M_a in DSPWM control signal. There is implement limitation to increase the output voltage to more than 300 volts also safety limitation is another issue for not increasing voltage more than 300 Volt. However, this proposed circuit has the capability to increase voltage to 500 volts, which is a limitation voltage break of the MOSFET. The result of the second case study shows that this control signal has the capability to optimise switching pattern to reduce low order harmonics amplitude. This amplitude of low order harmonics becomes less than 1.5% by optimising switching pattern in comparison with case study 1. THD of this case study reduces to 5.5%, which is reduced 9% in comparison with the first case study. There are more practical results of BLFI circuit which is attached in Appendix C. These results show the capability of the BLFI circuit in different situation. The output frequency of these example result is from 30 Hz to 120Hz which depends on frequency of H-bridge switches frequency.

6.5 Practical test of Flyback-based Low Frequency Inverter

The FLFI circuit can build in the same way as two previous circuits (BBLFI and BLFI). This proposed circuit uses the same component parameter in table 6-1. The main difference from this circuit to the previous circuit (BLFI) is to replace the transformer to inductor of BLFI circuit.

6.5.1 Practical FLFI circuit

Fig 6-11 shows practical implement of FLFI circuit which transformer (T_1) is replaced to inductor in BLFI circuit. The transformer parameters for this proposed circuit is 7.9mH for primary winding inductance and secondary winding inductance is 24.5mH. The ratio of this transformer is 1.76. The transformer operates at least 4 kHz because this transformer is handmade and accuracy is not very high for lower frequency than 4 kHz. The primary winding connects to DC voltage source and single switch which is connected to negative of DC source. The secondary winding of this transformer connects to diode and H-bridge. The control signal of this proposed circuit is programmed and uploaded in Arduino UNO 32 Microcontroller.

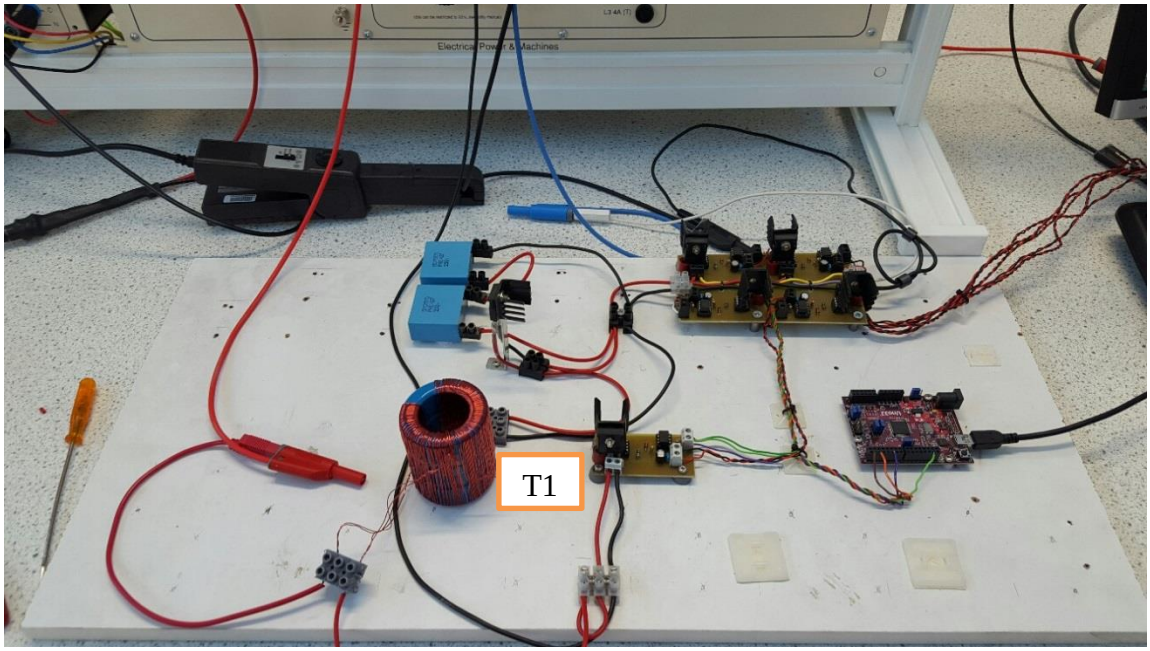


Fig. 6-11 Practical circuit of FLFI topology

6.5.2Practical results of FLFI circuit

The output frequency of proposed circuit is 60 Hz, which is the same switch frequency of H-bridge. The switching frequency of main switch in FLFI circuit is 4.8 kHz, which the M_f for this circuit is 80. There are two case studies for this proposed circuit which are original output voltage and optimised output voltage.

6.5.2.1 Practical Case study1 for FLFI circuit

The input DC voltage is 56volt which is shown by the pink colour in CH3 of Oscilloscope in fig6-13. The rms output voltage for this case study is 243 volts at 60 Hz which is shown in fig.6-12. This figure shows the output current of H-bridge which rms value is 1.35A. The voltage ratio of this proposed circuit is 4.34.

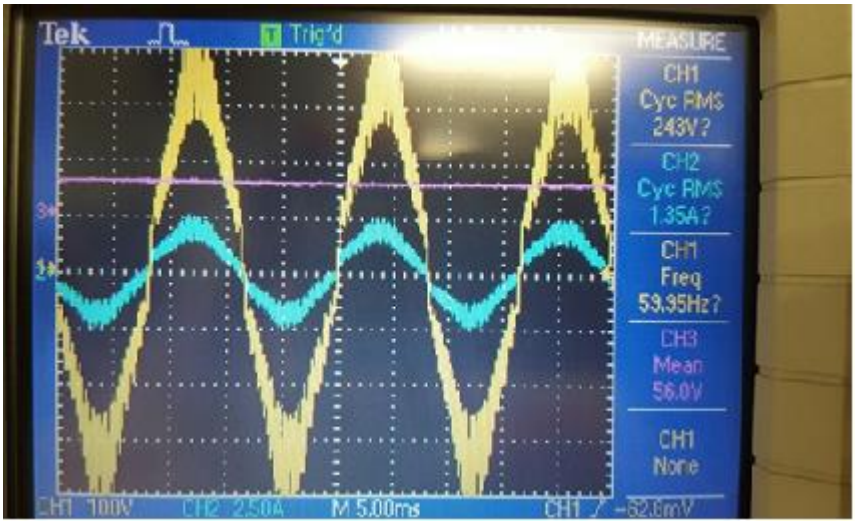


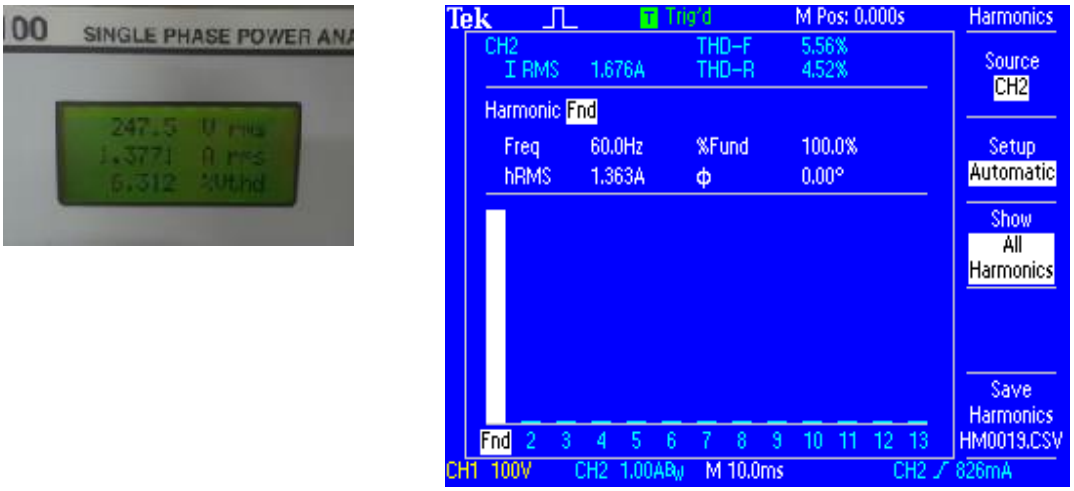
Fig. 6-12 original output voltage and current and DC input voltage

THD of the output current in FLFI is 13.5%, which is shown in fig. 6-13. The highest amplitude harmonic orders are switching frequency harmonic orders. The amplitudes of low order harmonic are 6%, 5% and 3% of fundamental value for 7^{th}, 5^{th} and 13^{th}.

Fig. 6-13 FFT of output current of FLFI circuit

6.5.2.2 Practical Case study 2 for FLFI circuit

Fig6-14.a) shows the rms value of optimised voltage and current from the FLFI circuit from the single phase power analyser. Fig 6-14.b) shows the FFT of optimised output current of FLFI circuit. All amplitude value of low order harmonic is reduced to less than 1% in FLFI circuit by optimising switching pattern. The THD of the output current for proposed circuit is 4.52% of fundamental value in Oscilloscope (fig6-14.b).



a b

Fig. 6-14 a) rms of optimised output voltage and current b)FFT of optimised output current of FLFI circuit

6.5.3 Finalising practical results of FLFI circuit

The results of FLFI show that proposed circuit has capability to control output voltage and frequency by varying M_a and M_f in DSPWM control signal. The output frequency of FLFI circuit could be 50Hz but the switching frequency should increase about 20%. The reason for this limitation is size of transformer which is used in this proposed circuit. The transformer needs to redesign for lower switching frequency, such as 2 kHz. This proposed circuit can have less THD in comparison to previous circuits (BBLFI and BLFI). The reason is use higher M_a with same voltage ratio in comparison to BBLFI and BLFI circuits. THD from power analyser in fig6-14.a is 6.312% of fundamental value which is different with THD from oscilloscope in fig6-14.b. The reason is the number of harmonic orders measurement in these two components.

6.6 BLFI circuit as Motor drive

The BLFI circuit tests as motor drive in this practical experiment. The BLFI circuit connects to 230volt single phase induction motor-capacitor start/induction run. The general specification of induction motor is shown in table 6-2.

Table 6.2 general specification of single phase induction motor

Items	**Description**
Brand	Feedback (64-110)
Power	Rated 250 W continuous
Rotates	Up to 2989 rpm at 50Hz
Power factor at full load	0.9

The motor drive and induction motor operate about 30 min without putting any load on it. Then every component is Ok then it starts to increase torque in induction motor by controlling potential meter in load controller. The power of the motor is increased by changing the power of load from the control panel of an induction motor (fig6-15). This figure shows the induction motor speed which is 2906 RPM at 50 Hz.

Fig. 6-15 The control torque panel of induction motor

The value of the capacitor in proposed circuit is 4.7µf which is not enough to correct power factor in load. The power factor of this induction motor with small load is 0.503. Fig.6-16 shows output voltage, output current and power factor of induction motor. The efficiency of motor drive is low which is about 50% because of low power factor in load.

Fig. 6-16 voltage across of load, current of load, Power factor of induction motor

The torque increases in induction motor which increases rotation power in shaft and then increase electrical power of induction motor. The output power of BLFI circuit reaches to 255 W which is the maximum power of induction motor. The power factor of induction motor is 0.85. This power factor can rise to 0.95 by parallel 10µF capacitor with H-bridge. Fig 6-17 shows output voltage, current, apparent power, real power and power factor. The capacitor is switched on from the panel in lab fig. 6-18 shows the capacitor bank in the lab.

a b c

Fig. 6-17 a) apparent power. b) Real power. c) Power factor

The 10µF capacitor is high for this induction motor to correct power factor in output, because of limitation of lab implement. This high value capacitor is leading current in this case study.

Fig. 6-18 Capacitorbanks

Fig 6-19 shows the current is leading of voltage is about 0.5ms. This figure shows the input voltage which is 56 V in this case. The voltage ratio of this motor drive is 4.07 and rms output voltage is 228V.

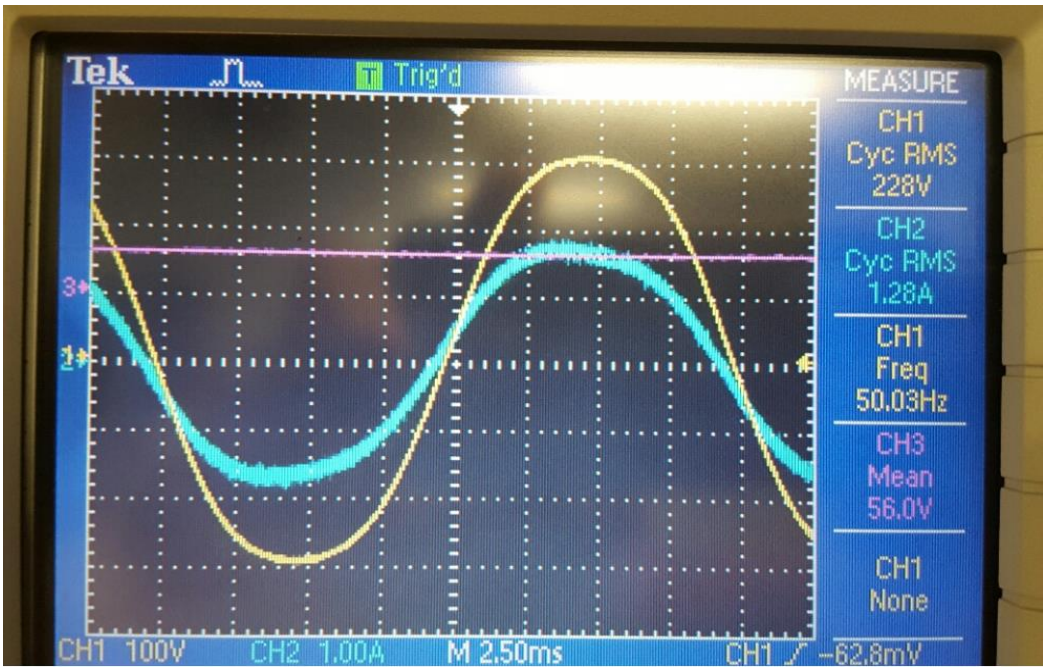


Fig. 6-19 input voltage, output voltage and output current

The high value capacitor increases the amplitude of 3rd harmonic in this case. Fig6-20 shows the FFT output current of proposed circuit. The amplitude of 3rd harmonic is 9.5% of fundamental value.

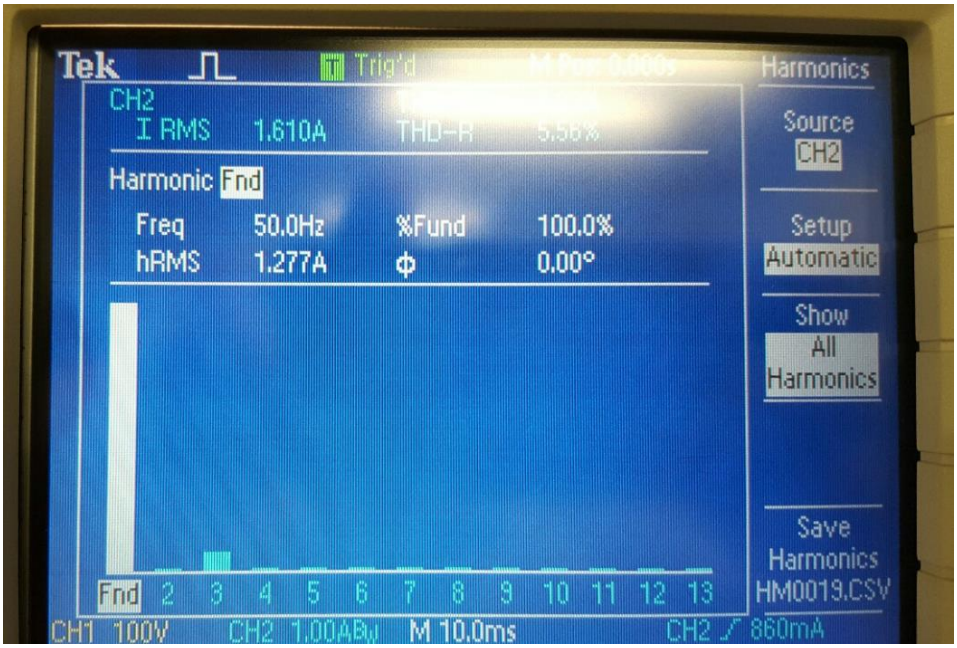


Fig. 6-20 FFT output current of induction motor drive

6.6.1Finalising induction motor driver

The result of induction motor drive shows that BLFI circuit can drive motor from DC voltage supply. The control signal of BLFI circuit is optimised to reduce the amplitude of low order harmonics. The capacitor bank can correct power factor in the system, but it is limitation to have bigger capacitor, which increases the amplitude of low order harmonic and decreases the power factor. There are more example of motor drive results in appendix C.

6.7 Practical Switching losses

The switching loss of the main switch of proposed circuits depends on current and voltage across of the MOSFET. Also the switching loss depends on MOSFET driver as well, which depends time turn on and turn off switch. So the faster MOSFET driver has less switching loss. Fig.2-21 shows the current oscillating in MOSFET which increases switching losses. This figure shows the current ripple when the switch is turned off. The inductance on system can cause this current ripple in MOSFET which depends on MOSFET driver size, length and size of wire.

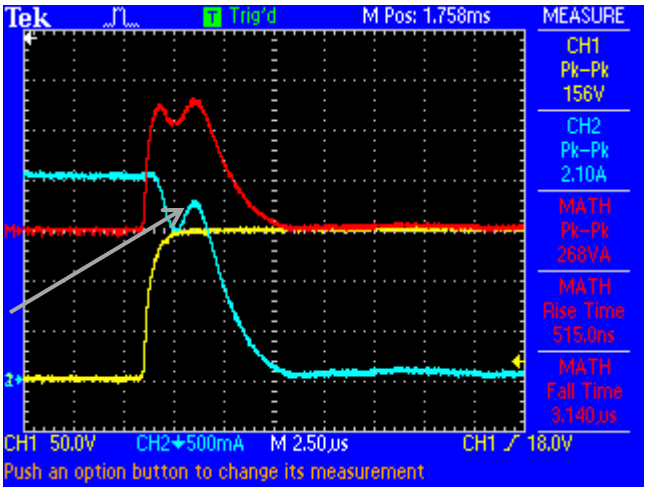
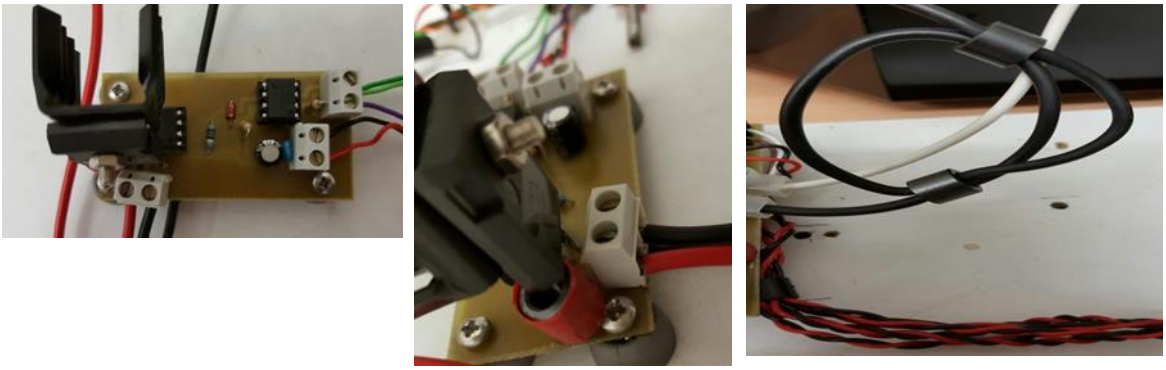


Fig. 6-21 voltage, current and power of turn off MOSFET

This oscillating current can reduce by designing and building the small size of MOSFET driver. Also ferrite ring toroid core can help to reduce this current ripple value in MOSFET which reduce switching losses in semiconductor switch. Also, this ferrite ring can suppress EMI in wire and system as well. Fig 6-22 shows the single MOSFET with ferrite ring, switch driver and ferrite ring on the wire. EMI can suppress by turning two times of wire on the ferrite ring as shown in fig.6-22c.



a b c

Fig. 6-22 a) single MOSFET and driver, b) ferrite ring on MOSFET driver, c) ferrite ring on wire

Fig.6-23 shows the current of MOSFET with no current oscillate when switch turns off. The ferrite ring reduces this current ripple which can reduce switching losses in the MOSFET.

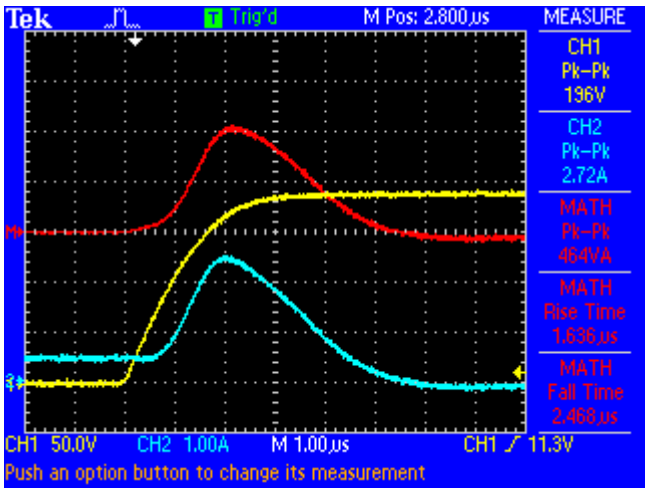


Fig. 6-23 turns off switching losses of MOSFET

Fig 2-25 shows an example of switching losses of MOSFET for 2A and 150 volts at 1 kHz switching frequency of BLFI circuit. A total energy loss for this MOSFET is 1.16mJ which is about 1.16W total switching losses. This total power loss is lower than calculation switching losses of MOSFET.

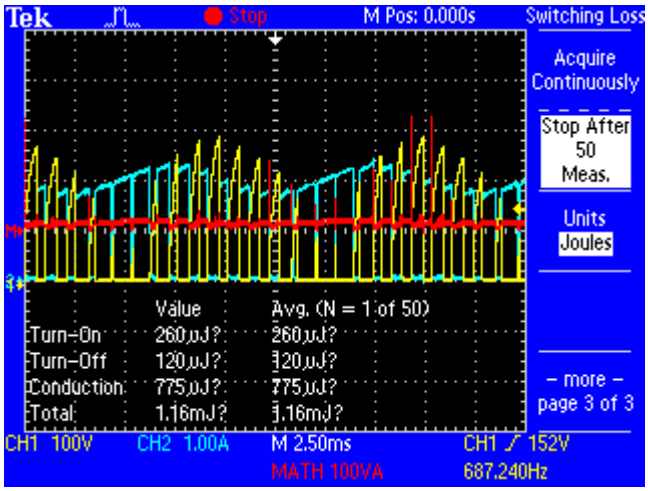


Fig. 6-24 switching losses of MOSFET

The total calculation switching losses of MOSFET is about 1.31W which is calculated from below equations.

From equation (4-4)

$$P_{sw(s1)} = \frac{1}{2} \times 2A \times 150V \times (5us) \times 1000 = 750mW$$

From equation (4-5)

$$P_{conducting\ loss\ (s1)} = 2^2 \times 0.14 = 560mW$$

Total switching losses =750mW+560mW=1.31W

This switching power loss increases 4 times by increase switching frequency to 4 kHz. Also, this switching loss increases where voltage and current of switch increase to have higher the output power. This switching loss is for any MOSFET or IGBT switches which are used in any DC to AC inverter topologies. There is a case study to compare different DC to AC inverter topologies in section 6-6.

6.8 Practical comparison between different DC to AC topologies

Table 6-3 shows a comparison between different types of DC to AC inverter circuits. These circuits are tested in practical implement under the same conditions without filters. The input voltage is 150 volt DC for Pulse Width Modulation (PWM), Cascade H-bridge (CHB), Neutral Point Clamped (NPC), BBLFI, BLFI and FLFI. The output voltages of all circuits are 250 volts in this case. So the rms output voltages are the same in each circuit. The load value for each circuit is 178Ω. The transformer is applied for each circuit except BBLFI and BLFI. The filter is not used in any of the circuits. It can be seen from the table that the efficiency of FLFI is higher than efficiency of other topologies. The THD of FLFI is less than THD in other topologies in this case-study.

Table 6.3 Comparison between different topologies

Type of dc to ac inverters	V_{in} V	I_{in} A	P_{in} W	V_{output}^{rms} V	I_{output}^{rms} A	P_{output} W	Efficiency	T.H.D %
PWM inverter	150	2.48	372	250	1.4	350	93%	76%
CHB (7 levels)	150	2.5	376	250	1.4	350	93%	18%
NPC (7 levels)	150	2.53	380	250	1.4	350	92%	20%
BBLFI	150	2.53	380	250	1.4	350	92%	7.26%
BLFI	150	2.5	376	250	1.4	350	93%	5.5%
FLFI	150	2.48	372	250	1.4	350	94%	4.52%

6.9 Discussion

The peak output voltage of the proposed circuits can be controlled to the same or larger value than the input voltage (DC source). The output voltage of the proposed circuits depends on hard devices (power devices) such as capacitor, inductance, type of

semiconductor (switches) and loads. Also the output voltages of proposed circuits depend on switching frequency of the current source from DSPWM control signal. Therefore the output voltage can be easily controlled through the control of the current source switching frequency and duty cycle in DSPWM control signal. The output frequency of BBLFI, BLFI and FLFI can be varied from 10 Hz to 2 kHz or more, which is dependent at limitation for power components, causing variation of the output voltage as well. The number of voltage level depends on the frequency used in the DSPWM frequency. The larger number of voltage levels in the BBLFI, BLFI and FLFI is proportion to the switching frequency of the current source.

Table.6-3 shows the comparison between results in this case study. The efficiency of practical circuit of proposed circuits is about 93%, so there are some losses in inductor and capacitor as well. There is not any power loss at inductor and capacitor in simulation part, because these components are a reactive component in simulation. So they do not have power loss in simulation.

Chapter 7 CONCLUSIONS AND FUTURE WORK

7.1 Summery

In this project a new inverter configuration is presented. It is based on stepping a DC voltage up and modulating the current source switch by a sinusoidal waveform. This waveform is then fed to an H-bridge which operates at 50Hz in order to reconstruct an AC waveform with low THD. The THD in the proposed topology is less than the THD in other inverter topologies and is also controllable, however, that could be at the expense of high switching losses. If the switching frequency is fixed in all other inverter configurations, the proposed circuits offer the less switching loses and this is due to the fact that only one switch (current source converter switch) operates at high frequency. The circuit is designed and then simulated on PSpice and a laboratory prototype is built to support the simulation results. It should be noted that there is no filter used in the final output in order to have a fair comparison between all inverter configurations. It is obvious that a small size of the filter will be required for a low THD.

7.2 Research contribution

There are very little in depth publications, which critically analyse inverter topology circuits. In chapter 2 of this thesis, an in depth literature review of different types of inverter topologies is presented. This has led into identifying a gap in thesis important research area and throughout the rest of the thesis a new topology is introduced in order to overcome the problem associated with present inverter circuits. The simulation and practical results show that this topology has some advantages in comparsion to 3-level and multilevel inverter topologies. The advantages of the proposed configuration over another inverter topologies can be summarised as:

- Less switching power loss in comparison to PWM inverter.
- The output voltage can be controlled through the switching frequency and the duty cycle of the main switch in the proposed circuit.
- This topology can be used as a soft start to run induction motor.
- This topology can be used as DC to AC inverter for renewable energy to achieve a maximum power point source.
- Lower cost, less number of power component.
- This topology does not need to use a transformer to step-up the output voltage, except FLFI circuit
- Topology of multilevel inverter based on current source converter.
- More capability than other voltage source multilevel inverter (VS-MLI).

The number of voltage levels at the output depends not on the number of DC sources, or the number of capacitors.

The output voltage and output frequency depend on the switching frequency. The voltage and frequency can be controlled in terms of the frequency and amplitude.

This topology of variable speed induction motor drive, which has more capability than other types of induction motor drives.

The voltage and frequency can be controlled using microcontroller, which can receive signals from different sensors in a closed loop fashion. This type of control system could be not complicated than a control system of other topologies.

7.3 Limitation

It is obvious that a current source configuration may add some complexity to the multilevel inverter, however the thesis examines the pros and cons of the proposed configuration. Initial results show that such new topology has many features, which can

be used in high power applications. In this thesis the switching frequency of the current source converter is chosen between 750 to 5 kHz and the output frequency of the proposed circuit is 10 to 2 kHz. At high frequency (above 5 kHz) the proposed circuit has more switching loss in comparison to the 3-level PWM inverters. Also the closed loop control system of this topology is very complicated, which needs to have more work on the closed loop control system. The control system of this topology for 3-phase inverter is very complicated and needs more investigation.

7.4 Future work

The control signal of proposed circuit can be a close loop system which can make the decision to constant output voltage in order to load's voltage requirement. This control close loop system needs to programme in Microcontroller by programmer engineering. This proposed circuit need to more research about nonlinear loads also this circuit needs more research for connecting to renewable energies. The output renewable energy power is not constant which depends on environment conduction. Then this proposed circuit needs to have more research to constant output voltage from the varying output voltage of renewable energy source by power point tracking.

This proposed circuit has the capability to have a higher power application in 3phases circuit. But 3 phase circuit is more complicated than single phase from the controller which needs to have more research how to connect switches in H-bridge. Also, three phase inverter needs to have more switches in current source in this topology which needs to redesign control signal for switching the main switch of the current source.

The most useful application of this proposed circuit is active filter for high power application to generate specific amplitude of harmonic orders.a\z

References

ADDA, R., MISHRA, S. and JOSHI, A., 2011. A PWM control strategy for switched boost inverter, *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE* 2011, IEEE, pp. 991-996.

AGORRETA, J.L., BORREGA, M., LÓPEZ, J. and MARROYO, L., 2011. Modeling and control of-paralleled grid-connected inverters with lcl filter coupled due to grid impedance in pv plants. *Power Electronics, IEEE Transactions on,* **26**(3), pp. 770-785.

ARMAN, M. and DARWISH, M., 2009. Critical Review of Cascaded H-Bridge Multilevel Inverter Topologies. *International Review of Electrical Engineering,* **4**(5),.

ARMAN, M., MAROUCHOS, C. and DARWISH, M., 2012. Self-tuning output passive-filter for low power DC/AC inverters, *Universities Power Engineering Conference (UPEC), 2012 47th International* 2012, IEEE, pp. 1-5.

ATLY, T.T. and AATHIRA, K., 2015a. Active buck-boost inverter for inverter air conditioner applications, *Electrical, Electronics, Signals, Communication and Optimization (EESCO), 2015 International Conference on* 2015a, IEEE, pp. 1-5.

ATLY, T.T. and AATHIRA, K., 2015b. Closed loop control of active buck-boost inverter for UPS applications, *Circuit, Power and Computing Technologies (ICCPCT), 2015 International Conference on* 2015b, IEEE, pp. 1-6.

ATMOPAWIRO, L., RACHMILDHA, T.D. and HAMDANI, D., 2012. Hybrid modeling of boost inverter using minimum ripple control, *Power Engineering and Renewable Energy (ICPERE), 2012 International Conference on* 2012, IEEE, pp. 1-5.

AXELROD, B., BERKOVICH, Y. and IOINOVICI, A., 2005. A cascade boost-switched-capacitor-converter-two level inverter with an optimized multilevel output waveform. *Circuits and Systems I: Regular Papers, IEEE Transactions on,* **52**(12), pp. 2763-2770.

AXELROD, B., BERKOVICH, Y. and IOINOVICI, A., 2004. A boost-switched capacitor-inverter with a multilevel waveform, *Circuits and Systems, 2004. ISCAS'04. Proceedings of the 2004 International Symposium on* 2004, IEEE, pp. V-884-V-887 Vol. 5.

AZLI, N. and BAKAR, M.S., 2004. A DSP-based regular sampled pulsewidth modulation (PWM) technique for a multilevel inverter, *Power System Technology, 2004. PowerCon 2004. 2004 International Conference on* 2004, IEEE, pp. 1613-1618.

BAI, Z., ZHANG, Z. and ZHANG, Y., 2007. A generalized three-phase multilevel current source inverter with carrier phase-shifted SPWM, *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE* 2007, IEEE, pp. 2055-2060.

BALAMURUGAN, C., NATARAJAN, S. and REVATHY, R., 2013. Analysis of Control Strategies for Diode Clamped Multilevel Inverter. *International Journal of Innovation and Applied Studies,* **3**(1), pp. 19-34.

BANAEI, M.R., DEHGHANZADEH, A.R., FAZEL, A. and OSKOUEI, A.B., 2013. Switching algorithm for single Z-source boost multilevel inverter with ability of voltage control. *IET Power Electronics,* **6**(7), pp. 1350-1359.

BAO, J.Y., BAO, W.B. and ZHANG, Z.C., 2011. A Generalized Three-Phase Multilevel Current-Source Inverter Topology, *Applied Mechanics and Materials* 2011, Trans Tech Publ, pp. 373-378.

BAO, J., BAO, W., ZHANG, Z. and FANG, W., 2009. A simple current-balancing method for a three-phase 5-level current-source inverter, *Industrial Electronics, 2009. IECON'09. 35th Annual Conference of IEEE* 2009, IEEE, pp. 104-108.

BARKATI, S., BAGHLI, L., BERKOUK, E.M. and BOUCHERIT, M., 2008. Harmonic elimination in diode-clamped multilevel inverter using evolutionary algorithms. *Electric Power Systems Research*, **78**(10), pp. 1736-1746.

BHAGWAT, P.M. and STEFANOVIĆ, V., 1983. Generalized structure of a multilevel PWM inverter. *Industry Applications, IEEE Transactions on*, (6), pp. 1057-1069.

BHATNAGAR, P. and NEMA, R., 2013. Maximum power point tracking control techniques: State-of-the-art in photovoltaic applications. *Renewable and Sustainable Energy Reviews*, **23**, pp. 224-241.

BINESH, N. and WU, B., 2011. 5-level parallel current source inverter for high power application with DC current balance control, *Electric Machines & Drives Conference (IEMDC), 2011 IEEE International* 2011, IEEE, pp. 504-509.

CACERES, R.O. and BARBI, I., 1999. A boost DC-AC converter: analysis, design, and experimentation. *Power Electronics, IEEE Transactions on*, **14**(1), pp. 134-141.

CANCELLIER, P., COLLI, V.D., DI STEFANO, R. and MARGNETTI, F., Transformerless voltage clamp circuit applied to a soft switched DC/AC current source inverter, *Power Electronics and Applications, 2005 European Conference on*, IEEE, pp. 8 pp.-P. 8.

CAO, L., LOO, K. and LAI, Y., Systematic Derivation of a Family of Output-Impedance Shaping Methods for Power Converters–A Case Study Using Fuel Cell-Battery-Powered Single-Phase Inverter System.

CHAKRABORTY, S., ANNIE, S.I. and RAZZAK, M., 2014. Design of single-stage buck and boost converters for photovoltaic inverter applications, *Informatics, Electronics & Vision (ICIEV), 2014 International Conference on* 2014, IEEE, pp. 1-6.

CHAKRABORTY, S., HASAN, W. and BAQUE BILLAH, S., 2014. Design and analysis of a transformer-less single-phase grid-tie photovoltaic inverter using boost converter with Immittance conversion topology, *Electrical Engineering and Information & Communication Technology (ICEEICT), 2014 International Conference on* 2014, IEEE, pp. 1-6.

CHAMARTHI, P., PRAGALLAPATI, N. and AGARWAL, V., 2014. Novel 1-ϕ multilevel current source inverter for balanced/unbalanced PV sources, *Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th* 2014, IEEE, pp. 3090-3093.

CHANG, Y., 2011. Design and analysis of multistage multiphase switched-capacitor boost DC–AC inverter. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, **58**(1), pp. 205-218.

CHEN, S., LIANG, T., YANG, L. and CHEN, J., 2013. A boost converter with capacitor multiplier and coupled inductor for AC module applications. *Industrial Electronics, IEEE Transactions on*, **60**(4), pp. 1503-1511.

CHEN, Y. and SMEDLEY, K., 2008. Three-phase boost-type grid-connected inverter. *Power Electronics, IEEE Transactions on*, **23**(5), pp. 2301-2309.

CHOWDHURY, A.S.K., CHAKRABORTY, S., SALAM, K. and RAZZAK, M., 2014. Design of a Single stage grid-connected buck-boost photovoltaic inverter for residential application, *Power and Energy Systems Conference: Towards Sustainable Energy, 2014* 2014, IEEE, pp. 1-6.

CHULAN, M.A. and YATIM, A.H.M., 2014. Design and implementation of a new H-bridge multilevel inverter for 7-level symmetric with less number of switches, *Power and Energy (PECon), 2014 IEEE International Conference on* 2014, IEEE, pp. 348-353.

CHUNXIA, G., LEI, Z. and LIXIA, Z., 2014. Research on specific integrated circuit of phase-shifting multilevel inverter PWM control, *Transportation Electrification Asia-Pacific (ITEC Asia-Pacific), 2014 IEEE Conference and Expo* 2014, IEEE, pp. 1-4.

COLAK, I., KABALCI, E. and BAYINDIR, R., 2011. Review of multilevel voltage source inverter topologies and control schemes. *Energy Conversion and Management,* **52**(2), pp. 1114-1128.

CORTES, J., SVIKOVIC, V., ALOU, P., OLIVER, J. and COBOS, J., 2014. v1 concept: designing a voltage mode control as current mode with near time-optimal response for Buck-type converters.

CORZINE, K., 2003. Operation and design of multilevel inverters. *Developed for the office of Naval research, ,* pp. 1-79.

DAHIDAH, M.S., KONSTANTINOU, G. and AGELIDIS, V.G., 2010. SHE-PWM and optimized DC voltage levels for cascaded multilevel inverters control, *Industrial Electronics & Applications (ISIEA), 2010 IEEE Symposium on* 2010, IEEE, pp. 143-148.

DASH, P.P. and KAZERANI, M., 2011. A multilevel current-source inverter based grid-connected photovoltaic system, *North American Power Symposium (NAPS), 2011* 2011, IEEE, pp. 1-6.

DIXON, J., PEREDA, J., CASTILLO, C. and BOSCH, S., 2010. Asymmetrical multilevel inverter for traction drives using only one DC supply. *Vehicular Technology, IEEE Transactions on,* **59**(8), pp. 3736-3743.

DRAXE, K.P., RANJANA, M.S.B. and PANDAV, K.M., 2014. A cascaded asymmetric multilevel inverter with minimum number of switches for solar applications, *Power and Energy Systems Conference: Towards Sustainable Energy, 2014* 2014, IEEE, pp. 1-6.

DU, Z., OZPINECI, B., TOLBERT, L.M. and CHIASSON, J.N., 2009. DC–AC cascaded H-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications. *Industry Applications, IEEE Transactions on,* **45**(3), pp. 963-970.

DU, Z., OZPINECI, B., TOLBERT, L.M. and CHIASSON, J.N., 2007. Inductorless DC-AC cascaded H-Bridge multilevel boost inverter for electric/hybrid electric vehicle applications, *Industry Applications Conference, 2007. 42nd IAS Annual Meeting. Conference Record of the 2007 IEEE* 2007, IEEE, pp. 603-608.

DUGGAPU, D.P., PULAVARTHI, S.V.K. and NULAKAJODU, S., 2013. Comparison between Diode Clamped and HBridge Multilevel Inverter (5 to 15 odd levels). *International Journal of Emerging Trends in Electrical and Electronics (IJETEE–ISSN: 2320-9569),* **1**(4), pp. 66-78.

EBADI, M., JOORABIAN, M. and MOGHANI, J.S., 2014. Voltage look-up table method to control multilevel cascaded transformerless inverters with unequal DC rail voltages. *Power Electronics, IET,* **7**(9), pp. 2300-2309.

ELSHEIKH, M.G., AHMED, M.E., ABDELKAREM, E. and ORABI, M., 2011. Single-phase five-level inverter with less number of power elements, *Telecommunications Energy Conference (INTELEC), 2011 IEEE 33rd International* 2011, IEEE, pp. 1-8.

GAJANAYAKE, C.J., LUO, F.L., GOOI, H.B., SO, P.L. and SIOW, L.K., 2010a. Extended-Boost-Source Inverters. *Power Electronics, IEEE Transactions on*, **25**(10), pp. 2642-2652.

GAJANAYAKE, C.J., LUO, F.L., GOOI, H.B., SO, P.L. and SIOW, L.K., 2010b. Extended-Boost-Source Inverters. *Power Electronics, IEEE Transactions on*, **25**(10), pp. 2642-2652.

GEORGAKAS, K.G., VOVOS, P.N. and VOVOS, N., 2014. Harmonic reduction method for a single-phase DC–AC converter without an output filter. *Power Electronics, IEEE Transactions on*, **29**(9), pp. 4624-4632.

GUAN, E., SONG, P., YE, M. and WU, B., 2005. Selective harmonic elimination techniques for multilevel cascaded H-bridge inverters, *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on* 2005, IEEE, pp. 1441-1446.

GUEDOUANI, R., FIALA, B., BERKOUK, E. and BOUCHERIT, M., 2011. Modeling and control of multilevel three-phase PWM current source inverter, *Electrical Machines and Power Electronics and 2011 Electromotion Joint Conference (ACEMP), 2011 International Aegean Conference on* 2011, IEEE, pp. 455-460.

GUEDOUANI, R., FIALA, B. and BOUCHERIT, M., 2013. New PWM control strategy for multilevel three—Phase current source inverter, *Power Engineering, Energy and Electrical Drives (POWERENG), 2013 Fourth International Conference on* 2013, IEEE, pp. 709-714.

GUPTA, A.K. and KHAMBADKONE, A.M., 2005. A general space vector PWM algorithm for multilevel inverters, including operation in overmodulation range, *Electric Machines and Drives, 2005 IEEE International Conference on* 2005, IEEE, pp. 1437-1444.

GÚRPIDE, P.S., SÁDABA, O.A., PALOMO, L.M., MEYNARD, T. and LEFEUVRE, E., 2001. A new control strategy for the boost DC-AC inverter, *Power Electronics Specialists Conference* 2001, pp. 974-979.

HAGH, M.T., TAGHIZADEH, H. and RAZI, K., 2009. Harmonic minimization in multilevel inverters using modified species-based particle swarm optimization. *Power Electronics, IEEE Transactions on*, **24**(10), pp. 2259-2267.

HASAN, M., MEKHILEF, S. and AHMED, M., 2014. Three-phase hybrid multilevel inverter with less power electronic components using space vector modulation. *IET Power Electronics*, **7**(5), pp. 1256-1265.

HAUKE, B., 2009. Basic calculation of a boost converter's power stage. *Texas Instruments: Application Report [online]*, .

HO, A., CHUN, T. and KIM, H., 2015. Extended Boost Active-Switched-Capacitor/Switched-Inductor Quasi-Z-Source Inverters.

HOTHONGKHAM, P. and KINNARES, V., 2007. Investigation into harmonic losses in a PWM multilevel cascaded H-bridge inverter fed induction motor, *Power Electronics and Drive Systems, 2007. PEDS'07. 7th International Conference on* 2007, IEEE, pp. 1043-1048.

HU, S., ZHANG, Z., LI, Y., LUO, L., LUO, P., CAO, Y., CHEN, Y., ZHOU, G., WU, B. and CHRISTIAN, R., 2015. A New Railway Power Flow Control System Coupled with Asymmetric Double LC Branches.

HUANG, J. and CORZINE, K., 2006. Extended operation of flying capacitor multilevel inverters. *Power Electronics, IEEE Transactions on*, **21**(1), pp. 140-147.

JAMALUDIN, J., RAHIM, N.A. and PING, H.W., 2014. Multilevel voltage source inverter with optimised usage of bidirectional switches. *IET Power Electronics,* **8**(3), pp. 378-390.

JANG, M. and AGELIDIS, V.G., 2011. A minimum power-processing-stage fuel-cell energy system based on a boost-inverter with a bidirectional backup battery storage. *Power Electronics, IEEE Transactions on,* **26**(5), pp. 1568-1577.

JANG, M., CIOBOTARU, M. and AGELIDIS, V.G., 2013. A single-phase grid-connected fuel cell system based on a boost-inverter. *Power Electronics, IEEE Transactions on,* **28**(1), pp. 279-288.

KABALCI, E., COLAK, I., BAYINDIR, R. and PAVLITOV, C., 2011. Modelling a 7-level asymmetrical H-bridge multilevel inverter with PS-SPWM control, *Electrical Machines and Power Electronics and 2011 Electromotion Joint Conference (ACEMP), 2011 International Aegean Conference on* 2011, IEEE, pp. 578-583.

KALASHANI, M.B. and FARSADI, M., 2014. A new switched-capacitors boost inverter for renewable energy sources and POD control modulation, *Electrical Engineering (ICEE), 2014 22nd Iranian Conference on* 2014, IEEE, pp. 636-641.

KANCHAN, R., BAIJU, M., MOHAPATRA, K., OUSEPH, P. and GOPAKUMAR, K., 2005. Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages, *Electric Power Applications, IEE Proceedings*- 2005, IET, pp. 297-309.

KANG, D., LEE, Y., SUH, B., CHOI, C. and HYUN, D., 2003. An improved carrier-based SVPWM method using leg voltage redundancies in generalized cascaded multilevel inverter topology. *Power Electronics, IEEE Transactions on,* **18**(1), pp. 180-187.

KANG, F., PARK, S., KIM, C. and CHO, S.E., 2004. Half-bridge and full-bridge cell based multilevel PWM inverter with cascaded transformers, *Circuits and Systems, 2004. MWSCAS'04. The 2004 47th Midwest Symposium on* 2004, IEEE, pp. II-273-II-276 vol. 2.

KANIMOZHI, M. and GEETHA, P., 2014a. A new boost switched capacitor multilevel inverter using different multi carrier PWM techniques, *Circuit, Power and Computing Technologies (ICCPCT), 2014 International Conference on* 2014a, IEEE, pp. 432-437.

KANIMOZHI, M. and GEETHA, P., 2014b. A new boost switched capacitor multilevel inverter using different multi carrier PWM techniques, *Circuit, Power and Computing Technologies (ICCPCT), 2014 International Conference on* 2014b, IEEE, pp. 432-437.

KJAER, S.B., PEDERSEN, J.K. and BLAABJERG, F., 2005. A review of single-phase grid-connected inverters for photovoltaic modules. *Industry Applications, IEEE Transactions on,* **41**(5), pp. 1292-1306.

KOURO, S., BERNAL, R., MIRANDA, H., RODRÍGUEZ, J. and PONTT, J., 2006. Direct torque control with reduced switching losses for asymmetric multilevel inverter fed induction motor drives, *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE* 2006, IEEE, pp. 2441-2446.

KOUSHKI, B., KHALILINIA, H., GHAISARI, J. and NEJAD, M.S., 2008. A new three-phase boost inverter: Topology and controller, *Electrical and Computer Engineering, 2008. CCECE 2008. Canadian Conference on* 2008, IEEE, pp. 000757-000760.

KUMAR, J., DAS, B. and AGARWAL, P., 2008. Selective harmonic elimination technique for a multilevel inverter. *space,* **1**, pp. 3.

KWAK, S. and KIM, T., 2009. An integrated current source inverter with reactive and harmonic power compensators. *Power Electronics, IEEE Transactions on,* **24**(2), pp. 348-357.

LAKSHMI, T., GEORGE, N., UMASHANKAR, S. and KOTHARI, D., 2013. Cascaded seven level inverter with reduced number of switches using level shifting PWM technique, *Power, Energy and Control (ICPEC), 2013 International Conference on* 2013, IEEE, pp. 676-680.

LAW, K.H. and DAHIDAH, M.S., 2014. DC-DC boost converter based MSHE-PWM cascaded multilevel inverter control for STATCOM systems, *Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA), 2014 International* 2014, IEEE, pp. 1283-1290.

LEI, Q. and PENG, F.Z., 2014. Space Vector Pulsewidth Amplitude Modulation for a Buck–Boost Voltage/Current Source Inverter. *Power Electronics, IEEE Transactions on*, **29**(1), pp. 266-274.

LEI, Q., PENG, F.Z. and SHEN, M., 2013. Switched-coupled-inductor inverter, *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE* 2013, IEEE, pp. 5280-5287.

LEI, Q., WANG, B. and PENG, F.Z., 2012. Unified space vector PWM control for current source inverter, *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* 2012, IEEE, pp. 4696-4702.

LI, J., LIU, J. and LIU, J., 2009. Comparison of Z-source inverter and traditional two-stage boost-buck inverter in grid-tied renewable energy generation, *Power Electronics and Motion Control Conference, 2009. IPEMC'09. IEEE 6th International* 2009, IEEE, pp. 1493-1497.

LI, L., CZARKOWSKI, D., LIU, Y. and PILLAY, P., 2000. Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters. *Industry Applications, IEEE Transactions on*, **36**(1), pp. 160-170.

LI, Y., ANDERSON, J., PENG, F.Z. and LIU, D., 2009. Quasi-Z-source inverter for photovoltaic power generation systems, *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE* 2009, IEEE, pp. 918-924.

LIU, H., TOLBERT, L.M., KHOMFOI, S., OZPINECI, B. and DU, Z., 2008. Hybrid cascaded multilevel inverter with PWM control method, *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* 2008, IEEE, pp. 162-166.

LIU, Y. and LUO, F.L., 2008. Trinary hybrid 81-level multilevel inverter for motor drive with zero common-mode voltage. *Industrial Electronics, IEEE Transactions on*, **55**(3), pp. 1014-1021.

LOPATKIN, N.N., 2011. Three-phase transformerless boost multilevel inverter with one DC voltage source, *2011 International Conference and Seminar on Micro/Nanotechnologies and Electron Devices Proceedings* 2011.

LUO, F.L., 2007. DC/DC Conversion Technique and Twelve Series Luo-converters.

LUO, F.L. and YE, H., 2010. *Power electronics: advanced conversion technologies.* CRC Press.

LUO, F.L. and YE, H., 2003. Positive output super-lift converters. *Power Electronics, IEEE Transactions on*, **18**(1), pp. 105-113.

MA, M., HE, X., CAO, W., SONG, X. and JI, B., 2015. Optimised phase disposition pulse-width modulation strategy for hybrid-clamped multilevel inverters using switching state sequences. *IET Power Electronics*, .

MADOUH, J., AHMED, N.A. and AL-KANDARI, A.M., 2012. Advanced power conditioner using sinewave modulated buck–boost converter cascaded polarity changing inverter. *International Journal of Electrical Power & Energy Systems*, **43**(1), pp. 280-289.

MALAD, C.P. and RAO, K.U., 2012. Simulation of a buck-boost single phase voltage source inverter for distribution generation systems. *Int.J.Modern Eng.Res*, **2**(5), pp. 3628-3632.

MALINOWSKI, M., GOPAKUMAR, K., RODRIGUEZ, J. and PEREZ, M.A., 2010. A survey on cascaded multilevel inverters. *Industrial Electronics, IEEE Transactions on*, **57**(7), pp. 2197-2206.

MARCOS-PASTOR, A., VIDAL-IDIARTE, E., CID-PASTOR, A. and MARTINEZ-SALAMERO, L., 2014. Loss-Free Resistor-based Power Factor Correction using a Semi-bridgeless Boost Rectifier in Sliding-Mode Control.

MAROUCHOS, C., DARWISH, M. and DIOMIDOU, L., 2013. A new concept for a multilevel switched capacitor sinusoidal grid connected inverter, *Power Engineering Conference (UPEC), 2013 48th International Universities'* 2013, IEEE, pp. 1-6.

MAROUCHOS, C., XENOFONTOS, D., DARWISH, M., MOGHADAM, M. and ARMEFTI, C., 2014. The switched capacitor inverter as a MPPT in a photovoltaic application, *Power Engineering Conference (UPEC), 2014 49th International Universities* 2014, IEEE, pp. 1-4.

MCGRATH, B.P., HOLMES, D.G. and LIPO, T., 2003. Optimized space vector switching sequences for multilevel inverters. *Power Electronics, IEEE Transactions on*, **18**(6), pp. 1293-1301.

MOGHADAM, M.S. and DARWISH, M., 2012. A buck/boost based Multilevel inverter topology for UPEC2012 conference proceeding, *2012 47th International Universities Power Engineering Conference (UPEC)* 2012.

MOGHADAM, M., DARWISH, M. and MAROUCHOS, C., 2013. A simple drive induction motor based on buck/boost inverter topology, *Power Engineering Conference (UPEC), 2013 48th International Universities'* 2013, IEEE, pp. 1-4.

MOSAZADEH, S., FATHI, S. and RADMANESH, H., 2012. New high frequency switching method of cascaded multilevel inverters in PV application, *Power Engineering and Renewable Energy (ICPERE), 2012 International Conference on* 2012, IEEE, pp. 1-6.

MURUGESAN, M., SIVARANJANI, S., ASOKKUMAR, G. and SIVAKUMAR, R., 2011. Seven level modified cascaded inverter for induction motor drive applications. *Journal of Information Engineering and Applications*, **1**(1), pp. 63-45.

MUTHUKUMAR, E., SANKAR, T., SARAVANAKUMAR, R. and RAMAKRISHNAN, A., 2015. A NEW MULTI LEVEL INVERTER TOPOLOGY FOR GRID INTERCONNECTION OF PV SYSTEMS. *Int.J.Engg.Res.& Sci.& Tech*, **240**.

NARIMANI, M., WU, B., TIAN, K., CHENG, Z. and ZARGARI, N.R., 2014. A new H-bridge NNPC converter for 10kV class motor drives, *Industrial Electronics Society, IECON 2014-40th Annual Conference of the IEEE* 2014, IEEE, pp. 1067-1071.

NAVABALACHANDRU, C., ASHOK, B., JAGADEESAN, A. and RAJA, R., 2013. Performance of variable frequency ISPWM technique for a cascaded multilevel inverter, *Energy Efficient Technologies for Sustainability (ICEETS), 2013 International Conference on* 2013, IEEE, pp. 611-616.

NEDUMGATT, J.J., VIJAYAKUMAR, D., KIRUBAKARAN, A. and UMASHANKAR, S., 2012. A multilevel inverter with reduced number of switches, *Electrical, Electronics and Computer Science (SCEECS), 2012 IEEE Students' Conference on* 2012, IEEE, pp. 1-4.

NG, N., TU, T.N.K., THANH, H.Q. and LEE, H., 2014a. A reduced switching loss PWM strategy to eliminate common mode voltage in multilevel inverters, *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* 2014a, IEEE, pp. 219-226.

NG, N., TU, T.N.K., THANH, H.Q. and LEE, H., 2014b. A reduced switching loss PWM strategy to eliminate common mode voltage in multilevel inverters, *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* 2014b, IEEE, pp. 219-226.

NGUYEN, N.K., NGUYEN, T. and LEE, H., 2015a. A Reduced Switching Loss PWM Strategy to Eliminate Common Mode Voltage In Multilevel Inverters.

NGUYEN, N.K., NGUYEN, T. and LEE, H., 2015b. A Reduced Switching Loss PWM Strategy to Eliminate Common Mode Voltage In Multilevel Inverters.

NGUYEN, N., NGUYEN, B. and LEE, H., 2011. An optimized discontinuous PWM method to minimize switching loss for multilevel inverters. *Industrial Electronics, IEEE Transactions on*, **58**(9), pp. 3958-3966.

NHO, N.V., CONG, T.T. and LEE, H., 2007. Carrier based two-state PWM method for optimising voltage error in multilevel inverters, *Power Electronics, 2007. ICPE'07. 7th Internatonal Conference on* 2007, IEEE, pp. 581-586.

NISHA, K. and JAIN, S., 2015. PV powered performance enhanced three-stage cascaded quasi Z-source inverter fed induction motor drive, *Circuit, Power and Computing Technologies (ICCPCT), 2015 International Conference on* 2015, IEEE, pp. 1-7.

NORDVALL, A., 2011. Multilevel inverter topology survey.

OZPINECI, B., TOLBERT, L.M. and CHIASSON, J.N., 2004. Harmonic optimization of multilevel converters using genetic algorithms, *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual* 2004, IEEE, pp. 3911-3916.

PENG, F.Z., 2003. Z-source inverter. *Industry Applications, IEEE Transactions on*, **39**(2), pp. 504-510.

PENG, F.Z., SHEN, M. and QIAN, Z., 2005. Maximum boost control of the Z-source inverter. *IEEE Transactions on power electronics*, **20**(4), pp. 833-838.

PRASADARAO, K., SUDHA RANI, P. and TABITA, G., 2014. A new multi level inverter topology for grid interconnection of PV systems, *Power and Energy Systems Conference: Towards Sustainable Energy, 2014* 2014, IEEE, pp. 1-5.

PRASHANTH, N., KUMAR, B., YADAGIRI, J. and DASGUPTA, A., 2011. Harmonic Minimization in Multilevel Inverter by using PSO. *ACEEE Int.J.on Control System and Instrumentation*, **2**(03),.

QIN, Z., SHA, D. and LIAO, X., 2012. A three-phase boost-type grid-connected inverter based on synchronous reference frame control, *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE* 2012, IEEE, pp. 384-388.

RAHNAMAEE, A. and MAZUMDER, S.K., 2014. A Soft-Switched Hybrid-Modulation Scheme for a Capacitor-Less Three-Phase Pulsating-DC-Link Inverter. *Power Electronics, IEEE Transactions on*, **29**(8), pp. 3893-3906.

RANJAN, A., GUPTA, K.K., KUMAR, L. and JAIN, S., 2012. A switched-capacitors based multilevel boost inverter with single input source, *Power Electronics (IICPE), 2012 IEEE 5th India International Conference on* 2012, IEEE, pp. 1-6.

RANJANA, M.S.B., MAROTI, P.K. and REVATHI, B., 2014. A novel single phase multilevel inverter with single photovoltaic source and less number of switches, *Devices, Circuits and Systems (ICDCS), 2014 2nd International Conference on* 2014, IEEE, pp. 1-6.

RAVINDRANATH, A., MISHRA, S.K. and JOSHI, A., 2013. Analysis and PWM control of switched boost inverter. *Industrial Electronics, IEEE Transactions on*, **60**(12), pp. 5593-5602.

RAY, R., CHATTERJEE, D. and GOSWAMI, S.K., 2009. Harmonics elimination in a multilevel inverter using the particle swarm optimisation technique. *Power Electronics, IET*, **2**(6), pp. 646-652.

RODRIGUEZ, J., LAI, J. and PENG, F.Z., 2002. Multilevel inverters: a survey of topologies, controls, and applications. *Industrial Electronics, IEEE Transactions on*, **49**(4), pp. 724-738.

SAGHALEINI, M. and MIRAFZAL, B., 2012. Reactive power control in three-phase grid-connected current source boost inverter, *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE* 2012, IEEE, pp. 904-910.

SALEHI, R., FAROKHNIA, N., ABEDI, M. and FATHI, S.H., 2011. Elimination of low order harmonics in multilevel inverters using genetic algorithm. *Journal of power electronics*, **11**(2), pp. 132-139.

SANCHIS, P., GUBÍA, E. and MARROYO, L., 2005. Design and experimental operation of a control strategy for the buck-boost DC-AC Inverter, *Electric Power Applications, IEE Proceedings*- 2005, IET, pp. 660-668.

SANCHIS, P., URSÆA, A., GUBÍA, E. and MARROYO, L., 2005. Boost DC-AC inverter: a new control strategy. *Power Electronics, IEEE Transactions on*, **20**(2), pp. 343-353.

SATO, Y., KAWASAKI, M. and ITO, T., 2011a. A diode-clamped multilevel inverter with voltage boost function, *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on* 2011a, IEEE, pp. 1987-1991.

SATO, Y., KAWASAKI, M. and ITO, T., 2011b. A diode-clamped multilevel inverter with voltage boost function, *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on* 2011b, IEEE, pp. 1987-1991.

SEKHAR, K.C. and DAS, G., 2006. Five-level SPWM Inverter for an Induction Motor with Open-end Windings, *Power and Energy Conference, 2006. PECon'06. IEEE International* 2006, IEEE, pp. 342-347.

SHAHALAMI, S. and DAMIROF, A.M., 2012. Implementation of variable-speed asynchronous drive fed by current source inverter, *Power Electronics and Drive Systems Technology (PEDSTC), 2012 3rd* 2012, IEEE, pp. 206-211.

SHEN, M., JOSEPH, A., WANG, J., PENG, F.Z. and ADAMS, D.J., 2007. Comparison of traditional inverters and Z-source inverter for fuel cell vehicles. *Power Electronics, IEEE Transactions on*, **22**(4), pp. 1453-1463.

SHUKLA, A., GHOSH, A. and JOSHI, A., 2012. Control of dc capacitor voltages in diode-clamped multilevel inverter using bidirectional buck–boost choppers. *IET Power Electronics*, **5**(9), pp. 1723-1732.

SINGH, P., TIWARI, S. and GUPTA, K., 2012. A new topology of transistor clamped 5-level H-Bridge multilevel inverter with voltage boosting capacity, *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on* 2012, IEEE, pp. 1-5.

SRUTHI, C. and SARITHA, P., 2014. A ninelevel multilevel inverter with DC link switches, *Electrical Energy Systems (ICEES), 2014 IEEE 2nd International Conference on* 2014, IEEE, pp. 272-276.

SUH, D., CHOI, J. and SUL, S., 1996. Voltage gradient suppression in application of voltage-fed PWM inverter to AC motor drives-resonant DC link inverter approach, *Applied Power Electronics Conference and Exposition, 1996. APEC'96. Conference Proceedings 1996., Eleventh Annual* 1996, IEEE, pp. 601-606.

SUJITHA, N. and RAMANI, K., 2012. A new Hybrid Cascaded H-Bridge Multilevel inverter-Performance analysis, *Advances in Engineering, Science and Management (ICAESM), 2012 International Conference on* 2012, IEEE, pp. 46-50.

TAGHIZADEH, H. and HAGH, M.T., 2010. Harmonic elimination of cascade multilevel inverters with nonequal DC sources using particle swarm optimization. *Industrial Electronics, IEEE Transactions on*, **57**(11), pp. 3678-3684.

TAKATSUKA, Y., YAMANAKA, K. and HARA, H., 2013. Common-mode voltage reduction method of PWM current source inverter modifying the distribution of zero current vector, *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE* 2013, IEEE, pp. 3088-3093.

TAMPUBOLON, M., PURNAMA, I., CHI, P., LIN, J., HSIEH, Y. and CHIU, H., 2015. A DSP-based differential boost inverter with maximum power point tracking, *Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on* 2015, IEEE, pp. 309-314.

TANG, Y., HE, Y. and DONG, X., 2014a. Active Buck-boost inverter with coupled inductors, *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* 2014a, IEEE, pp. 2754-2759.

TANG, Y., HE, Y. and DONG, X., 2014b. Active Buck-boost inverter with coupled inductors, *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* 2014b, IEEE, pp. 2754-2759.

TOLBERT, L.M. and HABETLER, T.G., 1999. Novel multilevel inverter carrier-based PWM method. *Industry Applications, IEEE Transactions on*, **35**(5), pp. 1098-1107.

TOURKHANI, F., VIAROUGE, P. and MEYNARD, T., 1999. A simulation-optimization system for the optimal design of a multilevel inverter. *Power Electronics, IEEE Transactions on*, **14**(6), pp. 1037-1045.

TUTEJA, A., MAHOR, A. and SIRSAT, A., 2013. A Review on Mitigation of Harmonics in Cascaded H-Bridge Multilevel Inverter using optimization Techniques.

WANG, C., 2003. A novel single-stage full-bridge buck-boost inverter, *Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE* 2003, IEEE, pp. 51-57.

WU, W., JI, J. and BLAABJERG, F., 2015a. Aalborg Inverter-A new type of "Buck in Buck, Boost in Boost" Grid-tied Inverter. *Power Electronics, IEEE Transactions on*, **30**(9), pp. 4784-4793.

WU, W., JI, J. and BLAABJERG, F., 2015b. Aalborg Inverter-A new type of "Buck in Buck, Boost in Boost" Grid-tied Inverter. *Power Electronics, IEEE Transactions on*, **30**(9), pp. 4784-4793.

XUJIAO, G., ZHENGMING, Z. and HAINAN, W., 2001. Evaluation on performances of a new three-phase five-level current source inverter, *Electrical Machines and Systems, 2001. ICEMS 2001. Proceedings of the Fifth International Conference on* 2001, IEEE, pp. 500-503.

YADAV, R., BANSAL, P. and SAXENA, A.R., 2014. A three-phase 9-level inverter with reduced switching devices for different PWM techniques, *Power India International Conference (PIICON), 2014 6th IEEE* 2014, IEEE, pp. 1-6.

YUAN, X. and BARBI, I., 2000. Fundamentals of a new diode clamping multilevel inverter. *Power Electronics, IEEE Transactions on*, **15**(4), pp. 711-718.

YUSOF, M.A., OTHMAN, M., LEE, S.S., ROSLAN, M. and LEONG, J., 2014. Three-phase multilevel inverter with reduced number of active power semiconductor switches for solar PV modules, *Electronic Design (ICED), 2014 2nd International Conference on* 2014, IEEE, pp. 329-334.

ZAMIRI, E., HAMKARI, S., MORADZADEH, M. and BABAEI, E., 2014. A new cascaded multilevel inverter structure with less number of switches, *Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2014 5th* 2014, IEEE, pp. 199-204.

ZHANG, W., WANG, Y., TONG, W., XU, H. and YANG, L., 2005. Study of Voltage-Source PWM Inverter Based on State Combination Method, *Transmission and Distribution Conference and Exhibition: Asia and Pacific, 2005 IEEE/PES* 2005, IEEE, pp. 1-4.

ZHANG, Y., LIU, J., MA, X. and FENG, J., 2014. Multi-loop controller design for diode-assisted buck-boost voltage source inverter, *Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA), 2014 International* 2014, IEEE, pp. 835-842.

ZHANG, Y. and QU, C., 2015. Direct Power Control of a Pulse Width Modulation Rectifier Using Space Vector Modulation Under Unbalanced Grid Voltage.

ZHANG, Z., WANG, F., TOLBERT, L.M., BLALOCK, B.J. and COSTINETT, D., 2014. Evaluation of switching performance of SiC devices in PWM inverter fed induction motor drives, *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* 2014, IEEE, pp. 1597-1604.

ZHENG, Z., WANG, K., XU, L. and LI, Y., 2014. A hybrid cascaded multilevel converter for battery energy management applied in electric vehicles. *Power Electronics, IEEE Transactions on,* **29**(7), pp. 3537-3546.

ZHOU, K., LOW, K., WANG, Y., LUO, F., ZHANG, B. and WANG, Y., 2006. Zero-phase odd-harmonic repetitive controller for a single-phase PWM inverter. *Power Electronics, IEEE Transactions on,* **21**(1), pp. 193-201.

ZHOU, Y. and HUANG, W., 2012. Single-stage boost inverter with coupled inductor. *Power Electronics, IEEE Transactions on,* **27**(4), pp. 1885-1893.

ZHU, M., YU, K. and LUO, F.L., 2010. Switched inductor Z-source inverter. *Power Electronics, IEEE Transactions on,* **25**(8), pp. 2150-2158.

Appendix A

Proof of equations 4-2:

$$\frac{2}{\sqrt{2}\,M_a} - 1 = \frac{V_{load}}{V_{Dc}}$$

In basic buck/ boost converter the relation between the input and output voltages can be expressed as:

$$\frac{V_{out}}{V_{in}} = -\frac{D}{D-1}$$

Where 'D' is the switch duty-cycle. In the case of the BBLFI the output voltage of the buck/boost converter is sinusoidaly modulated. In this case a '√2' factor is used to express the maximum value of the sinusoidaly modulated waveform. The factor of '2' is mainly to express the full wave rectification of also the sinusoidaly modulated waveform (double the output frequency). The factor of '1' is an invert control output signal. Fig. 4-1 illustrates the logic generation of equation 4-2.

Proof of equations 4-11 and 4-12:

The value of the inductor and capacitor in conventional buck/boost converter can be calculated from the following equations:

$$\frac{V_i DT}{L} = -\frac{V_{out}(1-D)T}{L}$$

The value of inductor in equation 4-11 of BBLFI uses M_a instead of the duty cycle in order to express the sinusoidaly modulated waveform. The factor '√2' is maximum value of the sinusioidaly waveform value. The factor '2' in equation 4-11 also reflects the double frequency issue as shown with the two OpAmps in the control circuit of S_1 in Fig. 4-1.

We are using 2 times switching frequency also we use non inverter in SPWM controller that is reason the M_a is in denominator (Fig.4-1). The equations 4-9 and 4-10 are substituting into equation 4-8. The final equation from this substituting is equation 4-11, which define the value of inductor. The value of inductor depends on M_a and M_f value of DSPWM control signal.

$$L = \frac{2V_{dc}}{2 \times \Delta I_{L(Dc)} \times M_a \times f_s} \quad \textbf{(7-1)}$$

$$\frac{2}{\sqrt{2}\,M_a} = \frac{I_{in(Dc)}}{I_{Load}} + 1 \quad \textbf{(7-2)}$$

$$\Delta I_{L(Dc)} = \%\ of\ I_{in(Dc)} \quad \textbf{(7-3)}$$

$$L = \frac{\sqrt{2}\, V_{Dc}}{\% \times (2I_{load} - \sqrt{2}\, M_a I_{load}) \times M_f \times f_s} \quad \textbf{(7-4)}$$

In equation 4-12, the duty cycle of the switch is expressed as M_a, the rest of the equation uses the same parameters used in conventional buck/boost capacitor equation.

$$C = \frac{\sqrt{2} I_{load} \times M_a}{\Delta V_{out} \times (1 - M_a) \times M_f \times f_s} \quad \textbf{(7-5)}$$

Where:

ΔV_{out}: ripple voltage across 'C'
$\Delta I_{in(Dc)}$:ripple current in S_1
f_s: Frequency of switch (S_1)

Proof of equations 4-14:

$$M_a = \frac{2\ V_{Dc}}{\sqrt{2}\, V_{load}}$$

In basic boost converter the relation between the input and output voltages can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D}$$

Where 'D' is the switch duty-cycle. In the case of the BLFI the output voltage of the boost converter is sinusoidal modulated. In this case a '√2' factor is used to express the maximum value of the sinusoidal modulated waveform. The factor of '2' is mainly to express the full wave rectification of also the sinusoidal modulated waveform (double the output frequency). Fig. 4-1 illustrates the logic generation of equation 4-14.

Proof of equations 4-18 and 4-19:

The value of the inductor and capacitor in conventional boost converter can be calculated from the following equations:

$$L = \frac{V_{dc} \times duty\ cycle}{\Delta I_{in(Dc)} \times f_s}$$

$$C = \frac{I_{load} \times duty\ cycle}{f_s \Delta V_{out}}$$

The value of an inductor in equation 4-18 of the BLFI uses M_a instead of the duty cycle in order to express the sinusoidal modulated waveform. The factor '2' in equation 2 also reflects the double frequency issue as shown with the two OpAmps in the control circuit of S_1 in Fig. 4-1.

We are using 2 times switching frequency also we use a non inverter in SPWM controller that is the reason the M_a is in the denominator (Fig.4-1).

$$L = \frac{2V_{dc}}{\Delta I_{in(Dc)} \times M_a \times f_s}$$

In equation 4-19, the duty cycle of the switch is expressed as M_a, the rest of the equation uses the same parameters used in the conventional boost capacitor equation.

$$C = \frac{\sqrt{2} I_{load} M_a}{f_s \Delta V_{out}}$$

Where:

ΔV_{out}: ripple voltage across 'C'
$\Delta I_{in(Dc)}$:ripple current in S_1 (current in inductance)
f_s: Frequency of switch (S_1)

Proof of equation 4-18:

Equations 4-18 can be evaluated from substituting the following two equations into equations 4-16 and 4-17.

$$M_a = \frac{\sqrt{2}\, I_{load(rms)}}{I_{in(dc)}}$$

$$\Delta I_{in(Dc)} = \%\ of\ I_{in(Dc)}$$

$$L = \frac{2V_{dc}}{\% \times \sqrt{2} I_{load} \times f_s}$$

Proof of equations 4-20:

$$\frac{2}{\sqrt{2}\, M_a} + (T_{rr} - 1) = \frac{V_{load}}{V_{Dc}}$$

This equation is same as equation 4-14 by adding extra transformer ratio 'T_{rr}' in this equation. The function of '1' is the minimum output voltage ratio of proposed circuit. This equation is only valid when the voltage ratio of the transformer is higher than 1.

Proof of equations 4-21and 4-22:

The value of the inductor in secondary of transformer winding is the same equation 4-18 by adding a transformer ratio

$$L_2 = \frac{2V_{dc} \times (T_{rr} - 1)}{\Delta I_{L2} \times M_a \times f_s}$$

The value of inductance of the transformer primary winding can be calculated from equation 4-22.

$$L_1 = L_2 \times \frac{1}{{T_{rr}}^2}$$

Capacitor in FLFI circuit is can be calculated from equation 4-19.

$$C = \frac{\sqrt{2} I_{load} M_a}{f_s \Delta V_{out}}$$

Where:

T_{rr}: Transformer ratio

ΔV_{out}: ripple voltage across 'C'
$\Delta I_{in(Dc)}$:ripple current in S_1 (current in inductance)
f_s: Frequency of switch (S_1)

Appendix B

DFT code in MATLAB for reducing the amplitude of low harmonic order;

DFT method is explained in section 4.5 which is optimised to reduce the amplitude of low order harmonics. This method is programmed in MATLAB.

```
% x=input data
%y=Value of the signal at time n


nx= length(y); %number of time samples
p=pi*2/nx;
% to difine Harmonic order amplitude freuquency
for t=1:nx;
   c(t)=0;
  for n=1:nx;
      c(t)=c(t)+(y(n)* exp(complex(0.0, (-1)*(t-1)*p*(n-1))));%
```

$$Hk = \sum_{n=0}^{N-1} y_n \left(e^{-\frac{j2\pi kn}{N}} \right)$$

```
  end
end

v=length(c);%number of current sample

% Reucing amplitude of low harmonic orders
for u=1;
    c(u)=0;
end

for u=2;
    c(u)=c(u);
end
for u=3:38;
    c(u)=c(u)*0.2;
end

for u=39:44;
    c(u)=c(u)*0.95;
end

 for u=45:7744;
    c(u)=0;
 end

 for u=7745:7754;
    c(u)=c(u)*0.95;
 end

 for u=7755:7786;
    c(u)=c(u)*0.2;
```

```
 end
 for u=7787;
    c(u)=c(u);
 end

% convert Harmonic order amplitude frequency to time domin
for u= 1:v;
    z(u)=complex(0,0);
    for n=1:v;
        z(u)= z(u)+(c(n)*exp(complex (0.0, (u-1)*p*(n-1))))/v; %
                        yn = 1/N ∑_{n=0}^{N-1} H_k ( e^{j2πkn/N} )
    end
end

% reduce number of data to comarison between two different output
k=1;

for  ii= 1 : length(b)
     if  y(ii) > y(ii+1) & mod(k,2)~=0
         k=k+1;
         b(k)=y(ii);
         a(k)=x(ii);
     elseif  b(ii) < b(ii+1) & mod(k,2)==0
         k=k+1;
         b(k)=y(ii);
         a(k)=x(ii);
     end

end

o=1;

for  q= 1 : length(z)
     if  z(q) > z(q+1) & mod(o,2)~=0
         o=o+1;
         f(o)=z(q);
         e(o)=x(q);
     elseif  z(q) < z(q+1) & mod(o,2)==0
         o=o+1;
         f(o)=z(q);
         e(o)=x(q);
     end

end

d=real(f); % only real value of f function
plot (b,d);
```

Arduino example code for 2.1 kHz; variable output frequency (30-70Hz) and variable output voltage.

The Output frequency and voltage can be controlled by changing the duty cycle (changing time delay) and frequency in Arduino by changing the value of X1, Y1 and Z1. These values are changed by varying potential meter as input of Arduino.

```
void setup(){
pinMode(1, OUTPUT); //2.1kHz
pinMode(2, OUTPUT); //50HZ 10ms on
pinMode(3, OUTPUT); //50Hz 10 ms off
pinMode(A0.INPUT);//  input read from potential meter 1
pinMode(A1.INPUT);//  input read from potential meter2
pinMode(A2.INPUT);//  input read from potential meter 3
}
void loop(){
x1=digitalRead(A0);// read value input value 1
y1=digitalRead (A1); // read value input value 2
z1=digitalRead (A2); // read value input value 3
if (x1<=300)
{x1=0}
else if (x1>=716)
{x1=0}
else {
x=x1/512;
y=y1/10;
z=z1/10;

digitalWrite(1, HIGH);
digitalWrite(2, HIGH);
digitalWrite(3, LOW);

 delayMicroseconds((132-z+y)/x);
 digitalWrite(1, LOW);  //1
 delayMicroseconds((10-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((470-z+y)/x);
 digitalWrite(1, LOW);  //2
 delayMicroseconds((16-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((460-z+y)/x);
 digitalWrite(1, LOW);  //3
 delayMicroseconds((23-z+y)/x);
 digitalWrite(1, HIGH); //
 delayMicroseconds((450-z+y)/x);
 digitalWrite(1, LOW);  //4
 delayMicroseconds((33-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((440-z+y)/x);
 digitalWrite(1, LOW);  //5
 delayMicroseconds((43-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((440-z+y)/x);
 digitalWrite(1, LOW);  //6
```

```
delayMicroseconds((53-z+y)/x);
digitalWrite(1, HIGH); //13
delayMicroseconds((420-z+y)/x);
digitalWrite(1, LOW);  // 7
delayMicroseconds((63-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((410-z+y)/x);
digitalWrite(1, LOW);  //8
delayMicroseconds((70-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((400-z+y)/x);
 digitalWrite(1, LOW);  //9
 delayMicroseconds((80-z+y)/x);
 digitalWrite(1, HIGH); //
 delayMicroseconds((400-z+y)/x);
 digitalWrite(1, LOW);  //10
 delayMicroseconds((85-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((390-z+y)/x);
 digitalWrite(1, LOW);  //11
 delayMicroseconds((90-z+y)/x); 5ms
 digitalWrite(1, HIGH); //
 delayMicroseconds((390-z+y)/x);
 digitalWrite(1, LOW);  //12
 delayMicroseconds((90-z+y)/x);
 digitalWrite(1, HIGH); //
 delayMicroseconds((400-z+y)/x);
 digitalWrite(1, LOW); //13
 delayMicroseconds((85-z+y)/x);
 digitalWrite(1, HIGH);
 delayMicroseconds((410-z+y)/x);
 digitalWrite(1, LOW);  //14
 delayMicroseconds((80-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((420-z+y)/x);
 digitalWrite(1, LOW);  //15
 delayMicroseconds((65-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((430-z+y)/x);
 digitalWrite(1, LOW);  //16
 delayMicroseconds((50-z+y)/x);
 digitalWrite(1, HIGH); //
 delayMicroseconds((440-z+y)/x);
 digitalWrite(1, LOW);  //17
 delayMicroseconds((40-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((450-z+y)/x);
 digitalWrite(1, LOW);  //18
 delayMicroseconds((30-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((460-z+y)/x);
 digitalWrite(1, LOW);  //19
 delayMicroseconds((20-z+y)/x);
 digitalWrite(1, HIGH); //
 delayMicroseconds((470-z+y)/x);
 digitalWrite(1, LOW);  // 20
 delayMicroseconds((10-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((480-z+y)/x);
```

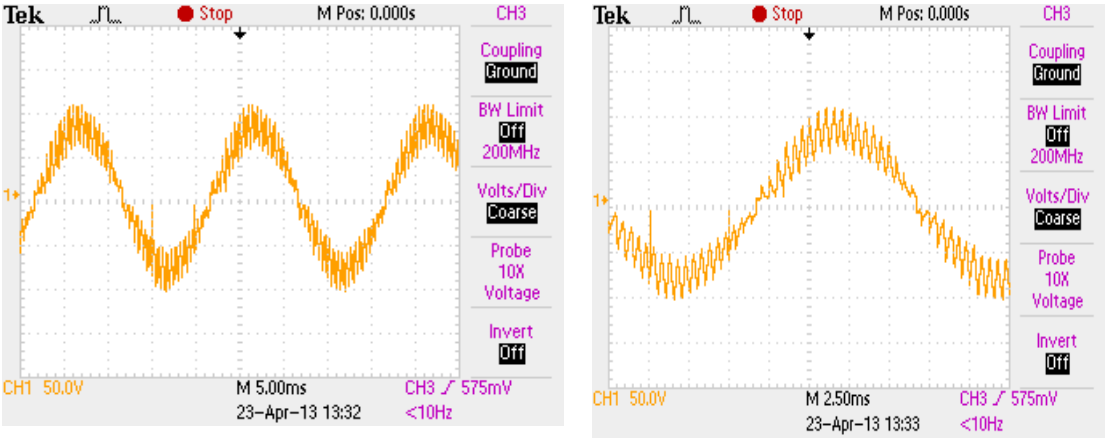
```
digitalWrite(1, LOW);  //21
delayMicroseconds((6-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((154-z+y)/x);
digitalWrite(1, HIGH);//10ms
digitalWrite(2, LOW); // 10ms off
digitalWrite(3, HIGH);//10ms on
delayMicroseconds((132-z+y)/x);
digitalWrite(1, LOW);  //1
delayMicroseconds((10-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((470-z+y)/x);
digitalWrite(1, LOW);  //2
delayMicroseconds((16-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((460-z+y)/x);
digitalWrite(1, LOW);  //3
delayMicroseconds((23-z+y)/x);
digitalWrite(1, HIGH); //
delayMicroseconds((450-z+y)/x);
digitalWrite(1, LOW);  //4
delayMicroseconds((33-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((440-z+y)/x);
digitalWrite(1, LOW);  //5
delayMicroseconds((43-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((440-z+y)/x);
digitalWrite(1, LOW);  //6
delayMicroseconds((53-z+y)/x);
digitalWrite(1, HIGH); //13
delayMicroseconds((420-z+y)/x);
digitalWrite(1, LOW);  // 7
delayMicroseconds((63-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((410-z+y)/x);
digitalWrite(1, LOW);  //8
delayMicroseconds((70-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((400-z+y)/x);
digitalWrite(1, LOW);  //9
delayMicroseconds((80-z+y)/x);
digitalWrite(1, HIGH); //
delayMicroseconds((400-z+y)/x);
digitalWrite(1, LOW);  //10
delayMicroseconds((85-z+y)/x);
digitalWrite(1, HIGH);  //
delayMicroseconds((390-z+y)/x);
digitalWrite(1, LOW);  //11
delayMicroseconds((90-z+y)/x); 5ms
digitalWrite(1, HIGH); //
delayMicroseconds((390-z+y)/x);
digitalWrite(1, LOW);  //12
delayMicroseconds((90-z+y)/x);
digitalWrite(1, HIGH); //
delayMicroseconds((400-z+y)/x);
digitalWrite(1, LOW); //13
delayMicroseconds((85-z+y)/x);
digitalWrite(1, HIGH);
```

```
 delayMicroseconds((410-z+y)/x);
 digitalWrite(1, LOW);  //14
 delayMicroseconds((80-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((420-z+y)/x);
 digitalWrite(1, LOW);  //15
 delayMicroseconds((65-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((430-z+y)/x);
 digitalWrite(1, LOW);  //16
 delayMicroseconds((50-z+y)/x);
 digitalWrite(1, HIGH); //
 delayMicroseconds((440-z+y)/x);
 digitalWrite(1, LOW);  //17
 delayMicroseconds((40-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((450-z+y)/x);
 digitalWrite(1, LOW);  //18
 delayMicroseconds((30-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((460-z+y)/x);
 digitalWrite(1, LOW);  //19
 delayMicroseconds((20-z+y)/x);
 digitalWrite(1, HIGH); //
 delayMicroseconds((470-z+y)/x);
 digitalWrite(1, LOW);  // 20
 delayMicroseconds((10-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((480-z+y)/x);
 digitalWrite(1, LOW);  //21
 delayMicroseconds((6-z+y)/x);
 digitalWrite(1, HIGH);  //
 delayMicroseconds((154-z+y)/x);
}}
```

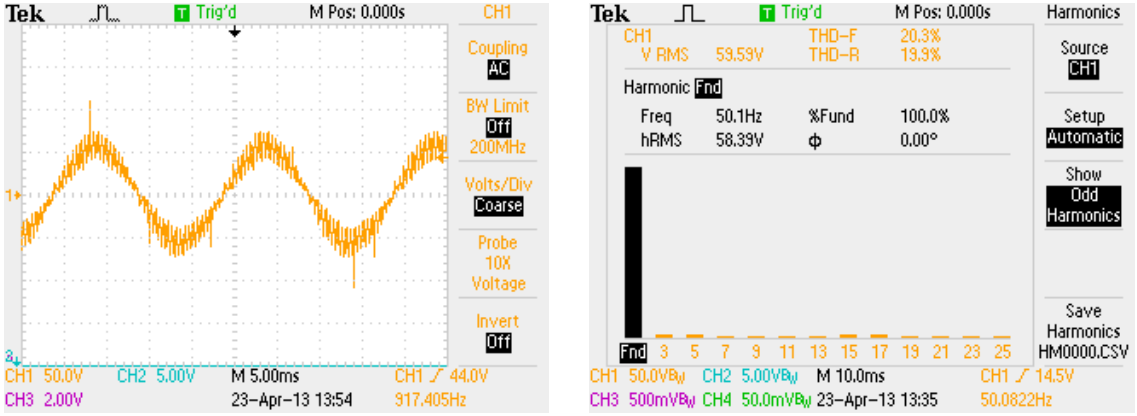
Appendix C

This appendix includes some of the practical results for extra information of proposed circuits with DSPWM controller. The output voltage, the input voltage of H-bridge, output current and FFT of output voltage are shown in this appendix. The first practical results are about BBLFI circuit with DSPWM controller. The second practical results show the output of the BLFI circuit with DSPWM controller. Next part shows the practical result of FLFI circuit and the last part shows the practical result of the proposed circuit as induction motor driver.

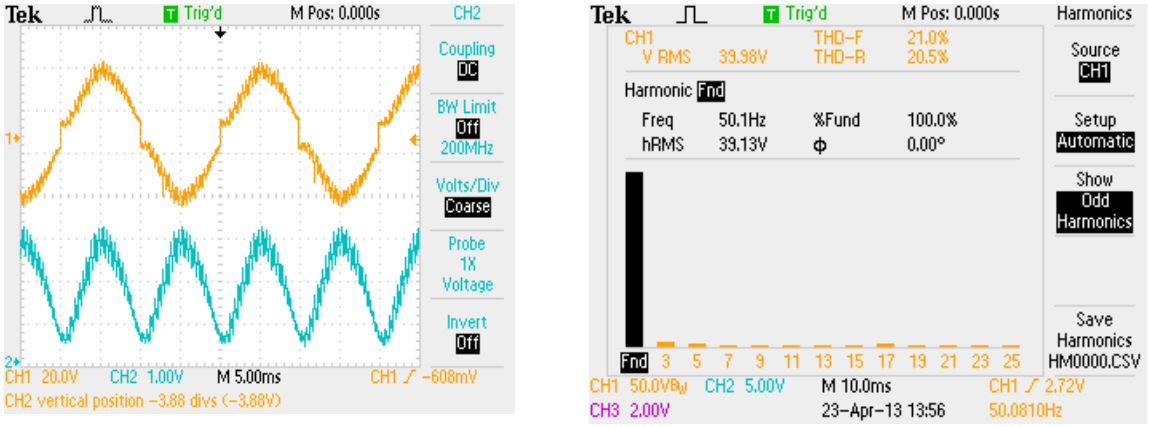
Buck/Boost-based Low Frequency practical example results



Output voltage of BBLFI



Output voltage and FFT of BBLFI circuit

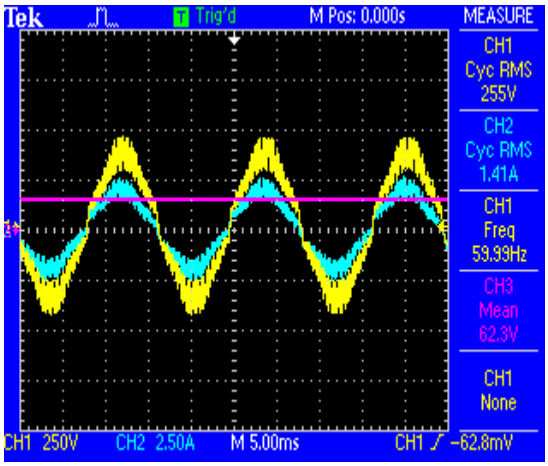


Input Voltage of H-bridge, Output voltage and FFT of BBLFI circuit

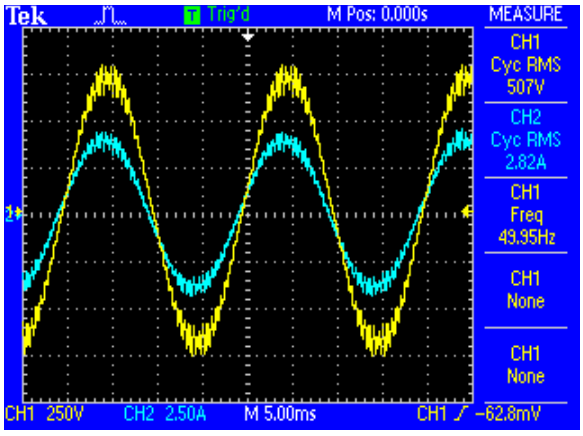
Practical results of BLFI circuit with DSPWM controller are shown in the next part, which shows the FFT of current and output voltage of proposed circuit. These results show the FFT of current with optimising low order harmonics. Also, these practical results are from the same circuit with different loads. However, there are some practical example of 60Hz output frequency. The last result is 500V output voltage of BLFI circuit also the FFT of the output current of this proposed circuit.

Boost-based Low Frequency practical example results

FFT of output current and FFT of output current with Optimising to minimise 3rd harmonic



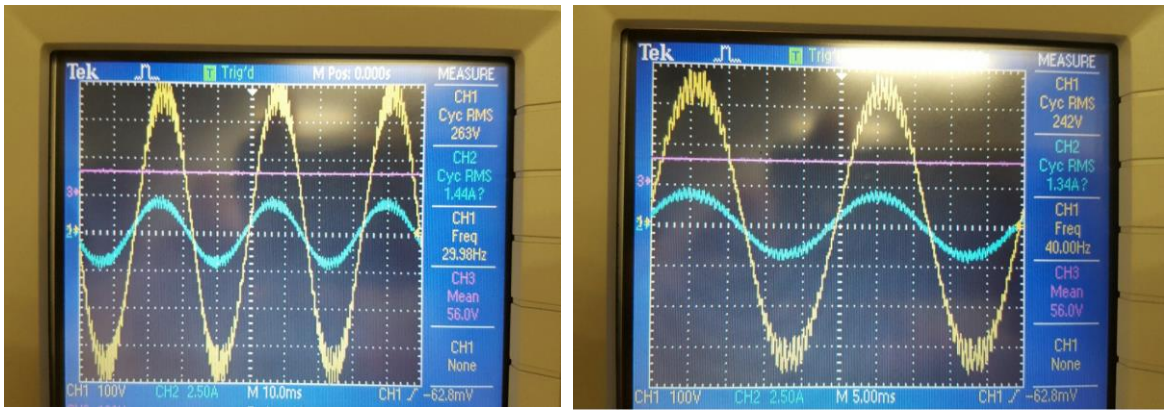
Output current, output voltage and FFT of output current of BLFI circuit (60Hz)



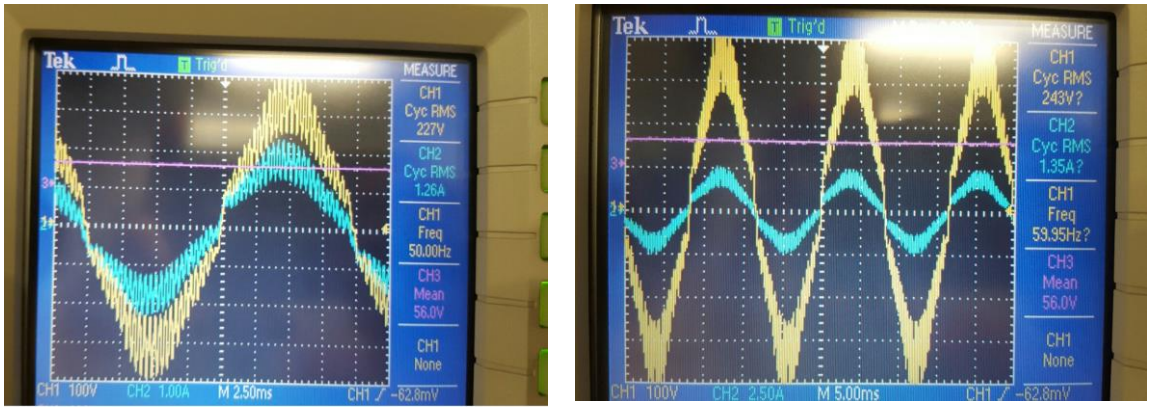
Output current, output voltage and FFT of output current of BLFI circuit in higher output voltage (507V)

Flyback-based Low Frequency practical example results

Practical results of FLFI circuit with DSPWM controller are shown in this part, which shows the FFT of current and output voltage of the proposed circuit in different output frequency. The last result shows the optimized output current to minimise low order harmonics.

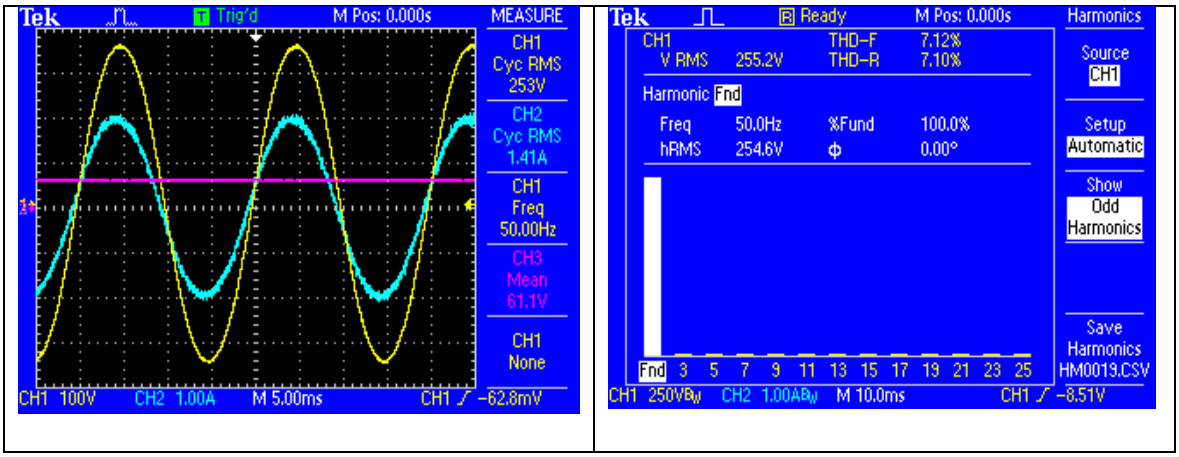


Output current and output voltage of FLFI circuit with 30Hz and 40Hz output frequency. The input voltage of this circuit is 56V



Output current and output voltage of FLFI circuit with 50Hz and 60Hz output frequency. The input voltage of this circuit is 56V

Output current and output voltage of FLFI circuit with 118Hz and 117Hz output frequency



Optimising Output current and output voltage to minimise low order harmonics of FLFI circuit with 50Hz output frequency. The input voltage of this circuit is 56V

Induction motor drive example results for different loads

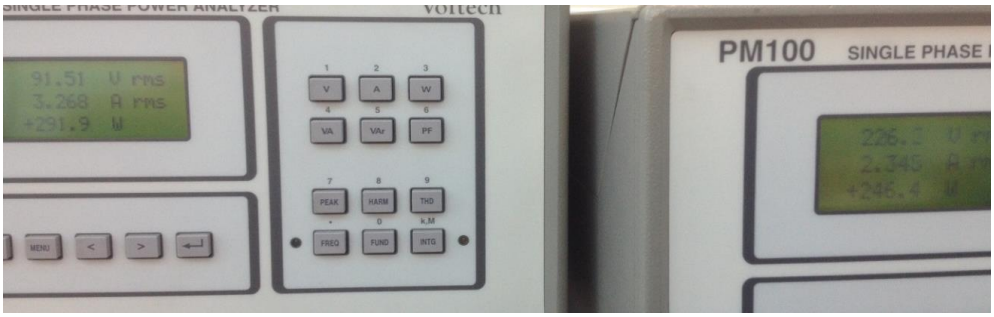
Lab results of induction motor drive, motor drive work about 30 min without putting any load on it to stable motor.

The power of the motor is increased by changing the power of load handily.

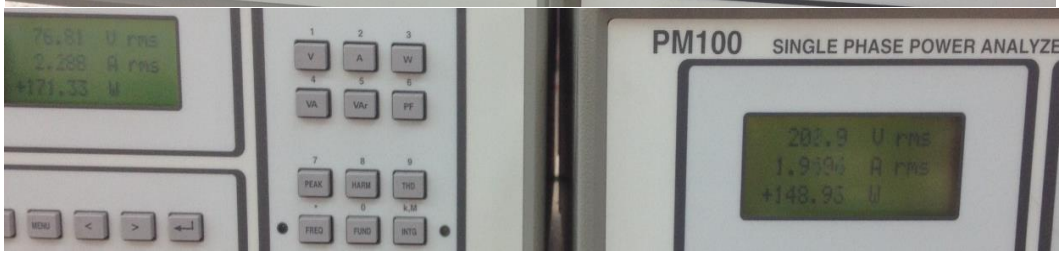
Reach power of 309 W, then the efficiency of inverters is about 80% and power factor is 72%.

The power factor was raised from 25% to 73% on load side. And power factor in supply can be reached to above 92%.

And efficiency was raised from 40% to 80%.


91.51 V rms
3.268 A rms
+291.9 W
PM100 SINGLE PHASE


PM100 SINGLE PHASE POWER AN
193.22 V rms
1.9259 A rms
+216.7 W


76.81 V rms
2.288 A rms
+171.33 W
PM100 SINGLE PHASE POWER ANALYZE
202.9 V rms
1.9494 A rms
+148.95 W

MOTOR DRIVER of BLFI circuit with frequency is 2kHz

Case No	V(in Dc) Volt (AVG)	I (in DC) A (AVG)	Power on (AVG)	V (Out Ac) Volt (rms)	$I_{rms\ output}$ A	P output W	Power factor (output)	Efficiency (%)	Torque (N.M)	Speed (RPM)
Case1	70	2.34	163.8	191.88	1.6	127.15	41.40%	77.62		
Case2	71	2.25	159.75	200.4	1.7	137.5	40.30%	86.07		
Case3	89	2.71	241.19	228	2.017	184	40%	76.28	0.1	2994
Case4	104	4	416	233	2.27	316	60%	75.96	0.45	2889
Case5	120	1.8	216	214	1.84	158	40%	73.14	0.074	3020
Case6	130	2.04	265.2	220	1.94	195	45%	73.58	0.16	3014
Case7	145	2.58	374.1	230	2.17	280	56%	74.84	0.35	2950
Case8	143	2.89	413.27	213	2.25	332	69%	80.33	0.46	3040

MOTOR DRIVER of BLFI circuit with frequency is 1kHz

Case No	V (in DC) Volt (AVG)	I (in DC) A (AVG)	Power on (AVG)	V (Out Ac) Volt (rms)	$I_{rms\ output}$ A	P output W	Power factor (output)	Efficiency (%)	Torque (N.M)	Speed (RPM)
Case 1	70	2.05	143.5	190	1.5	118	40%	82.2299652	0.076	2876
Case 2	90	2.7	243	240	2.1	173	34.50%	71.1934156	0.068	2893
Case3	93	3.15	292.95	224	1.97	241	54%	82.2665984	0.34	2800
Case4	104	3.78	393.12	230	2.32	320	62.10%	81.4000814	0.516	2730
Case5	92	1.43	131.56	173	1.4	110	45%	83.6120401	0.08	3020
Case6	120	1.8	216	216	1.85	152	38%	70.3703704	0.081	3047
Case7	136	2.66	361.76	216	2.135	295	63.80%	81.5457762	0.44	2900
Case 8	139	2.13	296.07	225	1.91	240	55%	81.061911	0.76	3248
Case9	95	3.1	294.5	245	1.9	240	50%	81.4940577	0.276	3140