Losses and Cost Optimisation of PV Multilevel Voltage Source Inverter with Integrated Passive Power Filters

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Submitted in partial fulfilment of the requirements for the degree of
Doctor of Philosophy

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December 2016

ABSTRACT

Nowadays, the need for more contributions from renewable energy sources is rapidly growing. This is forced by many factors including the requirements to meet the targeted reductions of greenhouse gas emissions as well as improving the security of energy supply. According to the International Renewable Energy Agency (IRENA) report 2016, the total installed capacity of solar energy was at least 227 GWs worldwide by the end of 2015 with an annual addition of about 50 GWs in 2015, making solar power the world's fastest growing energy source. The majority of these are grid-connected photo voltaic (PV) solar power plants, which are required be integrated efficiently into the power grids to meet the requirements of power quality standards at the minimum total investment cost. For this, multilevel voltage source inverters (VSI) have been applied extensively in recent years.

In practice, there is a trade-off between the inverter's number of levels and the required size of output filter, which is a key optimisation area. The aim of this research is to propose a generic model to optimise the design number of levels for the Cascaded H-Bridge Multilevel Inverter (CHB-MLI) and the size of output filter for medium voltage – high power applications. The model is based on key measures, including inverter power loss minimisation, efficient control for minimum total harmonic distortion (THD), minimisation of total system cost and proposing the optimum size of output filter. This research has made a contribution to knowledge in the optimisation of CHB-MLI for medium-voltage high-power applications, in particular, the trade-off optimisation of the inverter's number of levels and the size of the output filter. The main contribution is the establishment and demonstration of a sound methodology and model based on multi-objective optimisation for the considered key measures of the trade-off model. Furthermore, this study has developed a generic precise model for conduction and switching loss calculation in multilevel inverters. Moreover, it applied Genetic Algorithm (GA) optimisation to provide a complete optimum solution for the problem of selective harmonic elimination (SHE) and suggests the optimum size of output passive power filter (PPF) for different levels CHB-MLIs.

The proposed trade-off optimisation model presents an efficient tool for finding the optimum number of the inverter's levels and the size of output filter, in which the integration system is at its lowest cost, based on optimisation dimensions and applied system constraints. The trade-off optimisation model is generic and can be applied to any multilevel inverter topologies and different power applications.

DEDICATION

I would like to dedicate this thesis work to the souls of my mother ‘Atiqah’ and my father ‘Rashid’ who helped me in all things greats and small. Special thanks to my lovely kids ‘Battal’ and ‘Tulip’ for their emotional support and patience. Particularly and most sincerely, I would like to dedicate this work to my brilliant wife ‘Salwa’ for her endless love, patience, and outstanding support during the PhD journey. I am truly thankful for having you in my life.

ACKNOWLEDGMENTS

All praise is for Almighty Allah for having guided me at every stage of my life. Thanks to Allah for the strengths and guidance in completing this thesis.

I would like to express my sincere gratitude and appreciations to my great supervisor Dr. Mohamed Darwish, for his continuous support through all my PhD studies, I appreciate his patience, continuous motivations, and immense knowledge. His support and guidance helped me in all the time of my research and writing up this thesis.

I would like also to thank the faculty members : Prof. Hamed Al-Raweshidy, Dr. Ahmed Zobaa, Dr. Maysam Abbod, Dr. Barry Rawn and Dr. Cristos Marouchos for their insightful comments and encouragement. Also, for the valuable discussions, and research questions which widen my study from various perspectives.

My sincere thanks also go to my PhD office mates and friends for the stimulating discussions, their collaborations when we were working during hard times to meet deadlines. For being true friends which makes the office the most comfortable place to work in.

I am also grateful to Taif University (TU) for their support and funding through all this research. Without their precious support, it would not be possible to conduct this research.

Author's Declaration

I hereby declare and confirm that this thesis is my own work and efforts. Also, it has not been submitted anywhere for any award. Where other sources of information have been used, they have been acknowledged.

Basem Alamri

December 2016

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List of Abbreviations

AC	Alternating Current
ANN	Artificial Neural Network
ANSI	American National Standard Institute
APF	Active Power Filter
APOD	Alternative Phase Opposite Disposition
BP PLC	British Petroleum Public Limited Company
CHB-MLI	Cascaded H-Bridge Multilevel Inverter
CSI	Current Source Inverter
DC	Direct Current
DG	Distributed Generator
DSP	Digital Signal Processing
DT	Double Tuned
DVR	Dynamic Voltage Restoration
EA	Evolution Algorithm
EMI	Electro-Magnetic Interference
EN	European Norms
FACTS	Flexible Ac Transmission System
FC-MLI	Flying Capacitor Multilevel Inverter
FIT	Failure In Time
GA	Genetic Algorithm
GTO	Gate Turn-Off Thyristors
HP	High Pass
HV	High Voltage
HVDC	High Voltage Direct Current
IEA	International Energy Agency
IEEE	Institute Of Electrical And Electronics Engineers
IEEE-519	IEEE Recommended Practice And Requirements For Harmonic Control In Electrical Power Systems
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristor
LCI	Line Commutated Inverters
ML-VSI	Multilevel Voltage Source Inverter

NLC	Nearest Level Control
NPC-MLI	Neutral-Point Clamped Multilevel Inverter
NR	Newton Raphson
PCC	Point of Common Coupling
PD	Phase Disposition
POD	Phase Opposite Disposition
PPF	Passive Power Filter
PSO	Particle Swarm Optimisation
PV	Photo Voltaic
PWM	Pulse Width Modulation
PWM-CSI	Pulse width modulation – Current Source Inverter
Q	Quality factor of Filter
S	Power Switch
SA	Simulating Annealing
SCR	Silicon Controlled Rectifier
SDCS	Separate Direct Current Source
SHE	Selective Harmonic Elimination
SHE-PWM	Selective Harmonic Elimination – Pulse width Modulation
SMPS	switch mode power supply
SPWM	Sinusoidal Pulse Width Modulation
ST	Single Tuned
STATCOM	Static Synchronous Compensator
SVC	Space Vector Control
SVM	Space Voltage Modulation
THD	Total Harmonic Distortion
TS	Tabu Search
UK	United Kingdom
UPFC	Unified Power Flow Controller
UPQC	unified power quality conditioner
UPS	uninterruptible power supply
VSI	Voltage Source Inverter

CHAPTER 1: INTRODUCTION

1.1 Preface

The demand for an efficient power-generation contribution from renewable energy sources has grown exponentially in the last decade. This fast growth has been mainly forced by the requirements to meet the targeted reductions of greenhouse gases emissions, the price volatility of fossil fuel and the need to improve the security of power supply. Among renewable energy sources, solar and wind are considered to be the most dominant. Figure 1.1 depicts the annual growth of wind and solar energy generation capacity over the last decade [1].

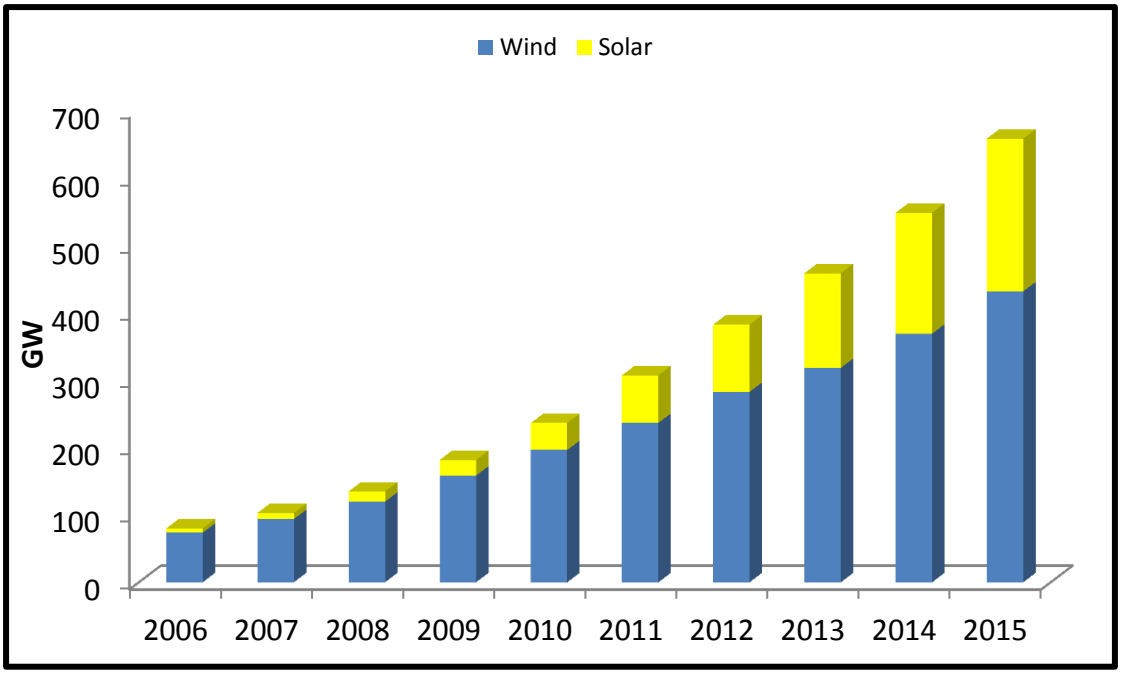


Figure 1.1: Annual growth of worldwide total installed capacity for wind and solar power.

It is possible to see that the generation capacity from wind and solar sources has increased six times over the last ten years. Power grids are experiencing more and rapid penetration of medium- and large-scale power plants from wind and solar. According to the International Renewable Energy Agency (IRENA) report 2016 , the installed capacity of wind power farms was around 432 GWs worldwide by the end of 2015 [1]. In addition, the installed capacity of solar photovoltaic (PV) technology was at least 227 GWs worldwide by the end of 2015, with an annual addition of about 50

GWs in year 2015. Most of these are grid-connected PV power plants. In the next few years, more than 250 solar (PV) power plants will be installed, some of them in excess of 500 MW capacity. This rapid spread is supported by the substantial decrease in the cost of PVs, which have reduced in price by more than 80% in the last eight years. Furthermore, PV power plants can be built and installed within a relatively short time scale (typically 6–12 months), which is much quicker compared to conventional fossil fuel power plants (typically 4–5 years) [2]. It is expected that solar PV power plants will continue to grow rapidly in the near future.

Due to the rapid spread and growth in renewable energy generation, more power electronics devices are being implemented in today's electrical power networks. Medium- and large-scale PV power plants are integrated into utility grids via power electronics inverters, which are considered a major source of harmonics and affect the power quality significantly. Therefore, it is important to efficiently design the inverter required for this integration to meet the harmonic limits as recommended by international standards for acceptable power-quality levels [3].

Several conventional inverters have been proposed and implemented for the integration of PV power plants into power grids. In conventional inverters, it is difficult to connect a single semiconductor switch to medium voltage – high power applications. Therefore, integration with conventional inverters requires the implementation of a step-up transformer, line filter and series/parallel connection of multiple high-voltage power switches; these increase the total system size, weight, power loss, cost and complexity. Nowadays, multilevel voltage-source inverters are replacing conventional inverters to better integrate PV grid-connected power plants. These multilevel inverters are capable of building a higher output voltage with a smaller number of switching devices with a lower blocking voltage. The application of multilevel inverters for direct grid connection of PV power plants has attracted many researchers and continues to gain more attention. The purpose is to achieve a more efficient and cost effective inverter design, which can be connected directly to the power grid without the need to use a step-up transformer or an output filter, or to significantly reduce the size of the required output filter.

1.2 Motivations

With today's movement towards deregulation and liberalization of power markets, a greater contribution and penetration of distributed generations (DGs) is taking place across the world. The rapid growth in renewable energy is expected to continue. According to British Petroleum Plc report-2016, solar energy grew by 33% in 2015, making sun power the world's fastest-growing energy source [4]. This has been supported by sharp cost reductions and technological advancement of PVs. Figure 1.2 depicts solar PV global capacity and annual additions for the period 2005–2015 [5].

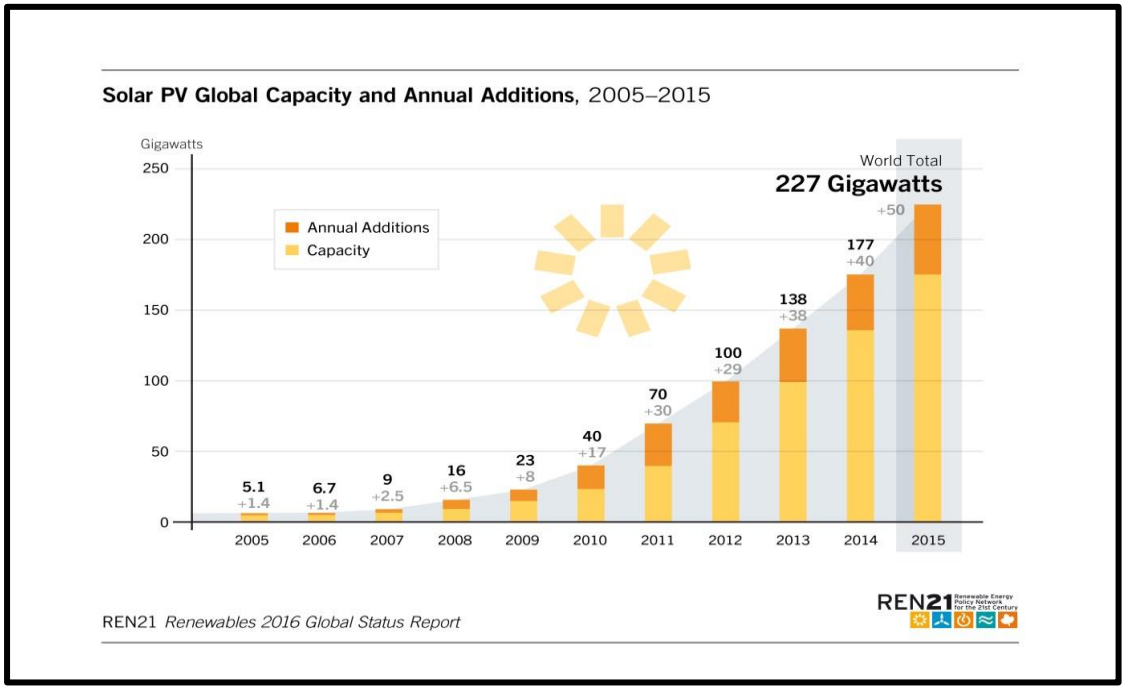


Figure 1.2: Solar PV global capacity and annual additions 2005–2015 [5].

Most of the installed capacity of solar PV power plants is grid-connected. These additional PV power plants should be integrated efficiently with the power grids. Voltage-source multilevel inverters play a vital rule in the integration of these distributed generators (DGs) due to their superiority compared to conventional two-level inverters in having: 1) higher output voltage at low-switching frequency, 2) low voltage stress (dv/dt), 3) lower total harmonic distortion (THD), 4) less electro-magnetic interference (EMI), 5) a smaller output filter and 6) higher fundamental

output. In practice, there is a trade-off between the inverter's number of levels and the required size of output filter, which is considered to be a key area for optimisation. This requirement has encouraged exploration and investigation of the potential for optimizing the integration system of solar PV power plants by proposing a generic optimisation model to deal with the trade-off problem. The optimisation model is based on key system-performance measures including: design efficiency, inverter control for minimum THD, number of inverter levels, system power losses and system cost for the required medium-voltage–high-power application and to recommend the optimum size of output filters.

1.3 Thesis Aim and Objectives

The aim of this thesis is to develop a generic optimization model for multilevel inverters for renewable energy sources. This will be achieved by finding a feasible way of quantifying the existing trade-off key measures to optimize the designed number of levels for the cascaded H-bridge multilevel inverter (CHB-MLI) topology and the required size of output filter for medium voltage – high power applications. The model is based on precise inverter power-loss minimisation, efficient control for minimum THD, minimisation to total system cost and proposing the optimum size of output filter. There is an optimum number of inverter levels and size of output filter where the integration system achieves its lowest cost, based on optimisation dimensions and applied system constraints. To achieve the research aim stated above, the following main objectives are set:

1. To undertake an extensive literature review through books, journals and conference papers about high-power inverters, with a focus on multilevel voltage-source inverter topologies and their applied control methods.
2. To critically review the problem of power-system harmonics, description of the phenomenon, causes/effects and applied solutions for harmonic mitigations.
3. To critically review and classify power-filter circuit configurations, key features, and the advantages and disadvantages of different filter topologies.

4. To propose a generic model to solve the problem of selective harmonic elimination (SHE) control and minimize THD for any number of inverter levels. This will be based on genetic algorithm (GA) optimisation and implementing the proposed algorithm to obtain the solution of SHE switching angles for inverter levels (3 to 31), according to the proposed GA solution.
5. To analyse and compare the results of %THD for different-level inverters when applying SHE and sinusoidal pulse-width modulation (SPWM) control.
6. To build a precise generic model for calculating conduction and switching power loss in multilevel inverters, based on actual switching device datasheets. The model is generic and can be applied for any multilevel inverter topology with any number of levels.
7. To implement an optimisation model based on GA to find the optimum design for the composite passive power filter at the output of CHB-MLI, which minimizes filter cost, power loss, %THD, and improves the power factor at the point of common coupling PCC.
8. To investigate the optimum number of levels for different CHB-MLI designs, based on inverter inverter's power loss, %THD, device counts and cost.
9. To analyse the optimum trade-off between number of inverter levels and size of output filters, based on the proposed optimisation approach.

1.4 Thesis Outline

The work accomplished in this thesis is presented and organized in six chapters, which are illustrated in Figure 1.3, with the relationship to the thesis objectives presented in section 1.3

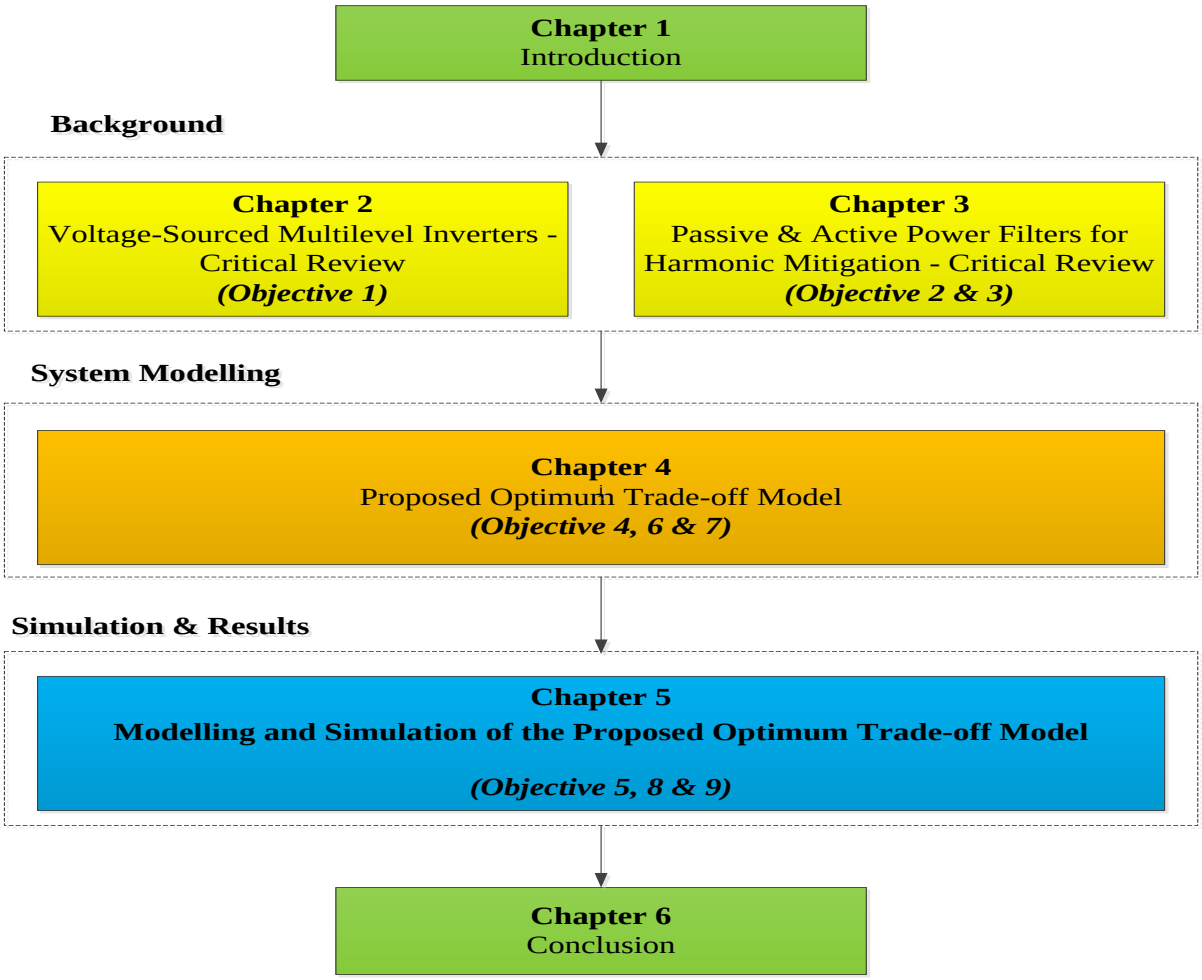


Figure 1.3: Thesis structure.

The content of each chapter is summarized below:

Chapter 1 provides general background about the worldwide rapid growth of renewable energy, especially wind and solar, with a focus on PV power plants. This is followed by a demonstration of the research aim, objectives and layout of the thesis.

Chapter 2 starts with a general classification of high-power inverters. Current-source inverters (CSIs) and voltage-source inverters (VSIs) are discussed in terms of historical development, main operating principles and key features. To sum up this part, a technical comparison is presented. A critical review for VSIs is conducted. This covers the three basic topologies and applied control techniques, and it highlights the superiority of the CHB-MLI for medium-voltage–high-power applications.

Chapter 3 addresses the problem of power-system harmonics by describing the phenomenon, classifying its main sources, discussing the adverse effects of harmonics on power systems and illustrating the existing solutions applied for harmonic mitigation. The second part of this chapter critically reviews power filters, and the chapter concludes by providing critical review tables for passive, active and hybrid power filters.

Chapter 4 sets out the background for the trade-off problem under investigation. It then presents the proposed optimisation for the trade-off model. The mathematical problem formulation for SHE control is demonstrated, and a GA-based generic optimisation model is introduced. The evaluation of power loss in multilevel inverters is reviewed. The chapter then proposes a generic detailed model for calculating conduction and switching power losses, particularly in multilevel inverters, based on actual switching device datasheets. The model can be applied for any multilevel inverter topology with any number of levels. The last part of this chapter investigates the problem of passive power filter design optimisation. First, a comparison review is demonstrated between conventional and heuristic approaches in passive power filter (PPF) design. Then, a GA-based optimum design model for PPFs, based on both economic and technical considerations, is proposed for the trade-off problem.

Chapter 5 illustrates the proposed optimum trade-off model implementation and simulation outcome in a Matlab/Simulink environment. The switching angles of SHE are determined for inverter levels (3 to 31) using GA-based optimisation. In addition, the %THD for CHB-MLI is compared for different inverter levels using SHE and SPWM control techniques. Furthermore, detailed analysis of conduction and switching power losses in CHB-MLI at different levels is presented. An investigation of the trade-off problem to find the optimum number of inverter levels and size of output filter is carried out. All discussions, investigations and analysis are supported by appropriate results.

Chapter 6 summarizes the main conclusions, findings and contribution to knowledge for the thesis and suggests possible future work.

1.5 Author's Publications

The following conferences and journals papers were published:

Journals:

1. B. Alamri and M. Darwish, "Power Loss Investigation for 13-level Cascaded H-Bridge Multilevel Inverter", J. Energy Power Sources, 2015 Vol. 2, No. 6 , pp. 230-238

Conferences:

1. B. Alamri and M. Darwish, "Enhancing Power Quality of Distributed Generator systems Using Multilevel VSC", ResCon2013, Brunel University, London, UK.
2. B. Alamri and M. Darwish, "Optimum Switching Angles Determination for Cadcaded H-Bridge Multilevel Inverters Using Genetic Algorithm (GA)", ResCon2014, Brunel University, London, UK.
3. B. Alamri and M. Darwish, "Precise Modelling of Switching and Conduction Losses in Cascaded H-bridge Multilevel Inverters", Int. Power Engineering Conference (UPEC), 49th International Universities, Cluj-Napoca, pp. 1-6. IEEE, 2014.
4. B. Alamri, A. Sallama and M. Darwish, "Optimum SHE for Cascaded H-Bridge Multilevel Inverters Using: NR-GA-PSO, Comparative Study," *AC and DC Power Transmission, 11th IET International Conference on*, Birmingham, 2015, pp. 1-10.
5. B. Alamri and M. Darwish, "Power loss investigation in HVDC for cascaded H-bridge multilevel inverters (CHB-MLI)," *PowerTech, 2015 IEEE Eindhoven*, Eindhoven, 2015, pp. 1-7.
6. B. Alamri, S. Alshahrani and M. Darwish, "Losses investigation in SPWM-controlled cascaded H-bridge multilevel inverters," *Power Engineering Conference (UPEC), 2015 50th International Universities*, Stoke on Trent, 2015, pp. 1-5.
7. M. Darwish, B. Alamri and C. Marouchos, "OrCAD vs Matlab Simulink in teaching power electronics," *Power Engineering Conference (UPEC), 2015 50th International Universities*, Stoke on Trent, 2015, pp. 1-5.

CHAPTER 2: VOLTAGE-SOURCED MULTILEVEL INVERTERS – CRITICAL REVIEW

2.1 Introduction

Power electronics plays a vital role in achieving efficient, reliable and high-power quality integration of renewable energy sources into power grids via power conversion and inversion, and through HVDC links. This chapter presents a critical review of high-power inversion, with a focus on voltage-source multilevel inverters. First, a general classification of high-power inverters is discussed, and a technical comparison of the major types is presented. Then, the three classical voltage-source multilevel-inverter topologies are reviewed and compared in depth, with a focus on the superiority of the cascaded H-bridge in high-power applications. The chapter concludes by demonstrating the main modulation techniques applied for multilevel inverters.

2.2 Classification of High-Power Inverters

Figure 2.1 shows the basic classification of high-power inverters, classified into two main categories: 1) current-source inverters (CSIs) and 2) voltage-source inverters (VSIs). Below, the basic concept and features of each type are explained, followed by a detailed technical comparison between CSIs and VSIs. [6]

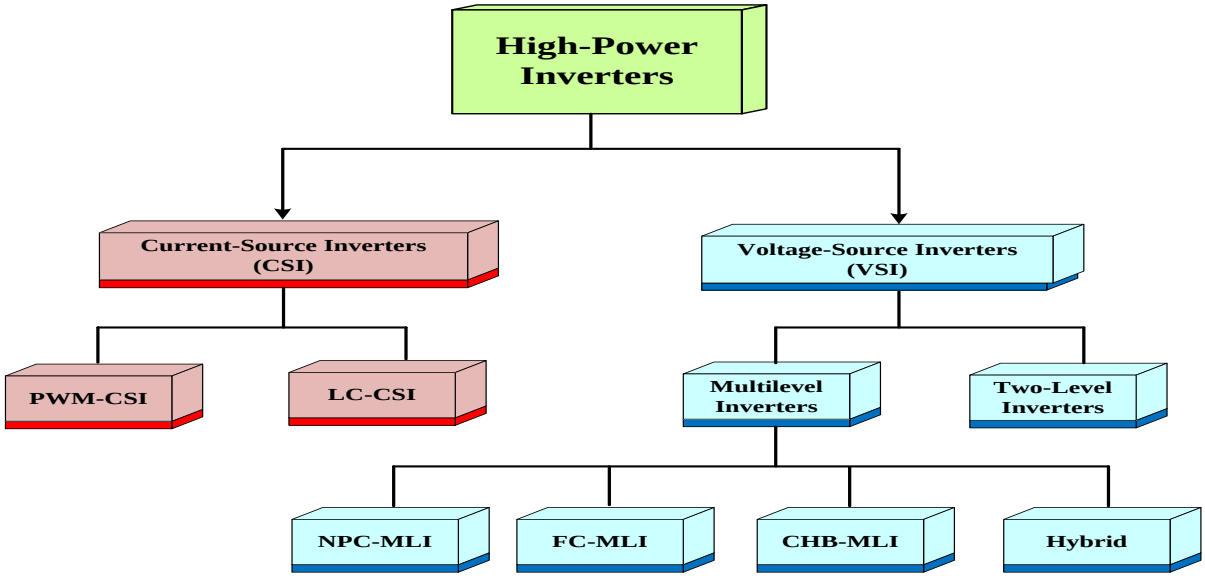


Figure 2.1 : Classification of high-power inverters.

2.2.1 Current-Source Inverters (CSI)

The current-source inverter (CSI) is a well-established technology and considered to be the classical topology for high-power inversion. It is also called a line commutated inverter (LCI) because it uses system voltage to force the commutation process between the inverter valves. It was the first technology applied for bulk power inversion and HVDC applications. In the early days of the twentieth century, the mercury-arc valve was introduced to handle high-power conversion and inversion. The first HVDC was installed between the island of Gotland and Sweden in the early 1950s. Mercury-arc valve technology has its own operational drawbacks and a limited-voltage–power-ratings ability. To overcome these problems, the thyristor or silicon-controlled rectifier (SCR) was developed, which revolutionized CSI technology . In order to increase the voltage ratings of valves, thyristors are simply connected in series; higher current ratings can be achieved by adding more thyristors in parallel, and stacking more thyristors in series and parallel for each valve results in a high-power inverter. For this reason, thyristor-based CSI is still the dominant technology for very-high-power inversion and HVDC links. The largest and longest HVDC will transmit 6.4 GW power from Xiangjiaba hydro power plant to Shanghai at 800 kV, 2071 km longline [7].

As shown in the high-power inverters classification given in Figure 2.1, there are two basic topologies for current-source inverters applied in industry, which are named: 1) load-commutated current-source inverter (LC-CSI) and 2) pulse-width modulation current-source inverters (PWM-CSI). The load-commutated inverter is considered a mature technology that has been applied for some time. It is considered a low-cost reliable topology that has a simple structure and suffers from distorted-input current and low-input power factor [7-9].

CSIs are designed in 6- and 12-pulse thyristor-based inverters. The circuit layout for a 6-pulse CSI is given in Figure 2.2. The 6-pulse CSI is basically a three-phase full-wave bridge that contains six controlled power switches – usually thyristor valves. This is known as a Greatz bridge or a 6-pulse bridge. In order to achieve higher DC voltage ratings, multiple thyristors are connected in series. However, the configuration of a 12-pulse CSI comprises two 6-pulse bridges connected in series and a phase displacement – usually 30 degrees between the phases on the AC side. The 30-degree phase displacement is achieved by connecting the AC side of one 6-pulse bridge to a delta transformer winding, while the other 6-pulse bridge is connected to a Y- (star) transformer winding as shown in Figure 2.3. The 12-pulse CSI produces fewer harmonics compared to the 6-pulse as the 5^{th} and 7^{th} harmonics are eliminated when used in the 12-pulse configuration. This results in minimizing the size of

the output filter; hence, the 12-pulse CSI is widely applied for high-power and HVDC applications.

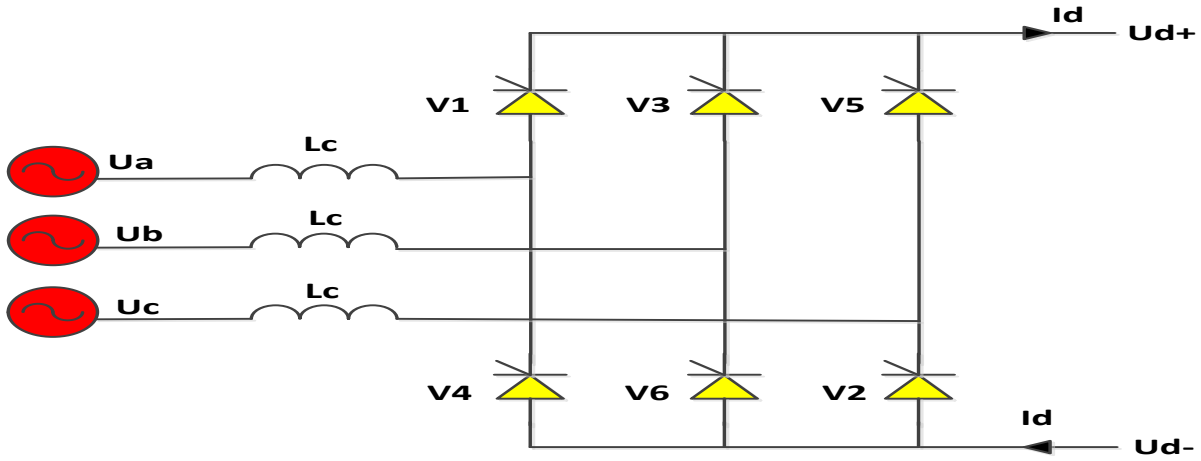


Figure 2.2: Greatz bridge (6-pulse) CSI circuit layout.

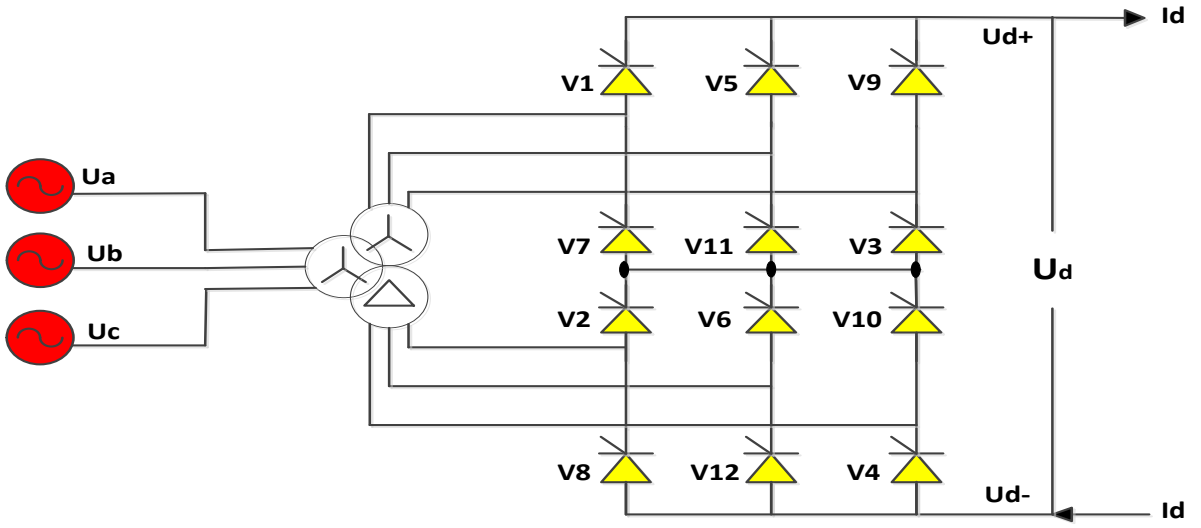


Figure 2.3: 12-pulse bridge CSI circuit layout.

Figure 2.4 demonstrates an HVDC system based on CSI technology. The main limitation of CSI is that thyristor valves can only be controlled to be turned ON and require an AC synchronous voltage source for commutation.

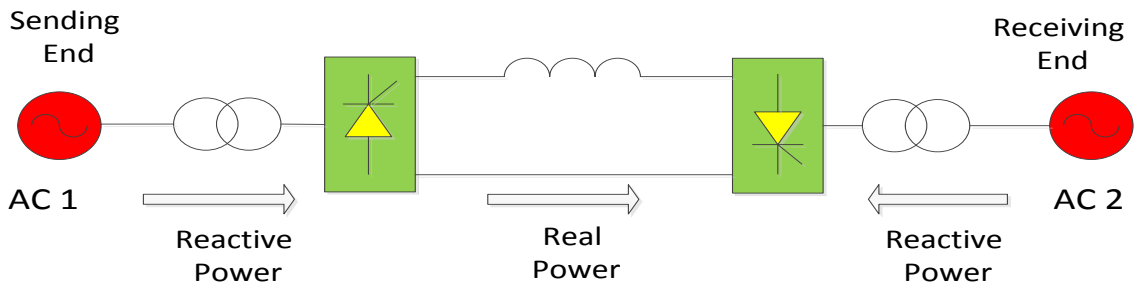


Figure 2.4 : HVDC based on current-source conversion technology.

2.2.2 Voltage-Source Inverters (VSI)

The VSI is based on the use of fully controlled semiconductors, mainly: insulated gate bipolar transistors (IGBTs), gate turn-off thyristors (GTOs) or integrated gate-commutated thyristors (IGCTs). The latter are replacing GTOs for high-power applications as IGCTs can be fully controlled to be turned ON and OFF, which gives two degrees of freedom. Nowadays, IGBTs and IGCTs are available on the market with blocking voltages of up to 6.5 kV. VSI is considered to be a new technology generation, mostly using IGBTs as a power switch. This technology is growing fast in industrial and utility power applications such as renewable energy integration and HVDC. It is a well-established technology for high-power–medium-voltage applications and is gaining attention for high-power–high-voltage applications. VSIs are also called self-commutated inverters. In such inverters, the DC voltage is considered constant and they are therefore called voltage-source inverters (VSIs), which are self-commutated as these inverters do not require an external synchronous voltage source for commutation.

VSIs are categorized into two main categories, which are: 1) two-level inverters and 2) multilevel inverters. In two-level inverters, the output-voltage waveform comprises two levels. In such a topology, it is necessary to stack many power switches in series and parallel to handle high-power ratings. This results in many operational drawbacks such as: unequal voltage distribution between stacked semiconductors, poor efficiency, reliability issues, high losses and high total harmonic distortion (THD). To overcome these drawbacks, the concept of multilevel inverters was proposed in 1975 [10]. Multilevel inverters are those producing the output-voltage waveform in three levels or more. Compared to conventional two-level inverters, multilevel inverters have the following key advantages: 1) higher output voltage at

low switching frequency, 2) low voltage stress (dv/dt), 3) lower THD, 4) less electromagnetic interference (EMI), 5) a smaller output filter and 6) higher fundamental output [11, 12].

The voltage-source multilevel inverters are classified into classical topologies and hybrid topologies. The classical topologies are named: 1) neutral-point clamped (NPC-MLI), 2) flying capacitor (FC-MLI) and 3) cascaded H-bridge (CHB-MLI). These topologies have been well established in industry for some time and are commercially available. Hybrid multilevel inverters are proposed topologies based on a combination of the two classical topologies mentioned above, or with a little modification of them [13]. Throughout the literature, numerous topologies have been proposed to suit certain applications, or to improve the original features.

In 1997, the first HVDC that implied IGBT-based VSIs was installed in Hellsjön, Sweden with ratings ±10 kV, 3 MW and 10 km distance [14]. Currently, VSIs are operated much beyond this at very high voltage and power ratings ±320 kV, 1000 MW. Figure 2.5 demonstrates an HVDC system based on VSI technology. In the next section, the three classical topologies of multilevel inverters are critically reviewed.

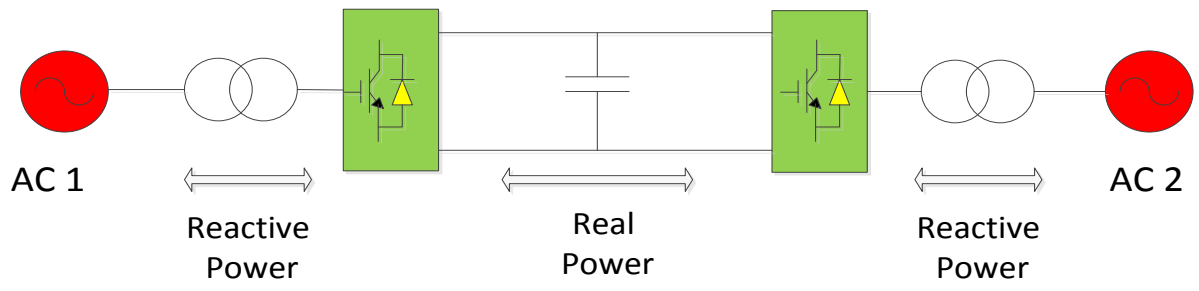


Figure 2.5 : HVDC based on voltage-source conversion technology.

2.2.3 Technical Comparison between CSI and VSI

Comparing CSI and VSI technologies, each technology has its own advantages and drawbacks. There is always a trade-off to decide which technology to use. The final decision is based on technical and economic factors and the nature of the required application. Table 2-1 presents a detailed technical comparison between CSI and VSI technologies, based on the literature review.

Table 2-1: Technical comparison of CSIs versus VSIs

Current-Source Inverters (CSIs)	Voltage-Source Inverters (VSIs)
Employing mercury-arc valves or thyristors.	Thyristor- or transistor-based technology [15].
Difficult to control, needs external AC voltage source for commutation.	Fully controllable and self-commutated.
Absorbs reactive power (Q) in operation and generates many harmonics; hence, large filter size and local Q compensation is essential.	Produces fewer harmonics; hence, smaller filter size is required and does not consume reactive power in operation, which makes it more compact. [16]
Dominant technology for high-voltage–high-power applications.	Preferable for medium-voltage–high- power applications [6].
Lower switching losses, about 0.8% per converter station [15] .	Higher switching losses. Typically, the total losses per converter in a VSI station are 1.8%.
Lower switching frequency.	Higher switching frequency can be achieved [14].
Cannot be connected to weak systems.	Has “black-start capability” [17].
Limited power control and needs local reactive power compensation.	Can control both active and reactive power independently and rapidly.
Power flow in one direction.	Bidirectional power flow is possible with VSIs [18].
Requires phase-shifting transformer.	Requires ordinary transformer.
Uses series and parallel connection of thyristors to achieve high-power ratings.	VSIs have modular and compact structure.
Commutation failure occurs in CSIs as a result of disturbances in the AC side.	This problem is eliminated when using VSIs.
Operates in two quadrants of the PQ operating plane.	VSIs operate in all four quadrants of the PQ operating plane [17].

2.3 Classical Topologies of Voltage-Source Multilevel Inverters

Many topologies have been introduced by researchers for multilevel inverters. However, most of the proposed topologies were built according to the three basic topologies that are well established in industry. The basic topologies, also known as classical (traditional) topologies, are: 1) neutral-point clamped multilevel inverters (NPC-MLI), 2) flying capacitor multilevel inverters (FC-MLI) and 3) cascaded H-bridge multilevel inverters (CHB-MLI). These classifications are shown in Figure 2.6. This section presents the theoretical background, operating principles, circuit layouts, and main features of the three classical topologies.

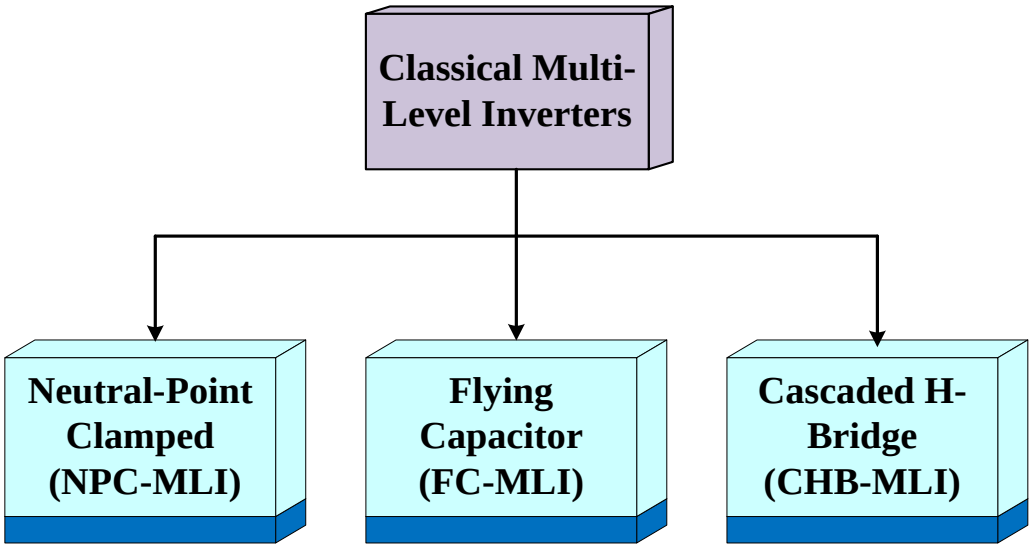


Figure 2.6: Classical topologies for multilevel inverters.

2.3.1 Neutral-Point Clamped Multilevel Inverter (NPC-MLI)

The first neutral-point clamped multilevel inverter was introduced by Nabae, Takahashi and Akagi in 1981 [19]. This was essentially a three-level inverter. It is called the neutral-point clamped inverter, based on the introduction of a neutral point as an additional level on the dc bus. Sometimes, it is called diode-clamped. This topology is very popular and commonly used in industry. Figure 2.7 illustrates the NPC-MLI single-phase circuit layout for a) three levels and b) five levels.

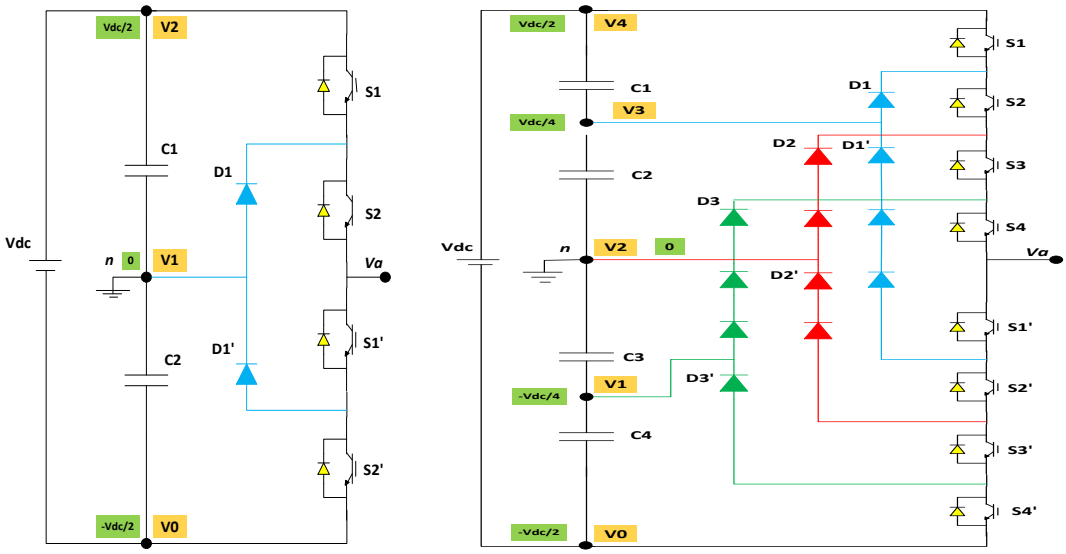


Figure 2. 7 : Neutral-point clamped multilevel inverter circuit layout for a) 3-levels, and b) 5-levels.

In this topology, for an m-level inverter, the main DC voltage V_{dc} is split by a connection of $(m-1)$ bulk series capacitors from the DC side. At steady state, the voltage across each capacitor is $V_{dc}/(m-1)$. The clamped diodes are used to limit the voltage across each active switch to one capacitor voltage. Hence, each switch is only required to block $V_{dc}/(m-1)$ voltage value. Multisteps in the output voltage can be easily generated by implementing the appropriate switching. Tables 2-2 and 2-3 present the switching states to synthesize 3- and 5-level output voltages, respectively [8, 20]

Table 2-2: Switching states for 3-level neutral-point clamped multilevel inverter (NPC-MLI)

Output voltage(V_{an})		Switch State (3-Level NPC-MLI)			
Level	Value	S1	S2	S1’	S2’
V2	$V_{dc}/2$	1	1	0	0
V1	0	0	1	1	0
V0	$-V_{dc}/2$	0	0	1	1

Table 2-3: Switching states for 5-level neutral-point clamped multilevel inverter (NPC-MLI)

Output voltage (V_{an})		Switch State (5-Level NPC-MLI)							
Level	Value	S1	S2	S3	S4	S1’	S2’	S3’	S4’
V4	$V_{dc}/2$	1	1	1	1	0	0	0	0
V3	$V_{dc}/4$	0	1	1	1	1	0	0	0
V2	0	0	0	1	1	1	1	0	0
V1	$-V_{dc}/4$	0	0	0	1	1	1	1	0
V0	$-V_{dc}/2$	0	0	0	0	1	1	1	1

For an m-level diode-clamped inverter, each phase has $(m-1)$ pairs of complementary switches. When one switch from the pair is turned on, the other complementary switch should be turned off. Tables 2.2–2.3 show that the switches that are turned on are always adjacent and in series [13]. In addition, for an m-level inverter, there should be $(m-1)$ switches turned on at a time. Table 2-4 demonstrates the required number of devices for an m-level diode-clamped inverter.

Table 2-4: Device count for neutral-point clamped multilevel inverter (NPC-MLI)

Device	Count per Phase Leg
Active Switching Devices	2 (m-1)
Freewheeling Diodes	2 (m-1)
Clamping Diodes	(m-1) (m-2)
DC Link Capacitors	(m-1)

The clamping diodes should have different voltage-blocking ratings compared to the active power-switching devices. However, when the inverter is designed in such a way that each clamping diode needs the same power ratings as the switches, $(m-1)(m-2)$ diodes are required [13, 21].

2.3.2 Flying Capacitor Multilevel Inverter (FC-MLI)

A new inverter based on the flying capacitor concept was introduced by Meynard and Foch in 1992 [12]. It was introduced as an alternative to the neutral-point clamped inverter. The basic idea behind this topology is the use of capacitors to clamp the device voltage to one capacitor voltage instead of using diodes, as with the neutral-point clamped inverter. Hence, this type of inverter is also called a capacitor-clamped invertor. Figure 2.8 demonstrates the FC-MLI single-phase circuit layout for a) three levels, and b) five levels.

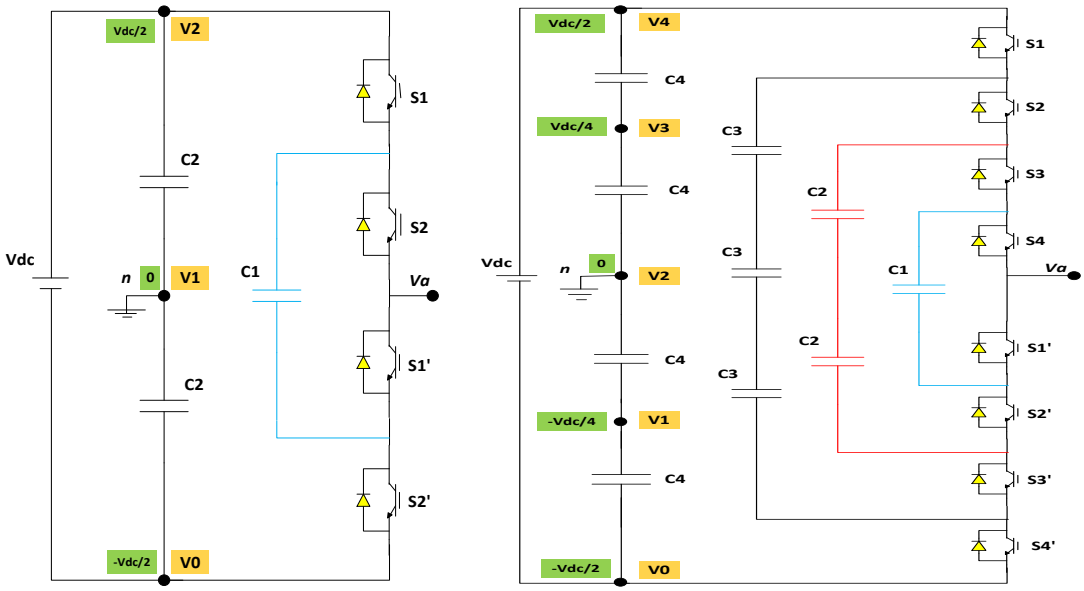


Figure 2.8: Flying capacitor multilevel inverter circuit layout for a) 3-levels, and b) 5-levels.

In this topology, as in diode-clamped inverters, for an m-level inverter, the main DC voltage V_{dc} is split by a connection of $(m-1)$ bulk-series capacitors from the DC side. These capacitors have a ladder structure in which the voltage across each capacitor differs from the voltage on the other capacitors. The voltage increase between two adjacent capacitors shapes the size of the voltage step in the output-voltage waveform [13, 22]. The clamping capacitors are used to limit the voltage across each active switch device to $V_{dc}/(m-1)$ voltage value. Multisteps in the output voltage can be easily generated using the appropriate switching of the inverter semiconductors. To illustrate this, consider the three-level multilevel capacitor-clamped inverter shown in Figure 2.8 (a). The three-level staircase output voltage can be obtained according to the switching table presented in Table 2-5. Similarly, Table 2-6 presents the switching states to synthesize a five-level inverter [8, 20].

Table 2-5: Switching states for 3-level fly capacitor multilevel inverter (FC-MLI)

Output Voltage(V_{an})		Switch State (3-Level FC-MLI)			
Level	Value	S1	S2	S1'	S2'
V2	$V_{dc}/2$	1	1	0	0
V1	0	1	0	0	1
		0	1	1	0
V0	$-V_{dc}/2$	0	0	1	1

Table 2-6: Switching states for 5-level fly capacitor multilevel inverter (FC-MLI)

Output Voltage (V_{an})		Switch State (5-Level FC-MLI)							
Level	Value	S1	S2	S3	S4	S1'	S2'	S3'	S4'
V4	$V_{dc}/2$	1	1	1	1	0	0	0	0
V3	$V_{dc}/4$	1	1	1	0	1	0	0	0
		0	1	1	1	0	0	0	1
		1	0	1	1	0	0	1	0
V2	0	1	1	0	0	1	0	0	1
		0	0	1	1	0	0	1	1
		1	0	1	0	1	0	1	0
		1	0	0	1	0	1	1	0
		0	1	0	1	0	1	0	1
		0	1	1	0	1	0	0	1
V1	$-V_{dc}/4$	1	0	0	0	1	1	1	0
		0	0	0	1	0	1	1	1
		0	0	1	0	1	0	1	1
V0	$-V_{dc}/2$	0	0	0	0	1	1	1	1

It is clear from Table 2-6 that the FC-MLI has more flexibility compared to the NPC-MLI. The flying capacitor's topology has many more redundancies for inner-voltage levels compared to the diode-clamped. This means there are two or more valid switch states that can synthesize the output-voltage waveform. As in the case of the NPC-MLI, for an m-level inverter, there should be $(m-1)$ switches on at a time. The number of devices required for an m-level FC-MLI can be found using Table 2-7.

Table 2-7: Device count for fly capacitor (FC-MLI)

Device	Count per Phase Leg
Active Switching	$2\ (m-1)$
Freewheeling Diodes	$2\ (m-1)$
Auxiliary Capacitors	$(m-1)(m-2)/2$
DC Link Capacitors	$(m-1)$

2.3.3 Cascaded H-bridge Multilevel Inverters (CHB-MLI)

The third classical topology is the cascaded H-bridge multilevel inverter (CHB-MLI). In [23], the author implemented the cascaded H-bridge multilevel inverter in medium-voltage AC drives. Figure 2.9 shows the CHB-MLI single-phase circuit layout for a) three-levels, and b) five-levels.

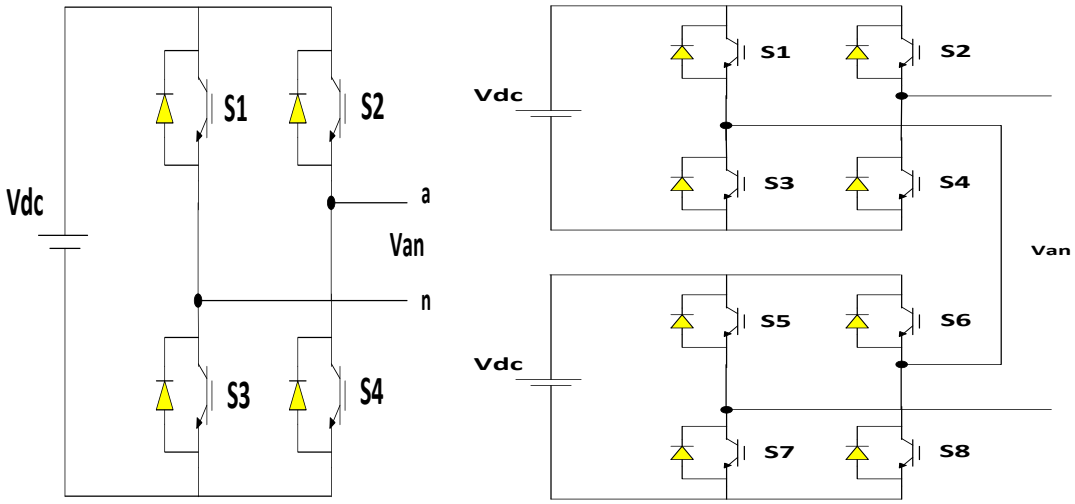


Figure 2.9: Cascaded H-bridge multilevel inverter-circuit layout for a) 3-levels, and b) 5-levels.

This topology comprises a series connection of single H-bridge inverters with separate DC sources. It has the lowest number of devices among the classical multilevel inverter topologies. The main idea is that each H-bridge cell will generate three different voltages, and the output waveform can be synthesized by the sum of the voltages generated by each cell. Each single H-bridge is able to generate $+V_{dc}$, 0, or $-V_{dc}$. This can be obtained by the appropriate selection of the four switches S1, S2, S3 and S4 of the cell. The switching states for three-level and five-level CHB-MLI are given in Tables 2-8 and 2-9, respectively [8, 20]. Assuming the number of separate DC voltage sources to be (S), the inverter can generate m-levels given by $m = (2S + 1)$. Generally, the separate DC sources (SDCS) are obtained by the use of batteries, fuel cells or solar PV cells. For reactive power flow, pre-charged capacitors are used at the dc side of the inverter. [13]

Table 2-8: Switching states for 3-level cascaded H-bridge multilevel inverter (CHB-MLI)

Output Voltage (Van)		Switch State (3-Level CHB-MLI)			
Level	Value	S1	S2	S3	S4
V2	Vdc	1	0	0	1
V1	0	1	1	0	0
		0	0	1	1
V0	-Vdc	0	1	1	0

Table 2-9: Switching states for 5-level cascaded H-bridge multilevel inverter (CHB-MLI)

Output Voltage (V_{an})		Switch State (5-Level CHB-MLI)							
Level	Value	S1	S2	S3	S4	S5	S6	S7	S8
V4	$V_{dc}/2$	1	0	0	1	1	0	0	1
V3	$V_{dc}/4$	1	0	0	1	0	0	1	1
		1	0	0	1	1	1	0	0
		0	0	1	1	1	0	0	1
		1	1	0	0	1	0	0	1
V2	0	0	0	1	1	0	0	1	1
		0	0	1	1	1	1	0	0
		1	1	0	0	0	0	1	1
		1	1	0	0	1	1	0	0
		1	0	0	1	0	1	1	0
		0	1	1	0	1	0	0	1
V1	$-V_{dc}/4$	0	1	1	0	1	1	0	0
		0	1	1	0	0	0	1	1
		0	0	1	1	0	1	1	0
		1	1	0	0	0	1	1	0
V0	$-V_{dc}/2$	0	1	1	0	0	1	1	0

The cascaded H-bridge multilevel inverter has the lowest number of device counts when compared to the diode-clamped or the flying capacitor multilevel inverters. Table 2-10 exhibits the required number of devices per phase leg for the cascaded H-bridge multilevel inverter topology.

Table 2-10: Device count for cascaded H-bridge multilevel inverter (CHB-MLI)

Device	Count per Phase Leg
Active Switching Devices	$2\ (m-1)$
Freewheeling Diodes	$2\ (m-1)$
SDCSs	$(m-1)/2$

2.3.4 Comparison of the Three Classical Multilevel Voltage-Source Inverter Topologies

The three-level neutral-point clamped inverter has been used extensively in industry for various applications. It is popular and considered to be one of the most used multilevel inverter topologies in industrial applications. The flying capacitor multilevel inverter has also been used in industry, but to a lesser degree than the neutral-point clamped and cascaded H-bridge. Both NPC-MLI and FC-MLI were found applied at a low number of levels – usually three-level to five-level as it becomes more complicated with level increase and requires a greater number of devices. Conversely, the cascaded H-bridge converter has a modular structure and has gained more attention for application in medium-power–high-voltage applications, as well as for high-power–high-voltage industrial and utility applications.

Figure 2.10 illustrates the number of devices required for each topology as the number of output-voltage levels increase. In Table 2-11, a critical comparison of the three classical topologies is presented [6, 12, 24, 25].

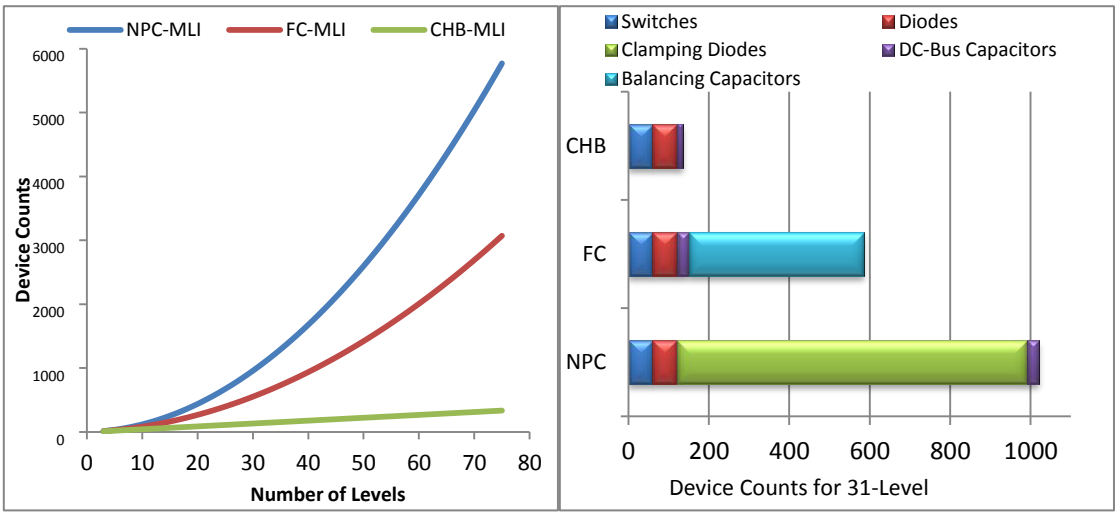


Figure 2.10: Device counts versus inverter levels for the classical topologies.

Table 2-11: Technical comparison of the three classical multilevel inverter topologies

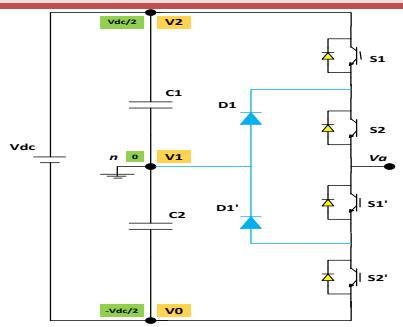
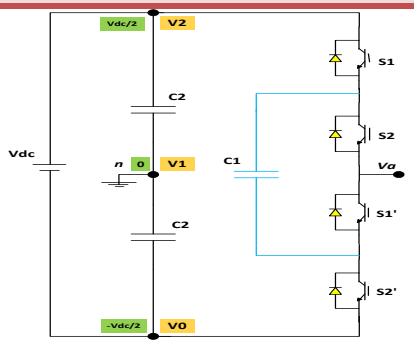
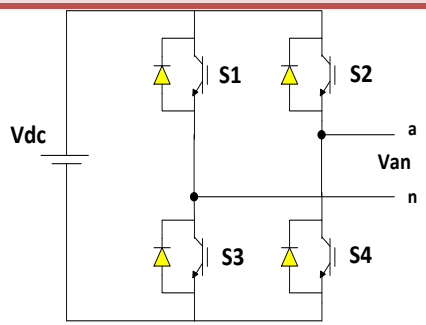
Features	NPC-MLI	FC-MLI	CHB-MLI
3-Level Circuit			
Merits	1) Common dc bus for all the phases, which results in minimum capacitor requirements. 2) Suitable and efficient for back-to-back applications. 3) Group pre-charging for the capacitors is possible. 4) High efficacy for fundamental frequency switching. 5) Fast dynamic response.	1) More switching redundancies, which might be used for balancing capacitor voltage levels. 2) Both real and reactive power flow can be controlled. 3) The existence of a large number of capacitors makes the inverter able to stay on during short outages and deep voltage sags.	1) Requires lowest number of components compared to NPC and FC. Hence, lower price and weight. The level number of generated output waveform is, m = 2S+1. 2) Easy packing as it has a modularized circuit layout. Mainly similar cell structures. 3) No need for clamping devices or voltage balancing. 4) Safe switching and inverter does not require a bulky snubber circuit.

Table 2-11 (Continued): Technical comparison of the three classical multilevel inverter topologies

Demerits	1) Difficulty in power flow for single inverter. 2) Needs a balancing method for the capacitor voltage on the dc bus. 3) The number of clamping diodes required increases quadratically with the number of level increases. 4) Diode clamping requirement and inverter packaging become more difficult with a higher number of levels.	1) Complicated control. 2) Complexity in the process of pre-charging the capacitors and start up. 3) Poor efficiency and switching utilization for real power. 4) Requires large number of capacitors, which are more expensive and bulky. 5) Packing of the inverter for high number of levels is difficult.	1) The need to use SDCSs limits the applications of this topology to those products that already have multiple SDCSs available.
Applications	1) PV systems, 2) wind turbines, 3) electrical ship propulsion, 4) train traction, 5) automotive applications: large heavy-duty trucks such as mining and military, 6) regenerative conveyors, 7) hydro-pumped storage, 8) FACTS, STATCOM, Active Filters, UPFC, UPQC, DVR and 7) HVDC.	1) PV systems, 2) electrical ship propulsion, 3) train traction. 4) automotive applications and FACTS devices such as: active power filters, UPFC, UPQC and DVR.	1) PV systems, 2) wind turbines, 3) electrical ship propulsion, 4) train traction, 5) automotive applications, 6) FACTS (STATCOM, active power filters, UPFC, UPQC and DVR) and 7) HVDC.

2.4 The Superiority of CHB-MLI for High-Power–Medium-Voltage Applications

For high-power and medium-voltage, the CHB-MLI is an attractive topology compared to a conventional two-level inverter and other multilevel topologies due to its superior merits. For high-power–medium-voltage applications, the conventional two-level inverter needs to have a series of connected semiconductors, which results in unequal voltage-sharing between connected devices as well as reliability issues [26]. The neutral-point clamped multilevel inverter (NPC-MLI) is widely applied with three levels in such applications. However, application becomes extremely complex for five levels and more as a greater number of clamping diodes is required. The same applies to the fly capacitor (FC-MLI) as it needs more capacitors for higher levels [6]. Nowadays, CHB-MLI topology is gaining more attention for use in even high-power and high-voltage applications. The main attractions and features of this topology are summarized as follows:

- The topology comprises a series of connected cascaded H-bridge cells, each connected to an SDCS to synthesize the required voltage. These multiple SDCSs make this topology suitable for integrating renewable energy sources (such as photovoltaics, fuel cells and battery storage) with the grid. [27]
- It has a modular structure and compact size, which makes it easy to construct, and it can be assembled in less time.
- It is easy to package as each H-bridge has the same structure [25].
- It has the lowest number of components for the same number of levels compared to other topologies.
- Due to its modularity, CHB-MLI can achieve higher voltage operation and higher power levels with classical low-voltage semiconductors. Higher voltage levels enable transformerless grid connection [6].
- It is commercially available at a wide range of power ratings and high number of output voltage levels, up to 17 levels [6].
- It can be operated at a low frequency when phase-shifting is applied, typically ≤ 500 Hz. This results in lower operation losses. [6]

- It does not require any clamping diodes, or capacitors. Furthermore, safe switching is possible with no bulky snubbers. [28]
- Because of its modularity, a faulty H-bridge can easily be replaced. The replacement can be done without even turning off the CHB-MLI after proper isolation of the faulty H-bridge. [25]
- This topology has more switching redundancies compared to other classical topologies. As the number of inverter levels increases, there will be an increase in the number of redundancies. This provides an advantage through enabling fault-tolerant operation. [29]

2.5 Main Modulation Techniques Applied for CHB-MLI

Different modulation schemes have been employed and developed by scholars for controlling different multilevel inverter topologies and applications. Each modulation method has its advantages and drawbacks. This section reviews classification of existing modulation techniques. Then, the most popular modulation techniques are applied in practice, and selective harmonic elimination (SHE), space vector modulation (SVM) and multicarrier sinusoidal pulse-width modulation (SPWM) are explained and discussed in detail.

2.5.1 Classification of Existing Modulation Techniques

Existing control techniques are classified mainly, based on switching frequency, into three types, which are: 1) low- (fundamental-) switching frequency modulation, 2) high-switching frequency modulation, and 3) hybrid-switching frequency modulation [13]. The classification of the most common modulation methods and the applicability of each modulation method for the three classical topologies are demonstrated in Figure 2.11. [6, 29]

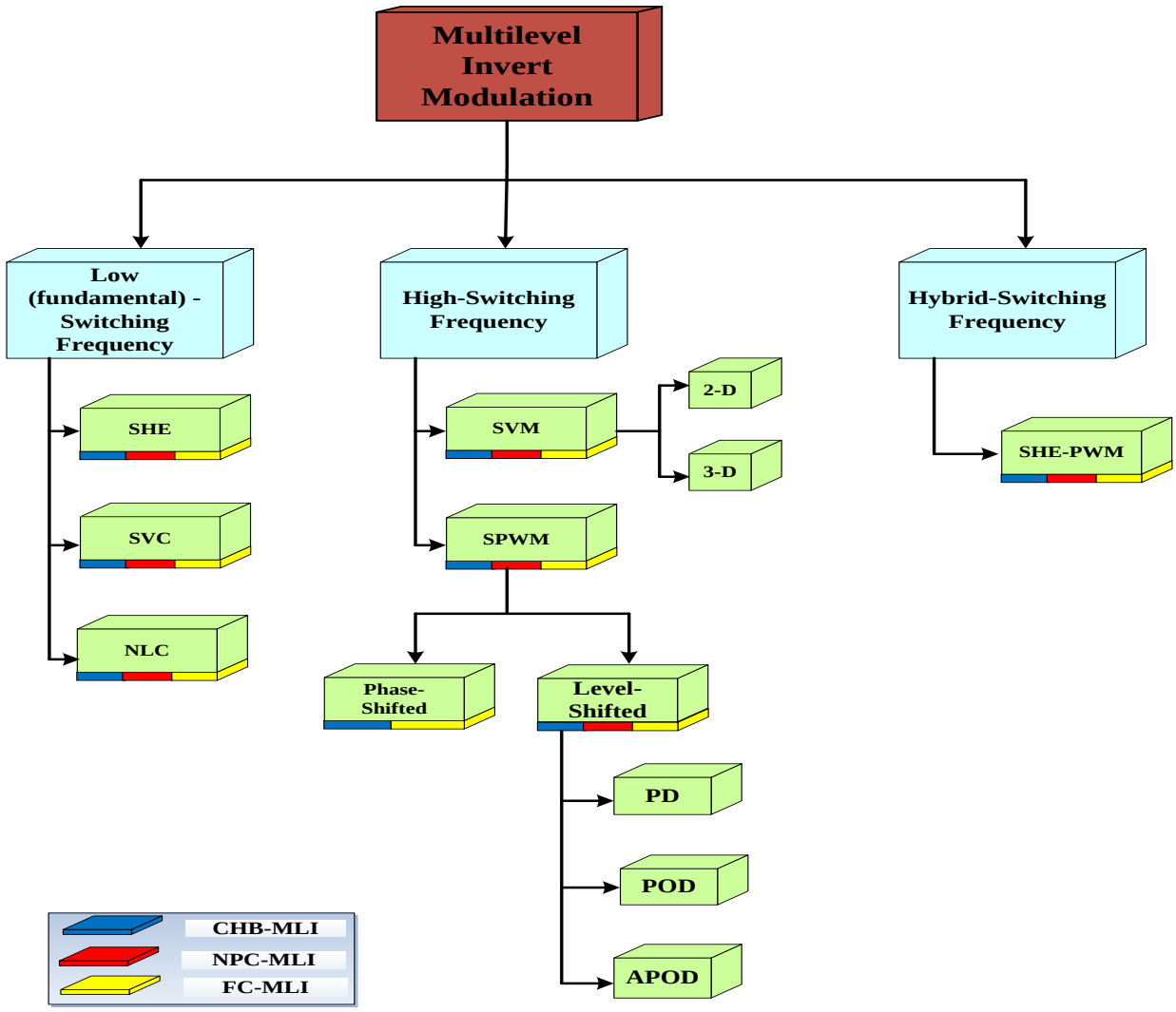


Figure 2.11: Classification of control and modulation techniques for multilevel inverters.

At high-switching frequency, the active power-switch device is commutated many times within one cycle of fundamental-output voltage. However, the active power-switch device, at low-switching frequency, is commutated only one or two times during one cycle of the output voltage [12]. In practice, those frequencies above 1 kHz are assumed to be high-switching frequency [29]. Among all different control schemes, three are mainly mentioned throughout the literature. These are: 1) selective harmonic elimination (SHE), 2) space vector modulation (SVM), and 3) sinusoidal multicarrier-based pulse-width modulation (SPWM).

2.5.2 Selective Harmonic Elimination (SHE)

Selective harmonic elimination (SHE) is a widely used low-switching frequency-control method. It is also known as the 'fundamental-switching frequency' method. It is based on the harmonic elimination theory presented by Patel and Hoft in 1974 [30]. The main concept in this modulation is to predetermine the switching angles based on Fourier analysis of the output signal, which results in eliminating a number of undesired low-order harmonics, and at the same time, in synthesizing the desired multilevel fundamental-voltage waveform. All the switching angle calculations are performed offline, so it is a pre-calculated control technique and can be classified as an open-loop control [22]. SHE is usually applied to control multilevel inverters operating in high-power applications and HVDC [29]. The proper application of SHE results in minimizing the total harmonic distortion %THD at the inverter output.

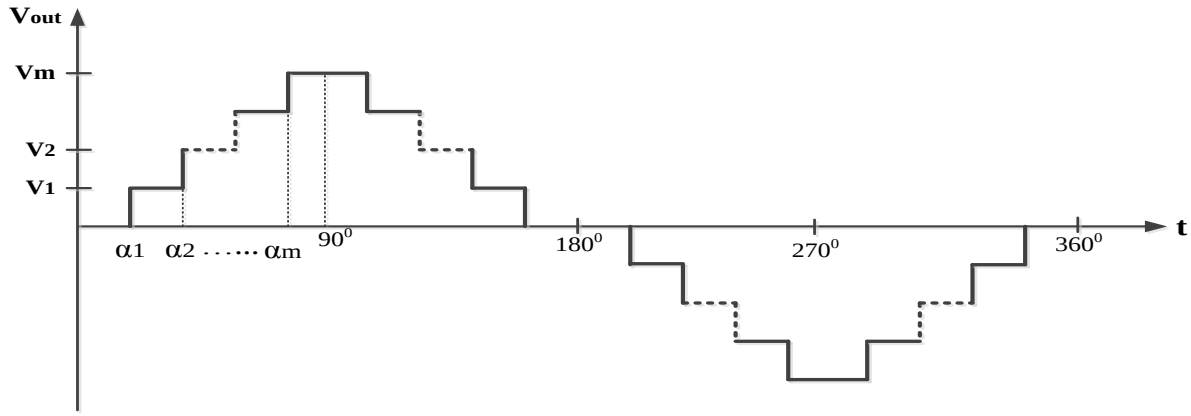


Figure 2.12: Generalized output stepped-voltage waveform for n-level inverter.

Figure 2.12 shows the generalized stepped-voltage waveform for an n-level inverter. Applying Fourier's expansion, the stepped-voltage waveform can be written as a sum of sine and cosine periodic signals, plus a dc constant. Such a signal consists of odd and even harmonics. As a result of the quarter symmetry of the waveform, the even harmonics and the dc constant are cancelled out. Hence, only odd harmonics remain. Assuming a balanced three-phase system, all triplen harmonics will be zero. For a multilevel inverter with m-levels, there will be S switching angles in a quarter cycle to be calculated in which $\left(S = \frac{m-1}{2}\right)$, and $(S-1)$ undesired low-order harmonics can

be eliminated. Mathematically, the output-stepped voltage waveform of a multilevel inverter can be written as:

$$v_{an}(\omega t) = \sum_{k=1,3,5,\ldots..}^{\infty} \frac{4V_{dc}}{k\pi}[cos(k \propto_1) + cos(k \propto_2) \ldots.. + cos(k \propto_s)]\, sin(k\omega t) \qquad 2.1$$

where S is the number of switching angles to be calculated. For CHB-MLI topology, S is equal to the number of series-connected H-bridge cells of the inverter. All switching angles, as shown in Figure 2.12, are in ascending order and smaller than 90°.

$$\theta_1 < \theta_2 < \cdots\cdots\cdots < \theta_S < 90^{\circ} \qquad 2.2$$

By solving the following system of a non-linear set of equations, it is possible to eliminate a total number, equal to (*S*-1), of low-order harmonics:

$$\begin{aligned}
&cos(\theta_1) + cos(\theta_2) + \cdots\cdots\cdots + cos(\theta_S) = S \times M_i \\
&cos(5\theta_1) + cos(5\theta_2) + \cdots\cdots\cdots + cos(5\theta_S) = 0 \\
&cos(7\theta_1) + cos(7\theta_2) + \cdots\cdots\cdots + cos(7\theta_S) = 0 \\
&\vdots \quad \vdots \quad\quad \vdots \\
&\vdots \quad \vdots \quad\quad \vdots \\
&cos(h\theta_1) + cos(h\theta_2) + \cdots\cdots\cdots + cos(h\theta_S) = 0
\end{aligned} \qquad 2.3$$

Where:

M_i is the modulation index. And $(h = 3S - k)$ is the highest harmonic order that can be eliminated. $(K = 1)$, for an even number of S, and $(K = 2)$, for an odd number of S [31].

This system of transcendental equations is a highly non-linear system and is sometimes known as SHE equations. The number of equations is equal to the number of switching angles to be calculated. In the case of CHB-MLI, the number of non-linear equations to be solved is equal to the number of series H-bridge cells.

In order to solve such a system, different techniques have been applied. Iterative and evolutionary algorithms (EA) are the most commonly used in the literature. Newton-Raphson (NR) has been applied extensively for this problem as an iterative technique. The key disadvantage is that when the inverter level increases, the algorithm becomes more difficult to converge into a solution. In addition, iterative techniques need good initial guessed switching angles to help the algorithm converge into a feasible solution. However, EA was found to be powerful and can solve the problem by applying intelligent approaches. The main idea is to transform the problem of SHE into an optimisation problem, in which the set of transcendental equations will be the constraints for the optimizer. The key attractions and drawbacks of SHE modulation are listed in Table 2-12 [12, 27].

Table 2-12: Key Attractions and Drawbacks of Selective Harmonic Elimination in Multilevel Inverters

Attractions	Drawbacks
➢ Low switching techniques and hence lower switching losses. ➢ Eliminates lower harmonics. ➢ Low %THD.	➢ Requires offline pre-calculations to determine switching angles. ➢ Becomes more complicated when solving at higher inverter levels. ➢ Narrow range of modulation index.

2.5.3 Space Vector Modulation (SVM)

One of the promising high-switching frequency control methods is space vector modulation (SVM) or SV-PWM. This method is based on the theory of vectorial representation of the three-phase system presented by Park [32] and Kron [33]. Since the 1970s, it has been used extensively and is well established for many industrial applications. This control scheme was first implemented for multilevel inverters by Choi [34]. The main attraction of SVM is the ability to analyse the three-phase systems as one system instead of dealing with each phase alone.

A three-phase system of three voltages can be represented by a unique rotating-space vector in a complex plane using Park's transformation as follows:

$$V_S = \frac{2}{3} \cdot [V_a(t) + a\,V_b(t) + a^2\,V_c(t)] \qquad 2.4$$

Where $a = e^{j.\frac{2\pi}{3}}$ and $a^2 = e^{j.\frac{4\pi}{3}}$

The main difference in SVM compared to other PWM methods is the use of a reference vector. The reference vector $(V_{Ref} = V_{\propto} + j\,V_{\beta})$ is represented in a two-dimensional plane (αβ-plane) as shown in Figure 2.13, and it can be found by applying the matrix transformation in equation 2.5.

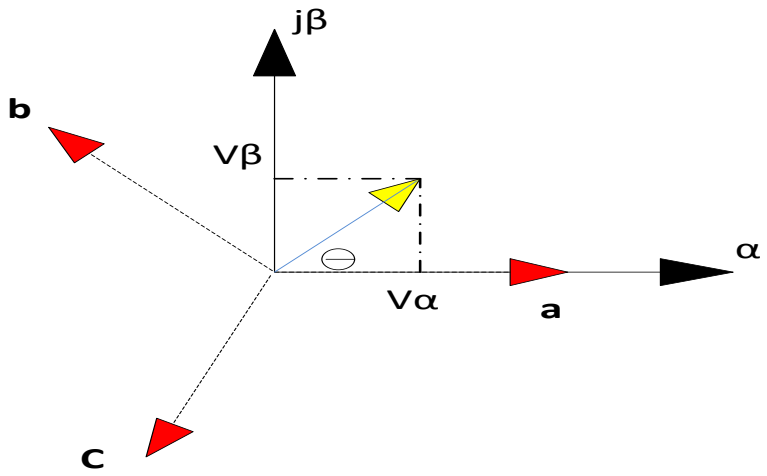


Figure 2.13: Reference vector in two dimensions.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \qquad 2.5$$

To illustrate this, it is necessary to consider the basic two-level voltage-source inverter with six switches shown in Figure 2.14.

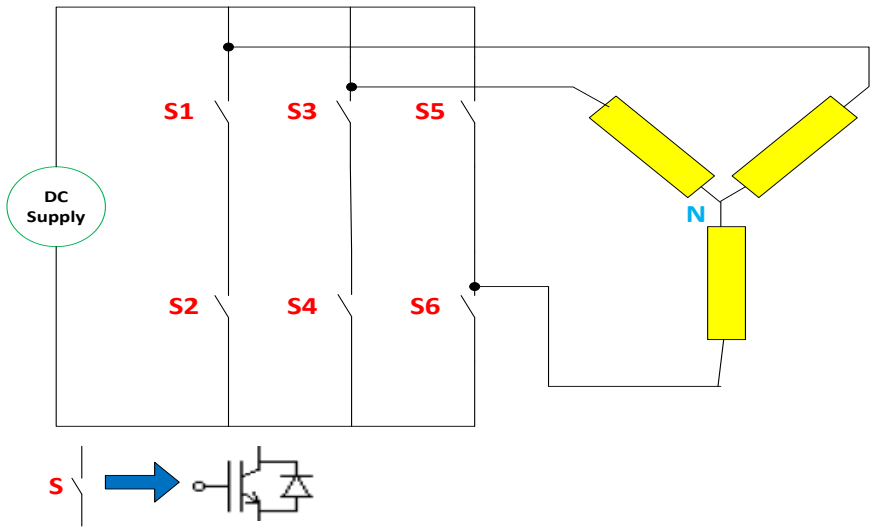


Figure 2.14: Two-level three-phase voltage-source inverter.

In the above inverter, there is a set of three upper switches and a set of three complementary lower switches. For the upper switches, the switching signal is (1) when it is ON. However, the switching signal is (0) for the lower switches to be ON. Hence, each phase (a, b or c) can either be switched from the upper switch (switch signal q=1) or the lower switch (switch signal q=0). There will be eight possible switching states as shown in Table 2-13. The generated eight-space vectors are presented in Figure 2.15. Vectors (V1–V6) are active vectors and vectors (V0 & V7) are zero vectors.

Table 2-13: Voltage Space Vectors with their Switching States for Two-Level Three-Phase Inverter

Space Vector	Switching State (q)		
	Phase A	Phase B	Phase C
V0	0	0	0
V1	0	0	1
V2	0	1	0
V3	0	1	1
V4	1	0	0
V5	1	0	1
V6	1	1	0
V7	1	1	1

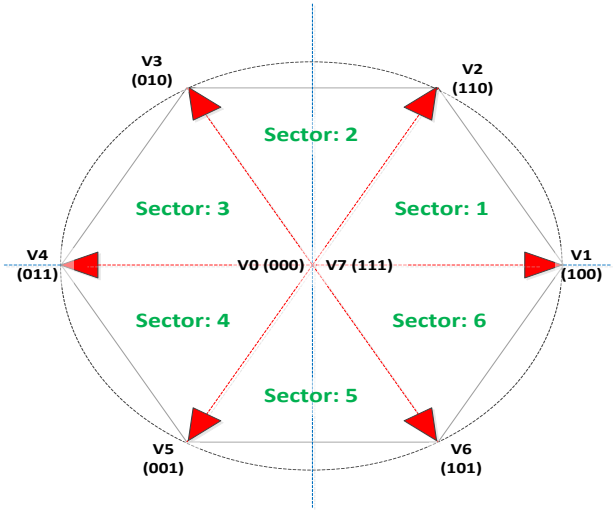


Figure 2.15: Space vector diagram for two-level three-phase voltage-source inverter.

The reference voltage can be found as the value of two active- and one zero-space vector, depending on the sector of operation. For example, if the reference voltage lies in sector 1, it can be calculated using V0, V1 and V2. In this case, $V_{Ref} = V_1.T_1 + V_2.T_2 + V_0.T_0$ in which $(T_1 + T_2 + T_0)$ is the total cycle time. The main idea here is to control the output voltages of the inverter by making their Park representation as close as possible to the reference voltage vector [22].

At steady state, the space vector should have a constant value of amplitude and should rotate at constant speed. This amplitude provides the maximum voltage that it is possible to obtain using SVM. To calculate this, the amplitude will be the value of the radius of the circle of rotation. It can be shown that the maximum line-to-line rms value of the obtained voltage is $V_{LL,max}(rms) = 0.707\, V_{dc}$, which is about 15% greater than in the case of SPWM. The main justification for this increase is that the voltage at the centre point of the winding is not fixed at $\frac{V_{dc}}{2}$ as is the case in SPWM. The voltage increase results in the ability to operate at a higher speed, making it suitable for higher-voltage applications. The SVM operates with significantly lower switching losses as it has fewer switching transitions compared to SPWM. To explain this, it is necessary to consider the modulation from V2=(110) to V3=(010), where only phase (a) switches state change. The other phases (b) and (c) remain in the same state, and hence, no switching is required for phase legs (b) and (c).

In the case of multilevel inverters, there will be more switching states and space vectors. For example, for a three-level diode-clamped multilevel inverter, there will

be 27 switching states, leading to a 19-space vector. Figure 2.16 shows the space vector diagram for a three-level inverter. The generated space vector diagrams are universal, which means they do not depend on the type of inverter used. For example, the space vector diagram shown in Figure 2.16 is suitable for all basic three-level topologies. As the levels increase, the switching redundancy increases, which make SVM difficult and complex.

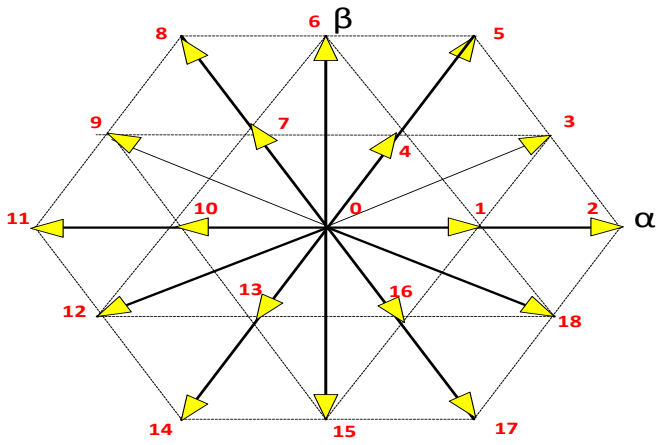


Figure 2.16: Space vector diagram for three-level inverter.

Compared to a traditional SPWM, the control of an SVM is much more complicated and difficult. However, digital signal processing (DSP) has played an important role in overcoming this complexity; hence, SVM is now used in most motor applications. The main attractions and drawbacks of SVM are presented in Table 2-14 [12, 27].

Table 2-14: Key Attractions and Drawbacks of Space Vector Modulation in Multilevel Inverters

Attractions	Drawbacks
➢ Good utilization of dc-link voltage. ➢ Fewer switching transitions; hence, significantly lower switching losses. ➢ Low current ripple. ➢ Easy-to-implement DSP. ➢ Good for high-voltage–high-power applications. ➢ 15% higher output peak voltage compared to SPWM.	➢ With the level increase of the inverter, the redundancy switching states and complexity in selecting them increases dramatically. ➢ Complicated sector identification and switching sequence.

2.5.4 Multicarrier Sinusoidal Pulse-Width Modulation (SPWM)

The sinusoidal pulse-width modulation (SPWM) is considered to be the most popular control scheme used by authors throughout the literature and in practice for multilevel inverter control. In principle, SPWM generates pulses by comparing a sinusoidal reference waveform with a triangular carrier waveform, as demonstrated in Figure 2.17.

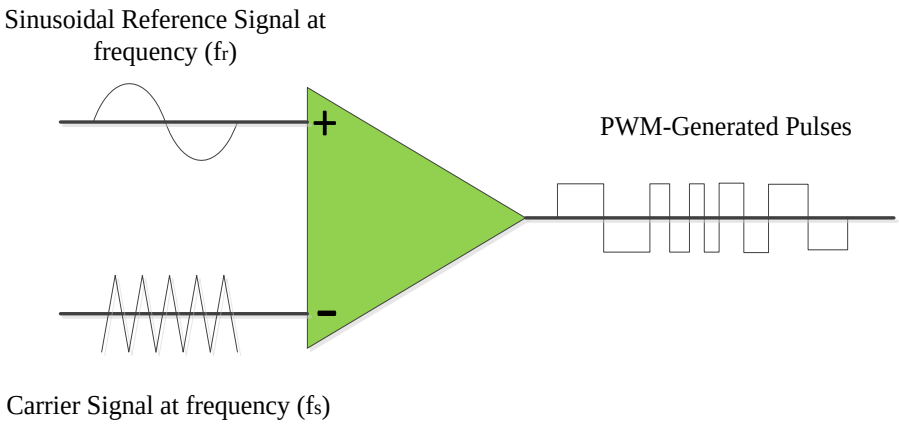


Figure 2.17: Basic principle of PWM control.

The triangular carrier waveform has a high frequency f_c (called the carrier frequency) and a peak-to-peak amplitude of A_c. The frequency of the carrier signal defines the switching frequency of the inverter and the high-order harmonic component of the output voltage. [25] However, the sinusoidal modulation signal will be at low frequency f_r (typically 50 Hz or 60 Hz) and a peak-to-peak amplitude of A_r. The frequency of the sinusoidal modulation waveform defines the required line-voltage frequency at the output of the inverter, and its amplitude controls the modulation index M_i [27].

In the case of a multilevel inverter control, there should be one reference waveform signal and multicarrier triangular waveforms. For an m-level inverter, $(m-1)$ triangular carriers are required. For the case of a cascaded H-bridge multilevel inverter, the number of carriers is equal to the number of series-connected H-bridge cells. All the carrier signals have the same value of peak-to-peak amplitude A_c and switching frequency f_c. In the control process, each carrier signal is compared to the reference waveform every time. This comparison generates a string of pulses that control the power switches. The active power switch is ON when the reference

waveform is greater than the carrier signal associated with that switch, and it is otherwise OFF.

The multicarrier SPWM control method can be classified according to the arrangement of the carrier signals into either a) phase-shifted or b) level-shifted [27]. The phase-shifted is further subdivided into: 1) phase disposition (PD), 2) phase opposite disposition (POD) and 3) alternative phase opposite disposition (APOD).

2.5.4.1 Phase-Shifted SPWM

In this technique, the carriers are disposed horizontally by a displacement-phase angle θ. This modulation is not applicable for NPC-MLI topology, but is mostly applied and suitable for CHB-MLI and FC-MLI topologies as each cell has two-level and three-level output in FC-MLI and CHB-MLI, respectively [12, 29]. Bipolar PWM and unipolar PWM can be applied to modulate each cell independently as both topologies are modular in structure. It has been proved that, to obtain the minimum distortion at the output waveform for an inverter with N_{cells}, the carrier signals should be shifted by a displacement angle $\theta = 180^0/N_{cells}$ or $\theta = 360^0/N_{cells}$ for the case of CHB-MLI and FC-MLI, respectively [12, 35]. The illustration of this modulation method is shown in Figure 2.18 for the case of a seven-level multilevel inverter. Here, the phase-0 shifted angle is $\theta = 180^0/3 = 60^0$, considering CHB-MLI topology.

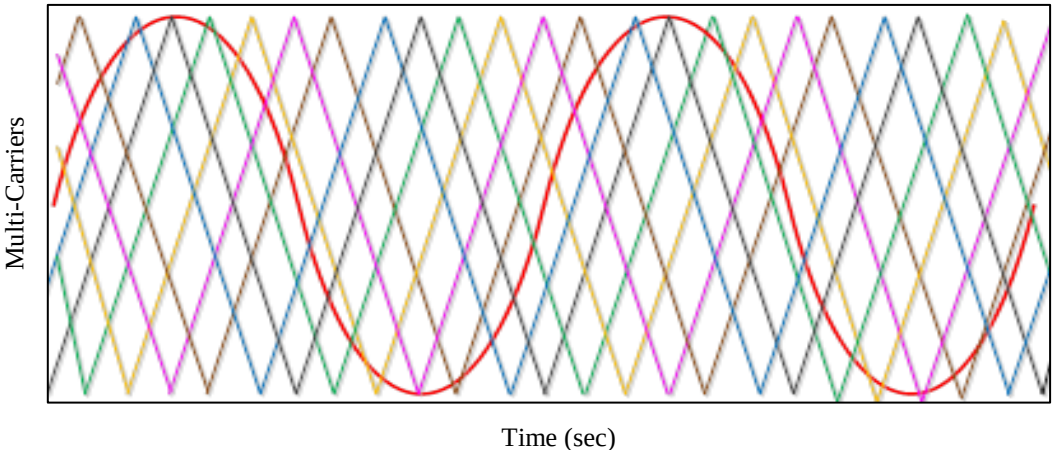


Figure 2.18: Modulation signals for seven-level inverter applying phase-shifted SPWM.

2.5.4.2 Level-Shifted SPWM

In this modulation method, all the carriers are in phase but vertically disposed. The carriers are placed to cover the whole possible amplitude range of the controlled inverter [29]. In this case, each carrier signal will represent one level. In practice, level-shifting can be applied for all the three classical multilevel inverter topologies. However, it is more practical and suitable for the NPC-MLI topology [35]. There are three categories of level-shifted SPWM, which are:

1. ***Phase disposition (PD)***, in which all carriers are in-phase. Figure 2.19 demonstrates the reference waveform and the arrangement of carrier waveforms in this type of modulation for a seven-level inverter.

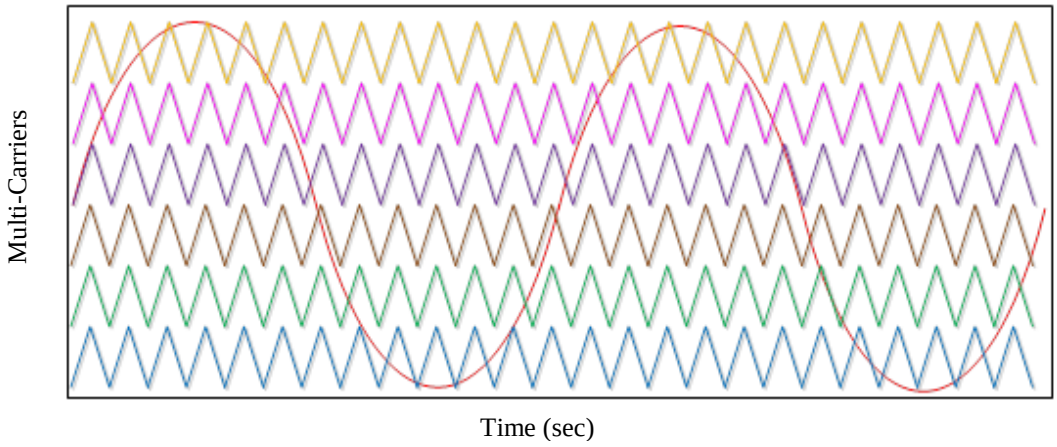


Figure 2.19: Modulation signals for seven-level inverter applying PD-SPWM.

2. ***Phase opposite disposition (POD)***, in which all carriers above the zero reference are in-phase. However, they are in opposition (shifted by 180°) from carriers below the zero reference. Figure 2.20 shows the reference waveform and carrier waveform arrangement for POD-SPWM modulation.

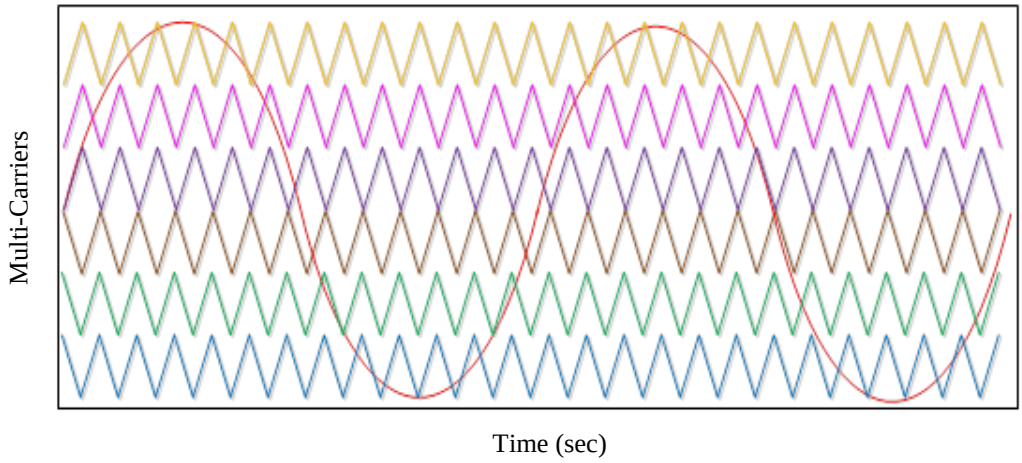


Figure 2.20: Modulation signals for seven-level inverter applying POD-SPWM.

3. ***Alternative phase opposite disposition (APOD)***, in which each carrier is shifted by 180° from the adjacent carrier. This modulation method is illustrated for a seven-level inverter in Figure 2.21

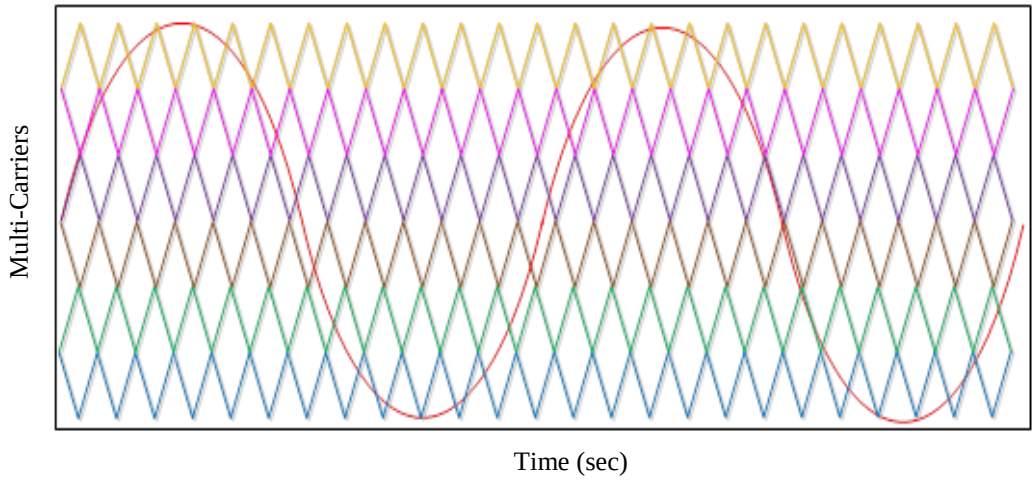


Figure 2.21: Modulation signals for seven-level inverter applying APOD-SPWM.

It was found that phase-shifted modulation generates N-time fewer switching losses compared to level-shifted modulation, where N is the number of series-connected H-bridge cells. However, level-shifted modulation results in less distortion in the output-line voltage as all carriers are in phase [8]. The known key attractions and drawbacks of SPWM modulation are listed in Table 2-15. [12, 27]

Table 2-15: Key Attractions and Drawbacks of Multicarrier SPWM in Multilevel Inverter Control

Attractions	Drawbacks
➢ Very popular and most commonly used high-switching modulation. ➢ Lower switching losses compared to other high-switching frequency modulations. ➢ Easy to implement. ➢ Lower THD compared to other control techniques.	➢ To further reduce the THD of voltage and current, it is necessary to increase the switching frequency, which significantly affects the switching losses. ➢ DC utilization is lower compared to other high-frequency control methods.

2.6 Summary

This chapter provided a general view of multilevel inverters, the main existing topologies, circuit configurations, and the applied modulation techniques for multilevel inverters. In the first part, a general classification of high-power inverters was presented. This was followed by a brief historical view of CSIs and VSIs, with an explanation of the key features of each configuration. Next was a technical comparison between CSIs and VSIs, based on the literature. This comparison indicated that there is a future for VSI technology in different power applications – including the integration of renewable energy sources into power grids. Hence, greater emphasis is placed on this technology in the second part of this chapter, which reviews the three classical topologies of voltage-source multilevel inverters. A very important comparison was made, based on the literature, which included key advantages, disadvantages, applications and device counts for the classical multilevel inverter topologies. Among the three topologies, the superiority of CHB-MLI for high-power–medium-voltage applications was highlighted and discussed. Based on the topology, technical, economical and structural features explained in section 2.4, the CHB-MLI was selected as an inverter topology for the trade-off optimisation model. In the chapter's final part, the existing modulation techniques applied for multilevel inverters were classified, and the most widely used modulations were discussed in detail.

CHAPTER 3: PASSIVE AND ACTIVE POWER FILTERS FOR HARMONIC MITIGATION – CRITICAL REVIEW

3.1 Introduction

Nowadays, the problem of power-system harmonics is attracting greater concern as a result of the rapid growth in power-electronics technology, the need for more penetration by renewable energy sources into the power system and implementation of HVDC technology. A huge amount of literature has addressed the problem of power-system harmonics. This chapter presents the problem of power-system harmonics, including: a description of the phenomena, sources of harmonics, its adverse effects on power quality, implemented solutions and existing power-harmonics standards and guidelines.

Power-harmonics filters are the most effective and widely applied techniques for harmonic mitigation in power systems and industrial applications. Throughout the literature, many circuits have been proposed, particularly over the last 30 years, for harmonics reduction. A well-implemented filter should reduce harmonics levels below the levels recommended by the international power-quality standard. Power filters are mainly categorized into passive and active filters. This chapter classifies power filters and presents a review of the most commonly applied topologies in industrial systems and utility grids. At the end of this chapter, a technical comparison is presented that highlights the key features, advantages and disadvantages of each topology.

3.2 Problem of Electrical Power Harmonics

This section reviews problems with power-system harmonics. It starts with an explanation of power-harmonics history, definition and theoretical background. Then, there is a discussion and clarification of the problem main causes and sources. Furthermore, the harmful effects of power harmonics are reviewed for the main system components. Finally, applied harmonic-mitigation techniques are classified and discussed, and the most common and well-known technical power-quality standards are briefly mentioned.

3.2.1 Description of the Phenomenon

Since the early 1990s, the phenomenon of power-system harmonics began. In 1916, Steinmetz's book was published, *Theory and Calculation of Alternating Current Phenomena*, which investigated the problem of harmonics in power systems [36]. Essentially, the nature of AC electrical voltage and current waveforms are periodic. The fundamental frequency of an electrical waveform in AC power systems can be defined as the number of repeating waveform periods within one-second duration. In any power system, the fundamental operating frequency is either 50 or 60 Hz, depending on the country's regulations; the UK system implies 50 Hz. An electrical load is said to be a "linear load", when it draws a linear current from the electrical power system in which the current is proportional to the supply voltage. Conversely, a "non-linear load" draws non-linear current from the electrical power system in which the current is non-sinusoidal. Naturally, electrical power systems have linear and non-linear loads. As a result of this, the periodic waveforms of voltage or current in electrical power systems comprise the summation of an infinite number of periodic sinusoidal waveforms in which each waveform has a frequency that is an integer multiple of the operating fundamental frequency [37] . The fundamental component of the voltage or current waveform is the fundamental frequency in which the system is designed to operate (50 Hz or 60 Hz). The other different waveforms that are at an integer multiple (> 1) of the fundamental frequency are the so-called harmonics (non-fundamental components) of the signal. The sum of all harmonics components of a waveform, including the fundamental component, is referred to as the Fourier Series of that waveform. In this dissertation, the fundamental frequency of 50 Hz has been considered throughout the analysis.

At steady state and by applying Fourier transform, periodic waveforms of voltage and currents can be expressed as follows:

$$f(t) = A_o + \sum_{h=1}^{\infty} A_h \ sin(h\omega t + \emptyset_h) \qquad 3.1$$

Where:

$f(t)$: is the time domain voltage or current waveform

A_o : is the magnitude of the dc component of the waveform

h : is the harmonic order, A_h : is the magnitude of the harmonic component h

ω : is the fundamental frequency, and $\emptyset_h$: is the phase shift of the harmonic component h

This waveform comprises odd and even harmonics, plus a dc component. The nature of non-sinusoidal current waveforms drawn by the majority of loads in power systems is symmetrical above and below its average centreline. Due to the quarter-wave symmetry of the waveform, the even harmonics and the dc component are cancelled and are almost zero. Therefore, only the odd harmonics are present. In balanced three-phase systems, all triplen harmonics (odd multiplies of third harmonics 3, 9, 15, 21…) are cancelled out to zero. In practice, harmonics up to the 50^{th} order are considered in the harmonic analysis.

Electrical power-system utilities should generate and deliver perfectly sinusoidal waveforms of voltage and currents to their customers. However, as explained, this is not practically possible because of the presence of harmonics waveforms due to non-linear currents. As a result, the non-fundamental harmonics cause deviation of the voltage and current fundamental waveforms from perfect sinusoidal waveforms. This deviation is the so-called harmonic distortion of voltage or current. Harmonic distortion in voltage and current waveforms affect the power system and the quality of power being delivered. The harmonic distortion in voltage or current waveform is measured mathematically by means of an index factor called total harmonic distortion (THD). The IEEE-519 standard defines the THD as the ratio of the rms value of all non-fundamental harmonics to the rms value of the fundamental component [3]. The voltage and current THDs are given in Equations 3.2 and 3.3, respectively.

$$\%THD_v = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_1} \times 100 \qquad 3.2$$

$$\%THD_i = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \times 100 \qquad 3.3$$

In the last decade, the technology of power-electronics components has been revolutionized and has grown very rapidly. In addition, there is a need for greater integration of renewable energy sources, such as photovoltaic systems (PV), wind turbines and fuel cells, into power systems. This leads to the extensive application of power-electronics devices and more non-linear loads in power systems, which results in more power harmonics. These harmonics have

harmful effects on power quality for both the electrical power system itself and for customers. Hence, there is currently serious concern about the THD levels in electrical power systems.

There is a great engineering challenge to investigate the harmonics problem and to keep the electrical power system operating within recommended harmonics standards to ensure delivery of quality power throughout the power system and to all customers. There are many international standards, which provide guidelines and recommendations for harmonics limits, such as Institute of Electrical and Electronics Engineers (IEEE), American National Standard Institute (ANSI) and European Norms (EN). A detailed discussion of these standards is presented later in this chapter. The following section discusses the sources of power-system harmonics in detail.

3.2.2 Sources of Power Harmonics

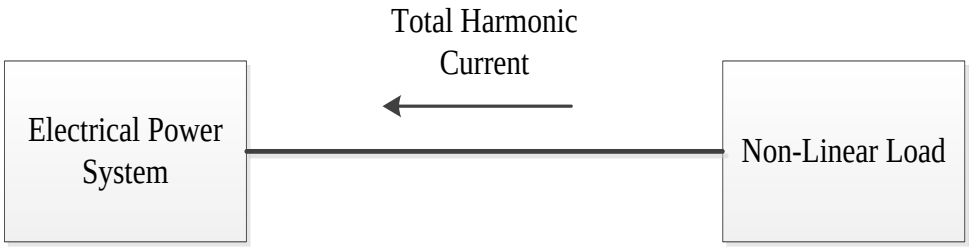


Figure 3.1 Harmonics caused by a connection of non-linear load.

As a result of non-linear loads connected to power systems, harmonic currents flow through the electrical power system, which causes voltage distortion. The flow of harmonic currents is shown in Figure 3.1. In the past, harmonic distortion was mainly caused by transformer saturation, industrial arc furnaces and other arc devices, such as welding equipment. [38] Since that time, there was a rapid growth of non-linear loads in electrical power systems. Recently, more power-electronics interfaces are required to integrate different renewable energy sources into electrical power systems. This results in an increase of harmonic distortion in distribution networks. Figure 3.2 provides a classification of the common sources of harmonics in electrical power systems [39].

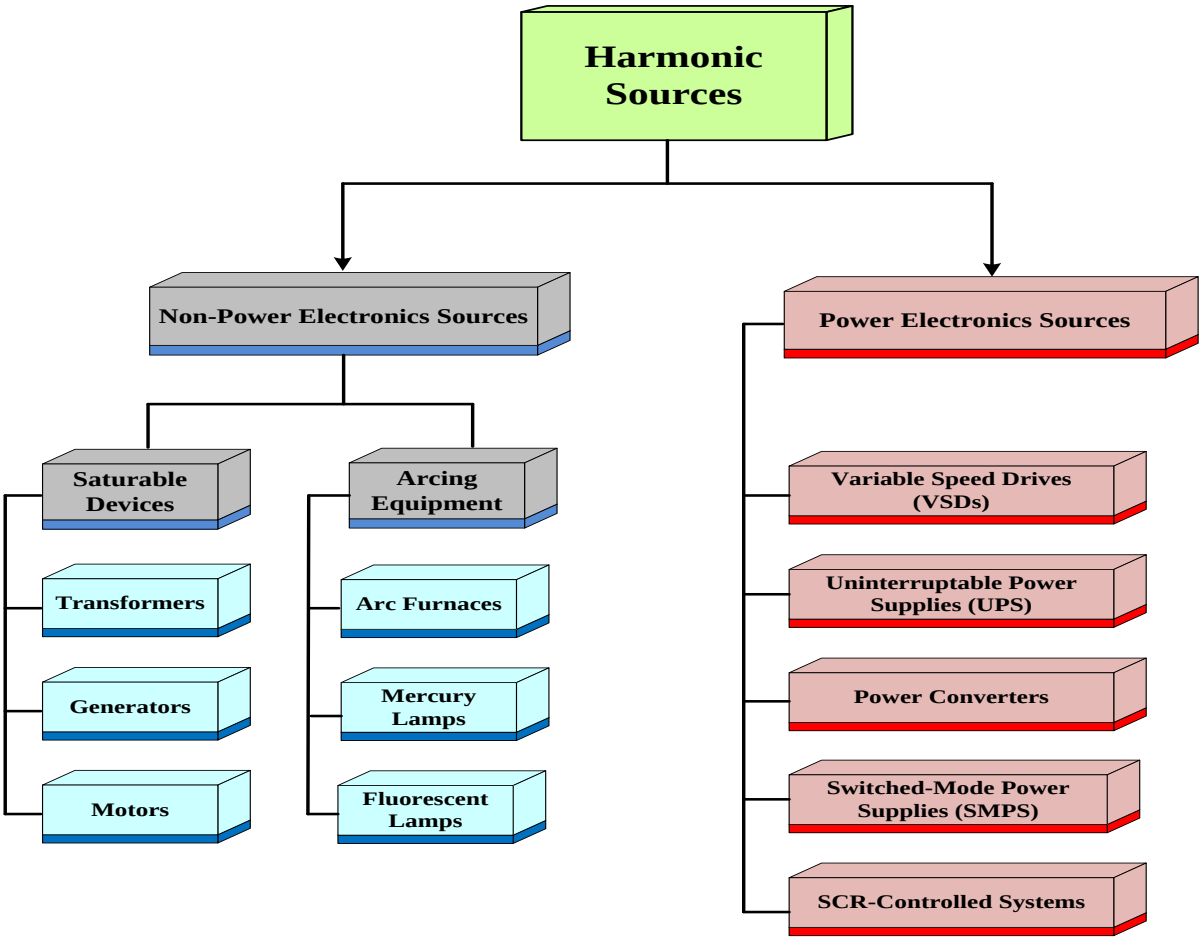


Figure 3.2: Classification of the common sources of harmonics in electrical power systems.

3.2.2.1 Non-Power-Electronics Sources

This category includes sources that have existed for some time and which are not related to the technology of power electronics; these are the classical or traditional sources of harmonics. The causes of harmonics in this category are either due to non-linear relationships between voltage and current, as in the case of arc devices. Alternatively, they result from nonlinearity of the magnetic core due to electromagnetic saturation, which occurs in rotating machines and power transformers. Typical sources in this category are: 1) power-transformer saturation, 2) rotating machines (synchronous generators, induction motors, refrigerators, freezers, air conditioning) and 3) arc devices (electrical furnaces, soldering equipment, fluorescent lamps, mercury-vapour or high-pressure lamps).

3.2.2.2 Power-Electronics Sources

This category of harmonics sources is considered new compared to the first category as it relates to the technology of power electronics. As a result of rapid development in the area of power electronics, most harmonics in power systems come from this category. The switching of power semiconductor devices associated with the control of power-electronics circuits generates harmonics. This switching is required for power converters, including AC/DC converters, DC/AC inverters, DC/DC choppers and AC/AC cycloconverters. Such power conversion and control is required for different applications in power systems such as electrical drives, renewable energy sources and HVDC applications. Other power-electronics applications include VAR compensators and power-factor improvement. In addition, power electronics are applied in switch-mode power supplies. In summary, the harmonic sources of this category include: 1) power-electronics converters (converters, inverters, choppers and cycloconverters), 2) static VAR compensators and capacitor banks and 3) switch-mode power supplies (typically, personal computers, televisions, fax machines, printers, home-entertainment devices, battery chargers and UPS).

3.2.3 Adverse Effects of Power Harmonics on Power Quality

Harmonic-current flow in electrical power systems causes several technical and economic problems. The adverse effects of harmonics on electrical power systems can be summarized as [40, 41]:

- Series and parallel resonance, which result in increased harmonics levels.
- Lower efficiency of generation, transmission and power delivery.
- Reduced life of insulation for power-system components.
- Malfunctioning power-system equipment.

However, each power-system component has a different sensitivity and reaction to harmonic distortion. In Table 3-1, the undesirable effects of power harmonics on the main components in electrical power systems are displayed separately for each component.

Table 3-1: Effects of Power Harmonics on Power-System Components

Device	Effects
Transformers	➢ Increase in core losses as a result of an increase in iron loss. ➢ Increased copper and stray flux losses. ➢ Overheating conductors and winding-insulation stress, which reduce their life and efficiency. ➢ A possibility of resonance between the transformer inductance and system capacitance and small core vibrations, which cause audible noise [42]
Rotating Machines	➢ Increased heating as a result of loss increase. ➢ The temperature increase in the machine winding reduces the service life of the machine. ➢ There might be an interaction between the airgap flux density and the fluxes generated by harmonic current in the rotor, which produces mechanical oscillation or pulsating torque [43]. ➢ Because of the differences between harmonic frequencies, an audible noise is produced [42].
Conductors	➢ Conductor (I^2R) losses increase due to carrying harmonic currents. ➢ This results in more heating of the conductor.
Circuit Breakers and Fuses	➢ Failure of the interruption capability of the circuit breaker. ➢ At low-level faults, the load current might contain a high component of distortion current. This makes high di/dt at zero crossing, making it difficult for the circuit breaker to interrupt. ➢ The need to consider higher rms current caused by harmonics in fuse settings to avoid improper operation.
Lights	➢ Light flickering, which for some lamps might not be convenient for the human eye. ➢ Operating continuously at slightly increased rated voltage significantly reduces lamp life.
Telephone Interference	➢ Possibility of power frequency interference with telephone communication between power lines and telephone lines connected on the same poles. ➢ The interface mechanism might occur by inductive, capacitive or conductive coupling [42, 43].
Capacitance	➢ Major concerns about the possibility of system resonance. ➢ With the increase in harmonics frequency, capacitive reactance decreases, which results in high harmonic currents flowing into capacitor banks. ➢ Overloading of capacitor bank and higher dielectric stress, which reduces the operating life of these banks [43].
Protective Relaying	➢ Harmonics may cause malfunction of protective relays. ➢ Harmonic distortion has significant effects on low-level faults, which needs to be considered for proper operation of the protection system [42] .

3.2.4 Implemented Solutions for Harmonics Mitigation

There are several well-established techniques for harmonics mitigation in electrical power systems. These techniques can be classified into two main categories, which are [44]: 1) internal solutions and 2) external solutions. Internal solutions are those that can be applied within existing system components. Common internal solutions include: choice of transformer connection, using higher pulse converters, or modification of electric circuit configuration. External solutions include: application of passive power filters or active power filters. In some applications, hybrid harmonic mitigation, which combines the use of two solution techniques, can give better results. Figure 3.3 presents a general classification of applied harmonic-mitigation techniques [45-47].

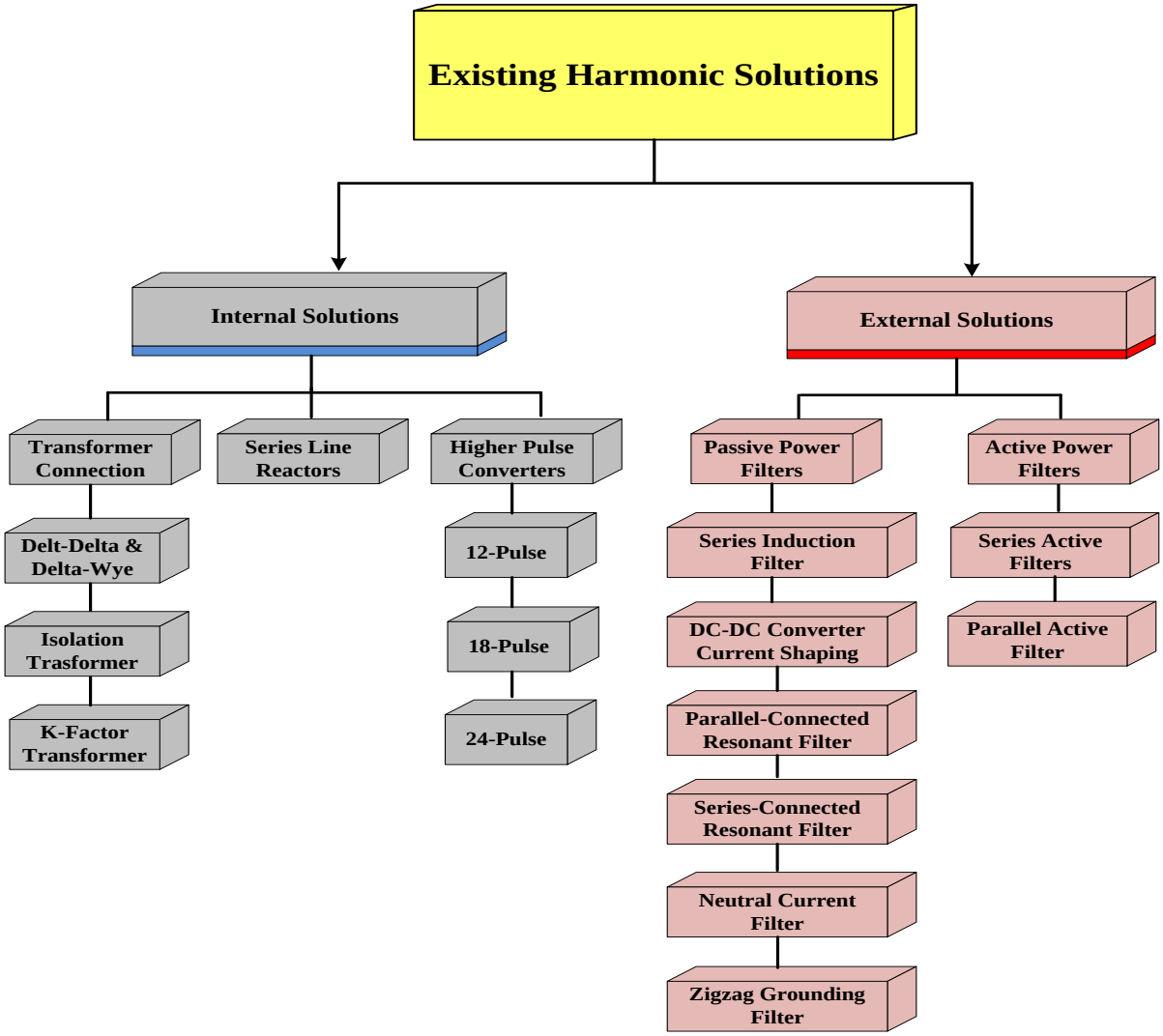


Figure 3.3: General classification of applied harmonic-mitigation techniques.

3.2.5 Power-Quality Standards: Harmonics in Power Systems

There are many technical standards that provide guidelines to engineers for the accepted levels of harmonics in power networks. The most popular and widely applied standards in the world are: IEEE-519, and IEC 61000. In this dissertation, the guidelines, recommendations and limits of the IEEE-519 standard have been followed.

The IEEE-519 standard "The IEEE Recommended Practice and Requirements for Harmonic Control in Electrical Power Systems" was issued in 1981 to provide guidelines, recommendations and limits for communication notching, voltage-distortion flickering and telephone interference generated by power converters [38]. In 2014, the standard was revised to make it more general and practical for application in power systems. Table 3-2 demonstrates the recommended limits of voltage distortion at point of common coupling PCC as given by the IEEE-519 [3].

Table 3-2: IEEE-519 Standard Recommended Voltage-Distortion Limits at PCC

Bus Voltage at PCC	Individual Voltage Distortion	Total Voltage Distortion THD
$1\ kV < V \leq 69\ kV$	3.0 %	5.0 %
$69\ kV < V \leq 161\ kV$	1.5 %	2.5 %
$V > 161\ kV$	1.0 %	1.5 %

3.3 Passive Power Filters (PPF)

This section reviews passive power filters (PPF). A general classification of PPF, based on the type of connection, is presented first. Then, each category is illustrated by discussing its circuit layout, operating principle, mathematical model and key features in brief.

3.3.1 Classification of Passive Power Filter (PPF)

A Passive Power Filter (PPF) comprises passive electrical elements such as resistors, inductors and capacitors; hence the term passive filters. Throughout the literature, many circuits with different configurations, employing passive filters, have been proposed for harmonic mitigation in power systems. The proposed passive power filters can be categorized, based on their connection, into: 1) series-connected PPFs, and 2) shunt-connected PPFs. This classification is illustrated in Figure 3.4. Compared to other harmonic-mitigation techniques, PPFs are simple, cheap and effective.

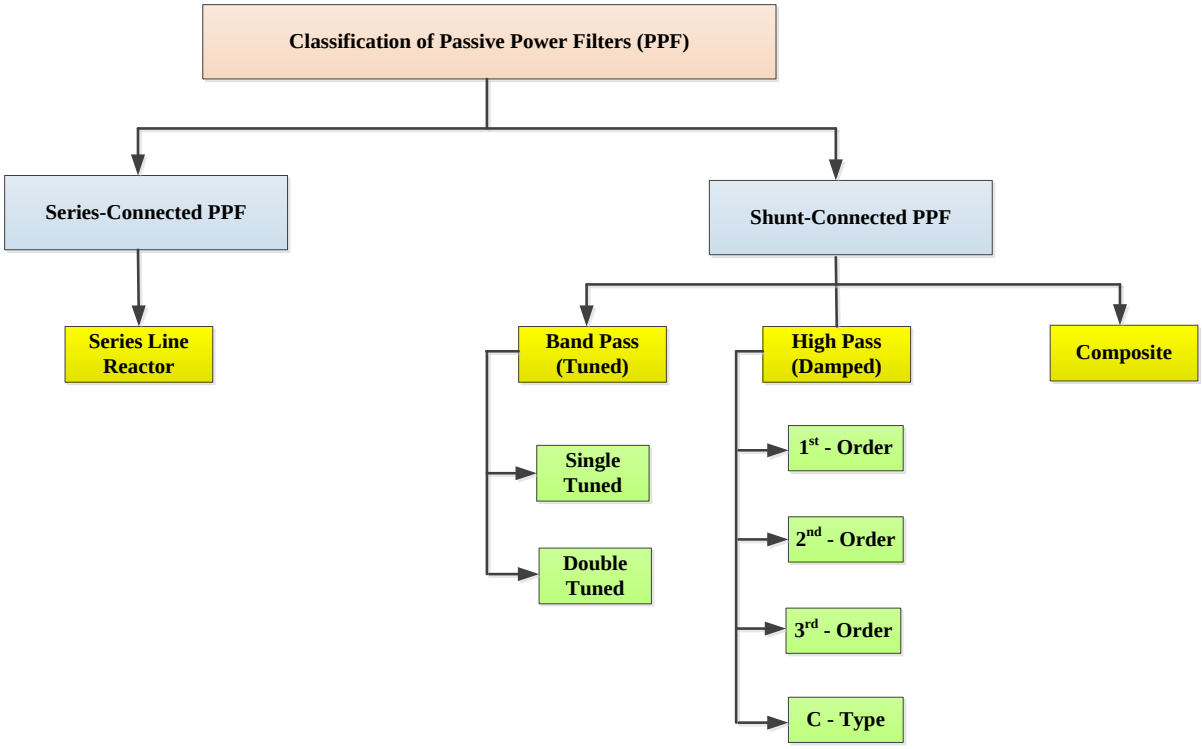


Figure 3.4: General classification of passive power filters (PPFs).

3.3.2 Series-Connected Passive Power Filters

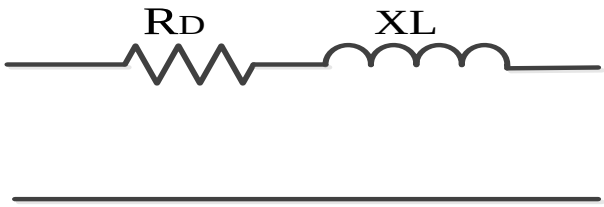


Figure 3.5: Series-connected passive power filter.

Series-connected power filter topology is essentially a reactor and damping resistor connected in series with the non-linear load; this is shown in Figure 3.5. The series-connected reactor acts as low-pass filter. It is designed to block the high harmonics as it provides high impedance for higher harmonics. However, it passes fundamental and low harmonics. The harmonic reduced by this filter is limited and usually not able to satisfy recommended standards. By increasing the inductance of the filter, more harmonic reduction can be obtained. However, this will result in a worse voltage drop and displacement factor [48]. This topology has several advantages as it is simple, cheap, small and does not cause resonance with the system. However, it results in minimum harmonic reduction and handles the full-

rated current [49]. Figure 3.6 illustrates the filter-impedance harmonic frequency characteristic with different damping resistors.

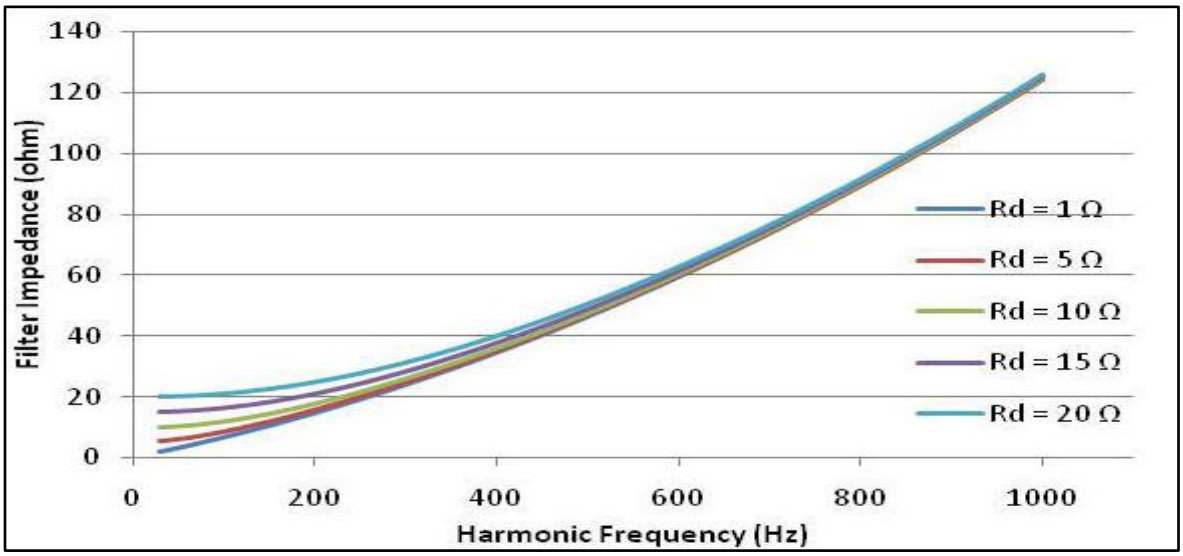


Figure 3.6: L-filter impedance-harmonic frequency characteristic with different damping resistors. [49]

3.3.3 Shunt-Connected Passive Power Filters

These filters are connected as shunt elements and are the most widely used in harmonic mitigation. Essentially, they are classified into: 1) single-tuned, 2) double-tuned, 3) high-pass and 4) composite. Each class is explained below.

3.3.3.1 Single-Tuned Passive Power Filters

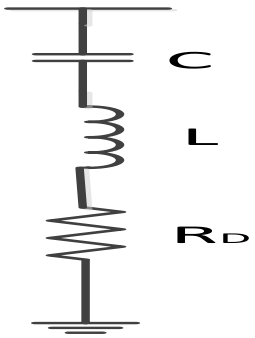


Figure 3.7: Single-tuned passive power filter (ST-PPF).

A single-tuned passive power filter is connected in shunt at PCC. It consists of a resistor (R), an inductor (L) and a capacitor (C) connected in series as shown in Figure 3.7. The word

"tuned" for passive filters means that the filter's inductive and capacitive reactances are equal at the tuned frequency of the filter. The tuning's sharpness is determined by the filter's quality factor (Q) [40].

$$Q = \frac{\sqrt{L/C}}{R} \tag{3.4}$$

For the single-tuned low-order harmonic, the quality factor is set high for sharp tuning. Conversely, low-quality factor values cover a wide range of harmonic frequencies and are usually applied for a high-pass filter. Single-tuned filters are the most-used solution in industrial applications [50]. The impedance of a single-tuned filter is given as:

$$Z = R + \left(\omega L - \frac{1}{\omega C}\right) \tag{3.5}$$

When tuned at the nth harmonic, inductive and capacitive reactances becomes equal; hence, filter impedance is lowest at the harmonic frequency f_n. This makes the nth harmonic-current flow through the filter (trapped); hence, it is eliminated from the power system. The filter design equations in this case are:

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{3.6}$$

$$Q = \frac{1}{\omega_n RC} = \frac{\omega_n L}{R} \tag{3.7}$$

Where, $(\omega_n = 2\pi f_n)$ is the angular frequency of the nth harmonic, Q is the quality factor of the filter. Figure 3.8 demonstrates the filter impedance-harmonic frequency characteristic with different quality factors.

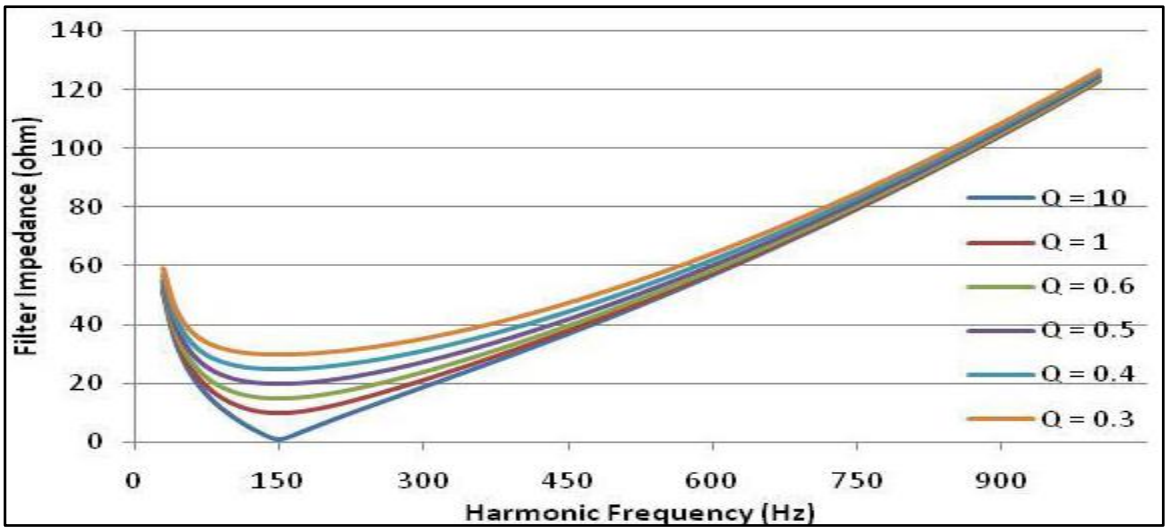


Figure 3.8: ST filter impedance-harmonic frequency characteristic with different quality factors. [49]

3.3.3.2 Double-Tuned Passive Power Filters

The double-tuned passive filter circuit configuration is shown in Figure 3.9. This topology is more difficult to tune compared to a single-tuned filter. However, it can eliminate two harmonics with the same filter. In practice, this filter is not popular and an application of two single-tuned filters is preferred. The following are the main advantages of double-tuned filters over two single-tuned filters [50]: 1) low power losses, 2) compact and 3) require only a single breaker. The disadvantages of this configuration include: 1) difficult tuning and 2) more sensitive in frequency to component values. The design equations for a double-tuned filter are as follows:

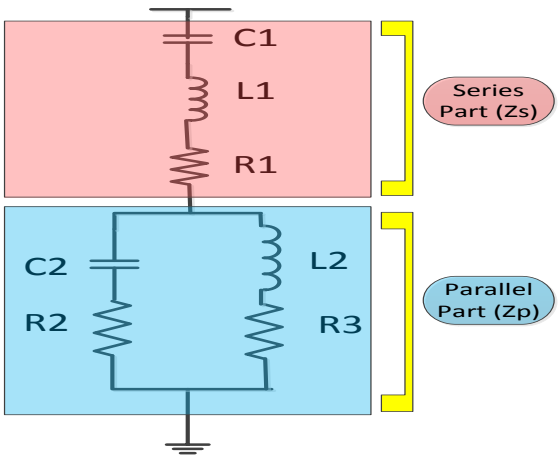


Figure 3.9: Double-tuned passive power filter (DT-PPF)

$$\omega_s = \frac{1}{\sqrt{L_1 C_1}} \quad 3.8$$

$$\omega_p = \frac{1}{\sqrt{L_2 C_2}} \quad 3.9$$

$$\omega_s = \frac{\omega_{n1}\omega_{n2}}{\omega_p} \quad 3.10$$

$$C_2 = \frac{\omega_s^2}{\omega_{n1}^2+\omega_{n2}^2-\omega_p^2-\omega_s^2}\, C_1 \quad 3.11$$

$$C_1 = \left\{\omega_1 \left(\frac{\omega_p}{\omega_{n1}\omega_{n2}}\right)^2 - \frac{1}{\omega_1} + \frac{\omega_1[(\omega_{n1}^2+\omega_{n2}^2-\omega_p^2)\omega_p^2-\omega_{n1}^2\omega_{n2}^2]}{\omega_{n1}^2\omega_{n2}^2(\omega_p^2-\omega_1^2)}\right\} \frac{U^2}{Q_F} \quad 3.12$$

3.3.3.3 High-Pass Passive Power Filters

High-pass filters are the second category of shunt filters, and they are also called damped filters. The circuit layout for the high-pass filter is illustrated in Figure 3.10 for 1st order, 2nd order, 3rd order and C-type circuit configurations. This topology is configured at a cutoff frequency f_c. Its operation principle is to provide low impedance for a wide spectrum of frequencies higher than the cutoff frequency $> f_c$ [40]. However, the filter provides high impedance for frequencies lower than the cutoff frequency $< f_c$. The filter design equations for the high-pass passive filter are given as:

$$\omega_n = \frac{1}{RC} \quad 3.13$$

$$Q = \frac{R}{\sqrt{L/C}} \quad 3.14$$

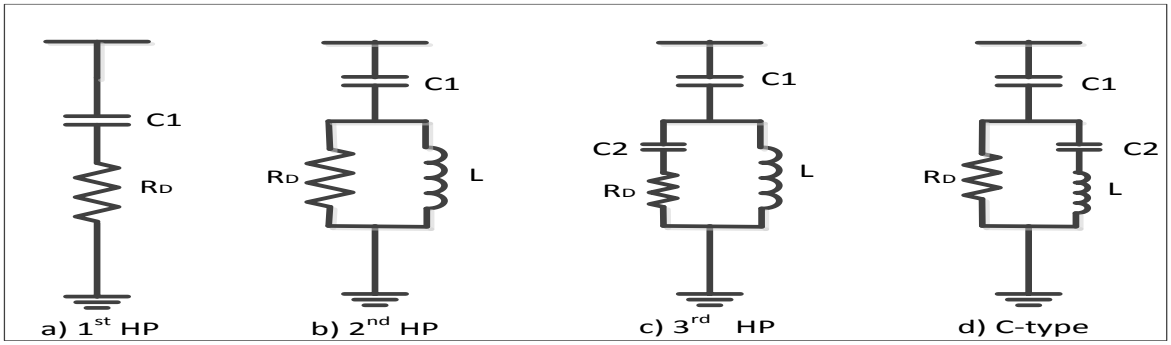


Figure 3.10: High-pass passive power filter configurations (HP-PPF).

The 1st order high-pass filter circuit consists of simply a capacitor and a resistor connected in series as shown in Figure 3.10-(a). Compared to other high-pass filters, the 1st order high-pass filter experiences higher power losses at fundamental frequency [51]. Furthermore, a greater capacitor size is required for better reduction of harmonics, which results in reactive power overcompensation and increases filter costs. Consequently, the 1st order high-pass filter is not preferred in industry. Figure 3.11 shows the filter-impedance harmonic frequency characteristic with different damping resistors.

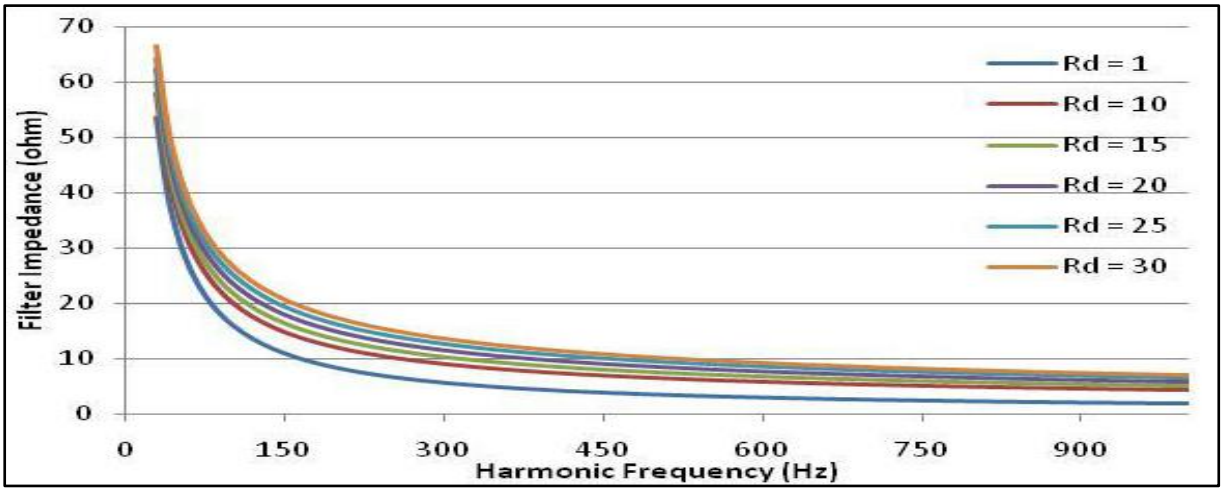


Figure 3.11: 1st-HP filter-impedance harmonic frequency characteristic with different resistors. [49]

The 2nd order high-pass filter circuit layout is shown in Figure 3.10-(b). The circuit consists of a capacitor connected in series with a parallel inductor and a resistor branch. This filter topology is the most widespread and preferred high-pass filter applied in industrial and utility systems [51]. Its topology is simple in design and has low-power losses compared to the 1st order topology. Filter parameters are designed so that the filter acts like a single-tuned filter for tuned frequencies and like a 1st order high-pass filter for higher frequencies [49]. Figure

3.12 depicts the filter-impedance harmonic frequency characteristic with different quality factors.

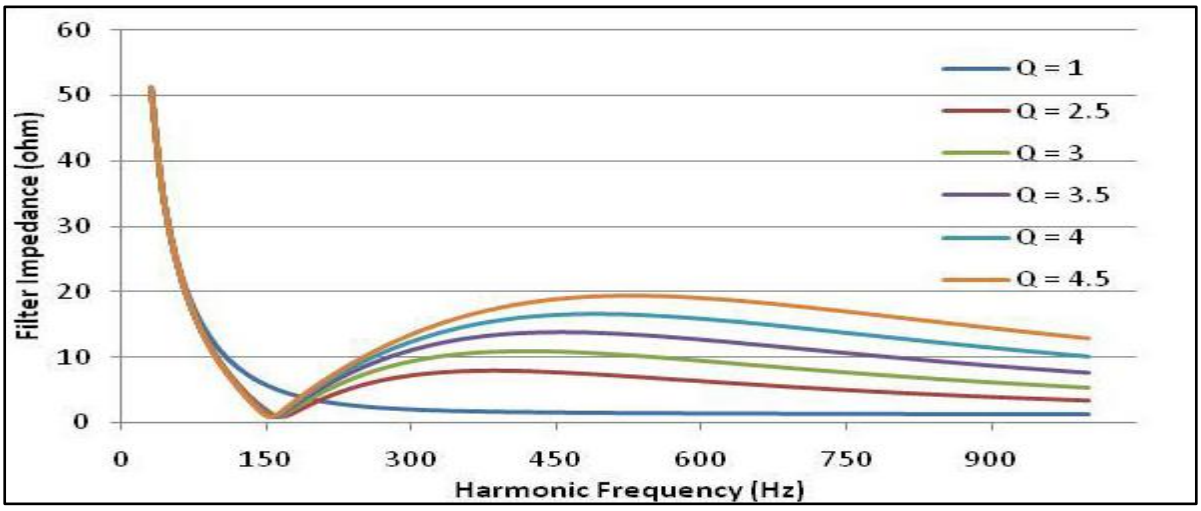


Figure 3.12: 2nd-HP filter-impedance harmonic frequency characteristic with different quality factors. [49]

The third configuration of the high-pass filter is the 3rd order topology illustrated in Figure 3.10-(c). Compared to the 2nd order filter circuit, there is an additional capacitor in series with the resistor. Actually, the 2nd order filter performs better than the 3rd order filter, but the 3rd order filter offers the advantage of lower power loss [51]. This filter topology provides high capacitive impedance at the fundamental frequency and low resistive impedance over high frequencies [49]. The 3rd order high-pass filter is more complex in design compared to the 2nd order filter. Figure 3.13 shows the filter impedance-harmonic frequency characteristic with different quality factors.

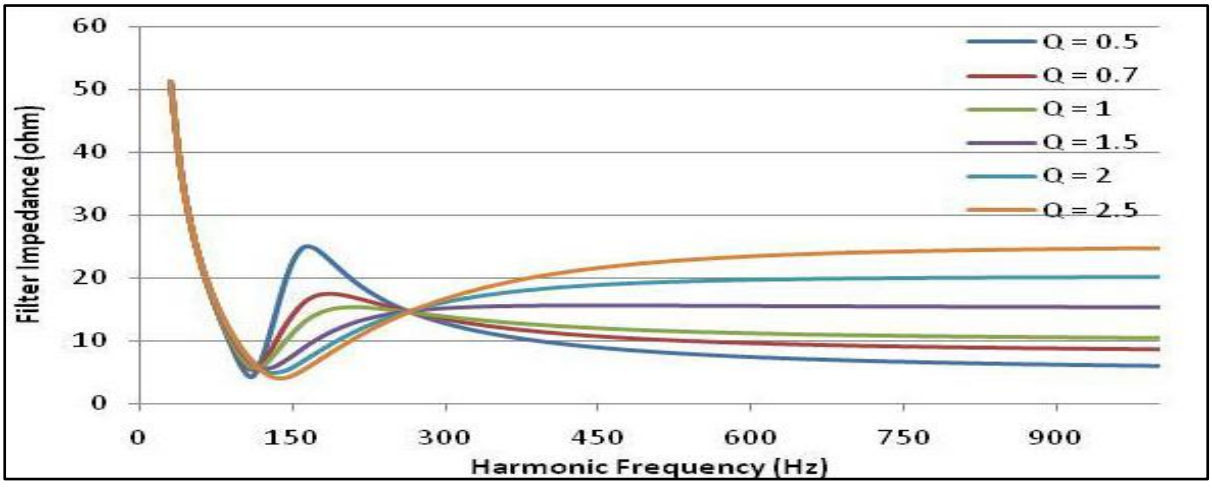


Figure 3.13: 3rd -HP filter-impedance harmonic frequency characteristic with different quality factors. [49]

The C-type high-pass filter circuit is similar to the 2nd order filter with the addition of a capacitor in series in the inductor branch as presented in Figure 3.10-(d). The harmonic-filtering performance of the C-type filter is intermediate between the 2nd and the 3rd order high-pass filters [51]. This topology is usually applied to filter lower-order harmonics compared to the 2nd and the 3rd order filters. At the fundamental frequency, the filter is mainly a capacitor branch as the resistor branch is bypassed by the tuned low-impedance branch of the capacitor and the inductor [49]. However, the filter behaves like the 1st order high-pass filter at high frequencies as the inductor's reactance will be high and the current fill flows through $C1$ and R_D [52]. The C-type filter has the minimum power loss as the fundamental current does not pass through the resistor [50]. The filter-impedance harmonic frequency characteristic with different quality factors is presented in Figure 3.14.

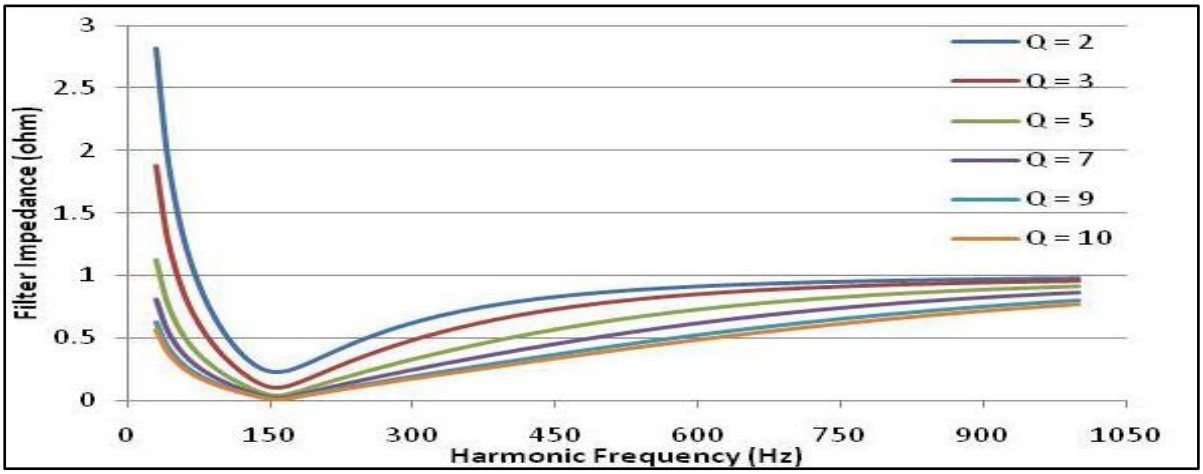


Figure 3. 14: C-type filter-impedance harmonic frequency characteristic with different quality factors. [49]

3.3.3.4 Composite Passive Power Filter

In practice, harmonic mitigation in electrical power systems can be improved by application of composite shunt-filter banks as shown in Figure 3.15. As the double-tuned passive filters are complex in structure and difficult to tune, the composite filter comprises several single-tuned filters and a high-pass filter [53]. In order to maintain the harmonic distortion well below the maximum allowable limits, the single-tuned filters are tuned for low-order harmonics, typically 5th, 7th, 11th and 13th, and a high-pass filter, usually 2nd order, is applied to remove high-order harmonics $> 13^{th}$.

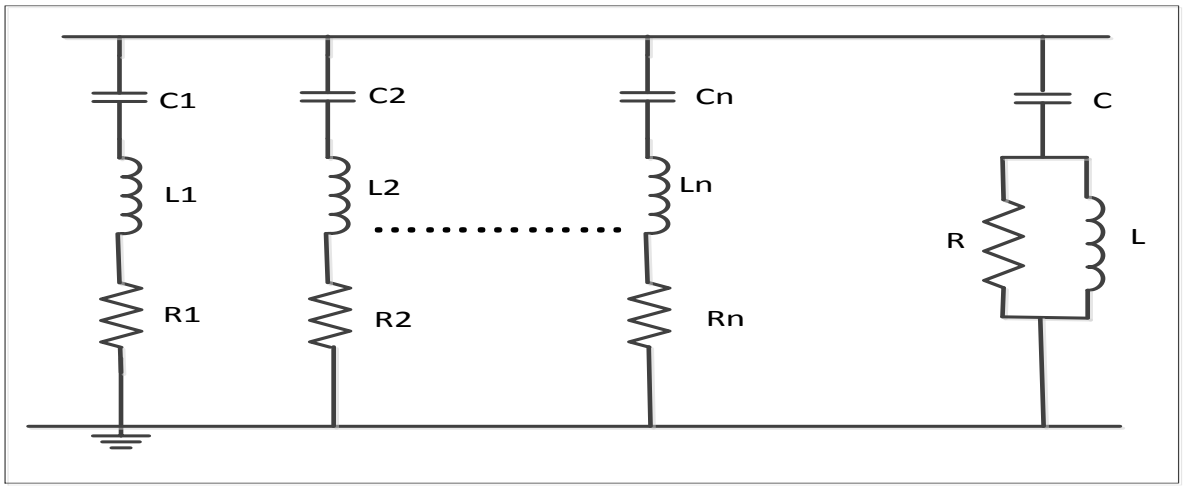


Figure 3.15: Composite passive power filter configurations.

3.4 Active Power Filters (APF)

Active Power Filters (APF) are considered to be the newest technology for power-harmonics mitigation. This technology is based on power-electronics devices, and harmonic filtering is performed by applying the appropriate control for these devices. The rapid advancement in the field of power electronics has drawn more attention to APF for harmonic filtering. The principle function of APF is to measure distortion and inject equal-but-opposite current or voltage distortion into the power system so that the original distortion is cancelled [45]. APF can be applied to cancel up to the 50^{th} harmonic and significantly reduces THD [46]. It is capable of dealing with more than one harmonic at a time. Compared to PPFs, APFs have several advantages such as: 1) superior filtering performance, 2) smaller physical size, 3) flexibility and 4) they do not cause resonance in the system. However, they have the following disadvantages: 1) higher operating losses, 2) higher costs and 3) greater complexity [54].

Active power filters can be classified based on the circuit configuration into: 1) parallel, 2) series and 3) hybrid as presented in Figure 3.16. In hybrid APFs, active and passive power filters are combined together to improve the filter-harmonic performance. [49]

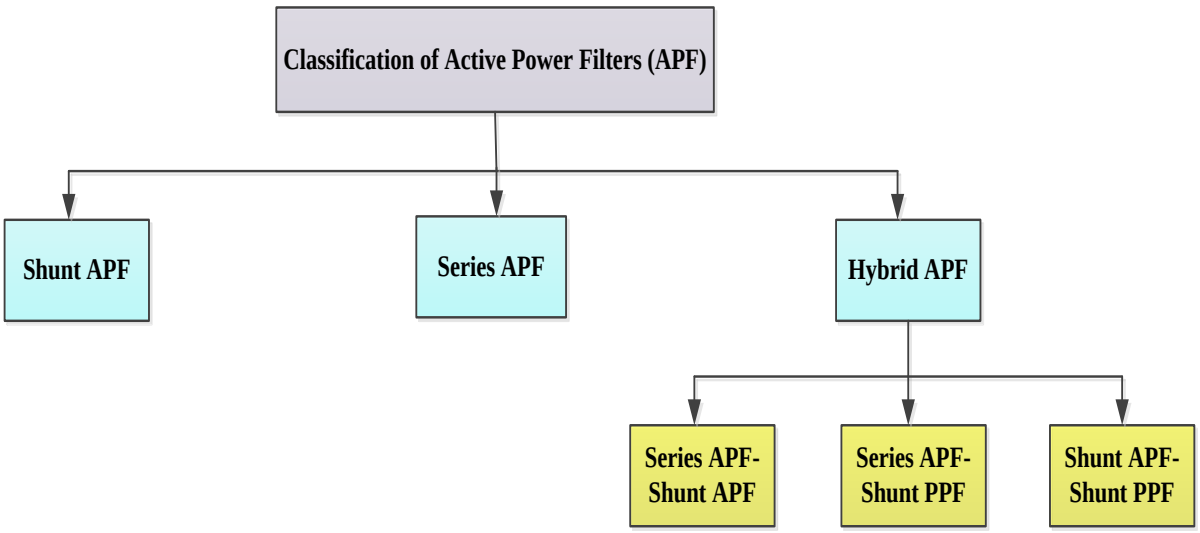


Figure 3.16: General classification of active power filters (APF).

3.4.1 Shunt Active Power Filters

The shunt active power filter is the most popular type of APF, and it is widely applied in industry. It was named shunt as the filter is connected in parallel to the electrical circuit as demonstrated in Figure 3.17. It applies controllable voltage or current source. The main attraction of this topology is that it carries the load harmonic current and not the full load of the circuit current [45].

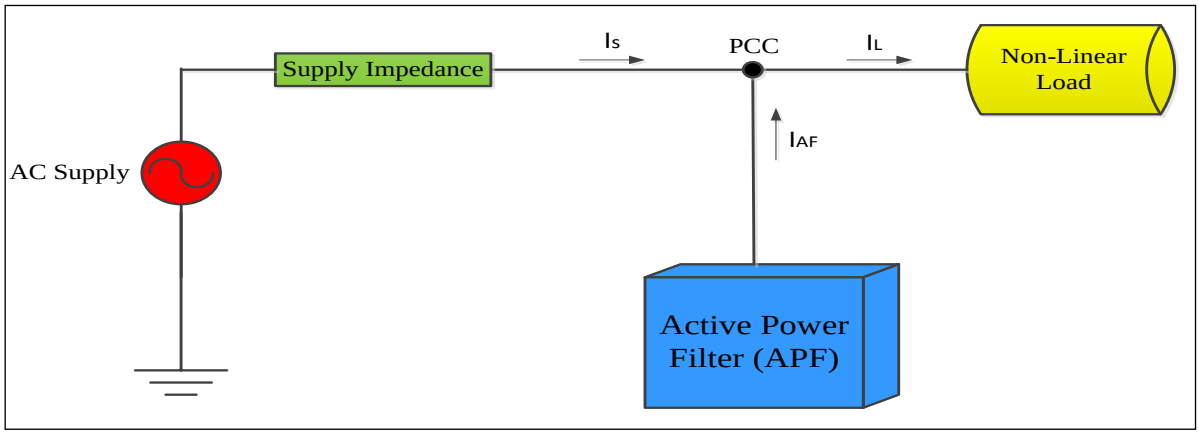


Figure 3.17: Shunt active power filter configuration.

Here, the shunt filter acts like a current source and injects the same harmonic current as generated by the load, but with a 180^{o}-phase shift so it is cancelled out with the harmonic current [55]. The instantaneous load current is detected by the controller, which applies digital signal processing (DSP) to extract the harmonic-current component from the total-load

current [54]. In this way, the harmonic-distortion current is mitigated from the system. In practice, shunt active power filters are applied with two levels (PWM-VSIs). Nowadays, multilevel inverters are becoming mature technology and are attractive for medium-voltage–high-power applications. Because of this, cascaded H-bridge multilevel inverters are considered to be an alternative for the conventional two levels (PWM-VSIs) for shunt APFs. [49]

3.4.2 Series Active Power Filters

Series APFs are connected to the electrical power system via an isolation transformer. The circuit configuration is presented in Figure 3.18. Here, the main idea is to isolate harmonics between the supply and the non-linear load. A series APF generates a PWM voltage waveform. This waveform is added or subtracted instantaneously to deliver a pure sinusoidal voltage waveform to the load. [56] First, the controller identifies the instantaneous supply current. Then, DSP is applied to extract harmonic current from the supply current. Finally, a compensation voltage is supplied across the primary windings of the isolation transformer using the series APF, which reduces harmonic distortion. [45]

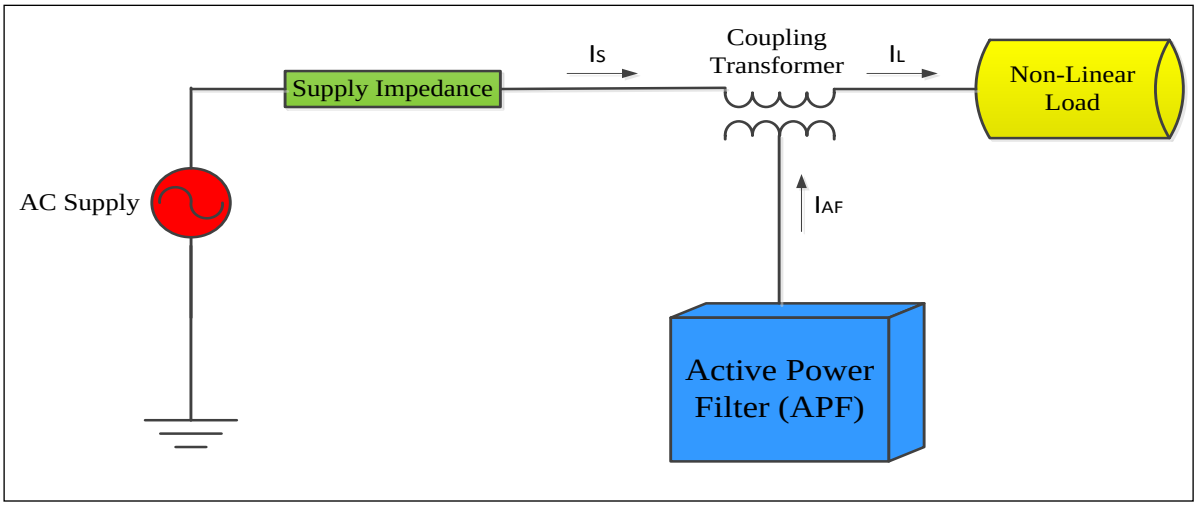


Figure 3.18: Series active power filter configuration.

The main drawback of this configuration is that it must carry the full-load current, which results in higher device ratings, higher losses and larger filters [56]. Because of this, series APFs are not commonly used in industry compared to shunt APFs. However, series APFs are superior to shunt APFs as they mitigate voltage harmonic distortions and can be used to balance three-phase voltage.

3.4.3 Hybrid Active Power Filters

At present, there is considerable interest in hybrid active power filters for different power-quality applications. The main reason for this interest in hybrid APFs is the performance improvement in harmonic mitigation and other power-quality problems. Essentially, hybrid APFs comprise passive and active power filters in different configurations. Hybrid APFs are classified, based on the literature review, into four basic categories: 1) series APF with shunt APF connected in series, 2) series APF and shunt PPF and 3) shunt APF with shunt PPF. In summary, the key advantages that can be achieved by implementing hybrid APFs are: 1) maximizing filter performance, 2) eliminating drawbacks of conventional topologies and 3) minimizing overall filter costs.

3.4.3.1 Series APF with Shunt APF Connected in Series

To come up with an APF topology with the merits of shunt APF and series APF, these two APFs are constructed to operate together in harmonic mitigation. The circuit layout of such a configuration is presented in Figure 3.19. This combination can achieve better harmonic elimination, but a special control algorithm is required to control the combined shunt and series APFs [49]. Due to control complexity and high costs, this hybrid filter topology is not commonly used compared to other topologies [56].

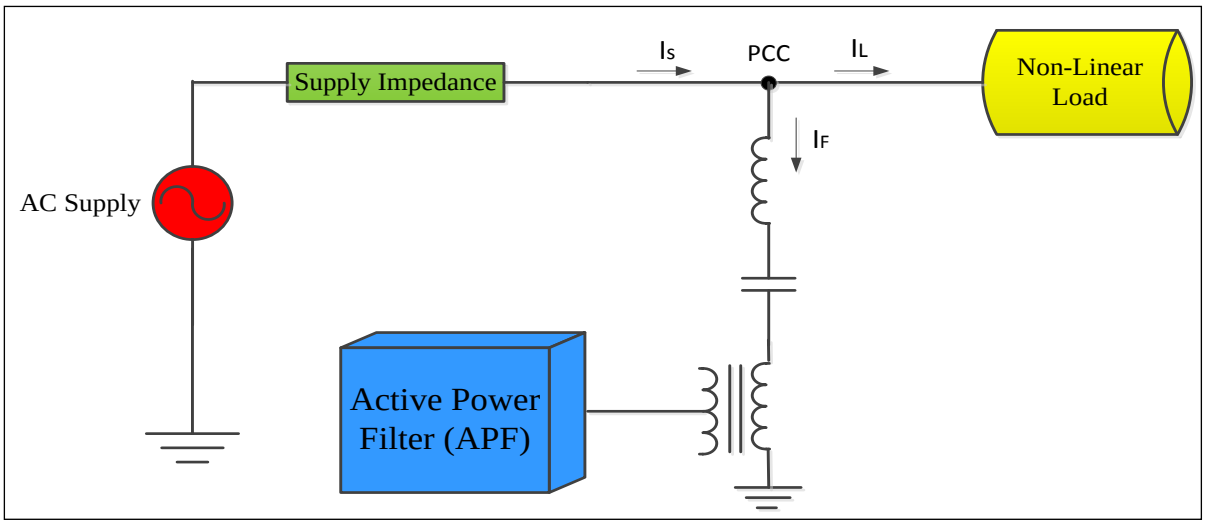


Figure 3.19: Series APF with shunt APF configuration.

3.4.3.2 Series APF with Shunt PPF

This hybrid APF combines a series APF and shunt PPF as displayed in Figure 3.20. In this configuration, the series APF efficiently isolates harmonic current between the supply and the non-linear load and improves the performance of the shunt passive filter by inserting high resistance in the source impedance branch for harmonic current [57]. The shunt passive filter is usually a shunt passive filter bank consisting of a group of single-tuned filters to eliminate low-order dominant harmonics – typically, the 5^{th} and 7^{th} in parallel with a 2^{nd} order high-pass filter. There is little interest in such a configuration as series APFs are less preferred in industry [56].

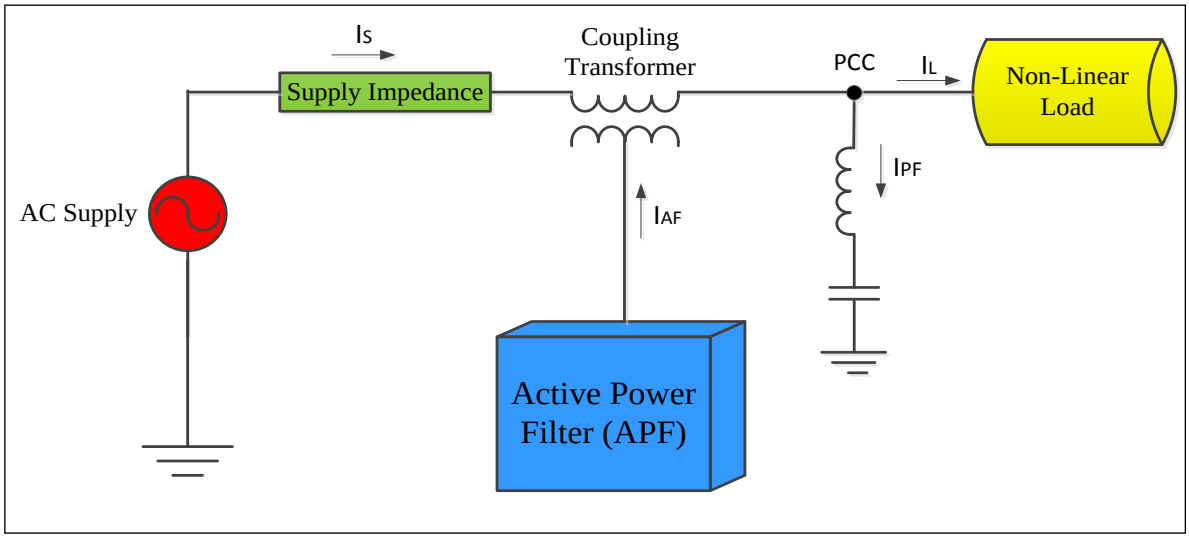


Figure 3.20: Series APF with shunt PPF configuration.

3.4.3.3 Shunt APF with Shunt PPF

Figure 3.21 demonstrates the circuit configuration of this filter. In this type of hybrid filter, the shunt APF and shunt PPF are connected in parallel to the PCC with non-linear load. The shunt PPF's main function in this configuration is to eliminate the low-order dominant harmonics of the load current and provide reactive power compensation [58] . The shunt APF is designed to eliminate part of the low-frequency harmonics. This design significantly reduces the series APF cost, and hence, the total filter cost [54]. In addition, low THD values can be achieved by applying this filter. The main disadvantage of this combination is that it requires a large number of power components [56].

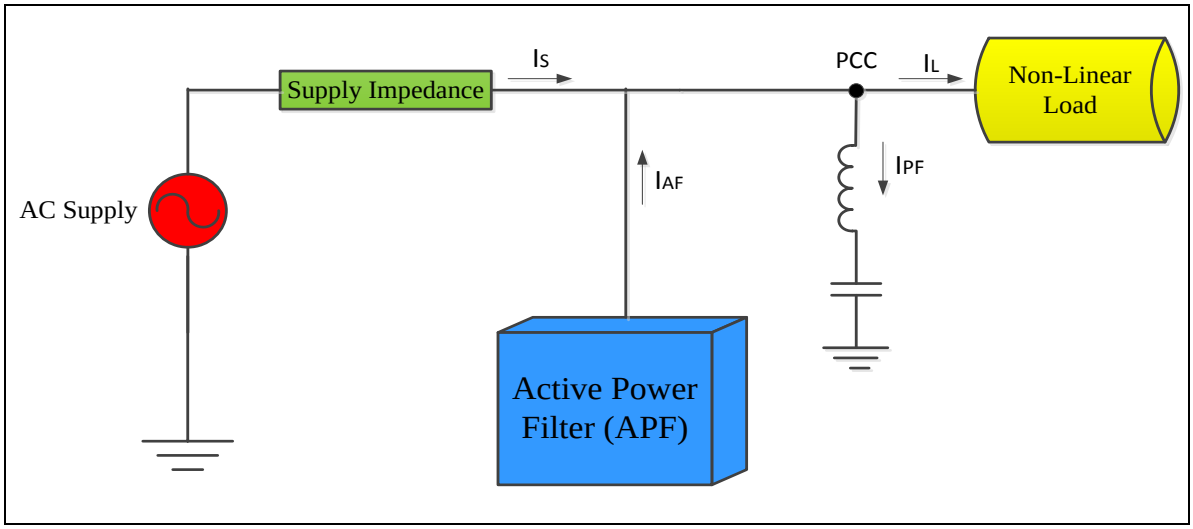


Figure 3.21: Shunt APF with shunt PPF configuration.

3.5 Technical Comparison of PPF and APF

Passive power filters (PPF) are widespread in both industrial and power-utility applications, mainly because they have a simple structure and are considered to be a cost-effective solution for harmonics. However, APFs have more features, which make them more suitable in certain applications. In operation, hybrid filters merge the benefits of passive and active filters, and having the features of both topologies makes them efficient. The system engineer is responsible for determining the most suitable filtering topology. Tables 3-3 and 3-4 each provide a selection matrix that serves as guidelines to help select the most suitable filter topology according to application requirement. [40, 45, 46, 48, 49, 51, 52, 54, 56-60]

Table 3-3: Passive Power Filter Selection Matrix

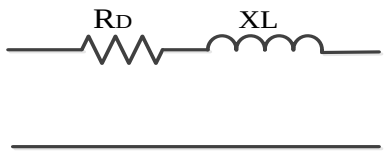
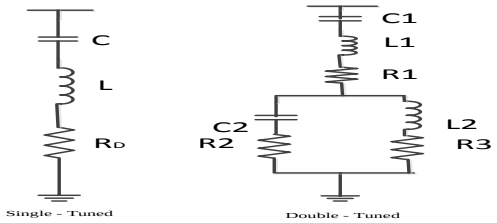
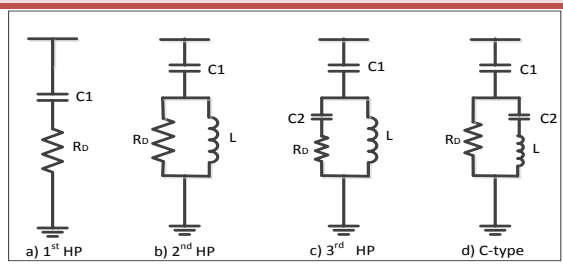
Topology	Passive Power Filters		
	Series	Shunt-tuned	High-pass
Components	R, L	R, L, C	R, L, C
Circuit Layout			
Key Features	➢ Series reactor connected in series with the line. ➢ Mainly applied for current smoothing. ➢ Typically available in percentage impedance (1–1.5%, 3% and 5%). ➢ Moderate reduction in both voltage and current harmonics.	➢ Most commonly used filters in industry. ➢ Tuned to eliminate particular harmonics. ➢ Available in single-tuned or double-tuned. ➢ Connected in shunt with the system. ➢ At tuned frequency, provide a low-impedance path for tuned-harmonics current. ➢ When designed, care should be taken to avoid capacitive overcompensation at light load. ➢ Two single-tuned filters in parallel have the same characteristic as double-tuned.	➢ Tuned at a cut-off frequency, and all harmonics above cut-off frequency are filtered out. ➢ Shunt-connected. ➢ Usually applied to filter higher-order harmonics. ➢ Used in complement with tuned filters. ➢ Typically: 1st, 2nd, 3rd order and C-type. ➢ 1st order: high losses and not commonly used. ➢ 2nd order: most commonly used in industry. ➢ 3rd order: complicated – high number of components.
Merits	➢ Low cost. ➢ Minimum number of components. ➢ Better input protection for non-linear load and components from system transients.	➢ Simple and reliable. ➢ Cost-effective. ➢ Handles only the harmonic component of load current.	➢ Eliminates a wide range of harmonics spectrum using only one filter. ➢ Not sensitive to parameter deviations (shallower notch valley).
Demerits	➢ Not enough harmonic reduction to power-quality requirements. ➢ Handles full-load current, hence: ➢ High power loss and high component ratings are required.	➢ Possible resonance with system impedance. ➢ Eliminates one/two harmonics per filter and hence multiple shunt filters are required. ➢ Possibility of detuning. ➢ Possible resonance with system impedance.	➢ Large ratings at fundamental, hence: ➢ Higher power losses. ➢ Requires high number of components.

Table 3-4: Active Power Filter Selection Matrix

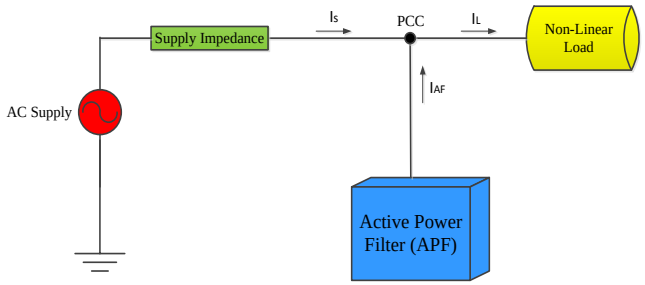
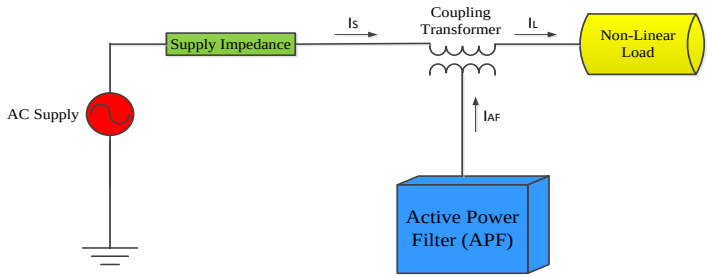
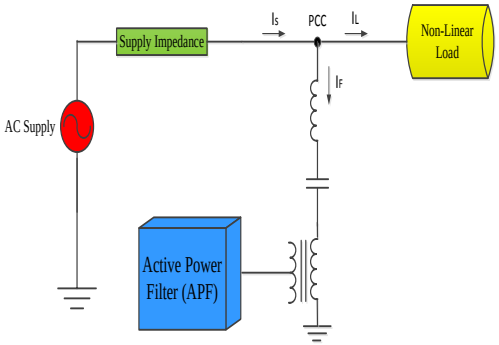
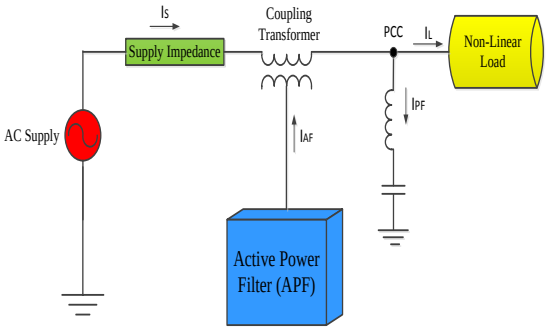
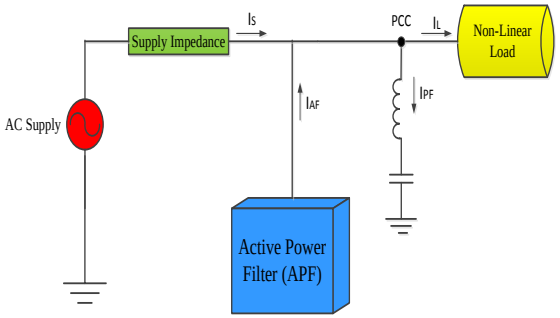
Topology	Active Power Filter (APF)	
	Shunt	Series
Components	Semiconductor Devices	Semiconductor Devices
Circuit Layout		
Key Features	➢ Most popular type of APF applied in industrial applications. ➢ Connected in shunt at PCC. ➢ Current harmonics compensation. ➢ Detects instantaneous load current, supresses harmonics components by applying DSP and injects equivalent current to the system, but 180^{o}-phase shifted to cancel harmonics. ➢ In practice, it is applied on two levels (PWM-VSIs). ➢ Multilevel VSIs are considered an alternative of conventional (PWM-VSIs).	➢ Not commonly used compared to shunt APFs. ➢ Series-connected via isolation transformer. ➢ Voltage harmonics compensation. ➢ Main purpose to isolate harmonics between supply and non-linear load. ➢ Detects instantaneous supply current, supresses harmonics components by applying DSP and injects equivalent current to the system, but 180^{o}-phase shifted to cancel harmonics. ➢ Applied as voltage regulators and harmonic isolators. ➢ Attractive for unbalanced voltage compensation, voltage sags, swells and low-power applications.
Merits	➢ Filter handles and carries harmonic-current component only. ➢ Superior harmonic mitigation, can cancel up to 50th harmonic. ➢ Multifunction: harmonics reduction, power-factor correction and VAR compensation. ➢ Effectively protects supply from load harmonics.	➢ Filter handles and carries full-load current component. ➢ Higher device ratings, higher losses and large filter size. ➢ Effectively protects the load from supply harmonics.
Demerits	➢ High cost compared to passive filters. ➢ High switching frequency.	➢ Filter handles and carries full-load current component. ➢ Higher device ratings, higher losses and large filter size. ➢ Higher cost and complex control compared to shunt APFs. ➢ Isolation transformer failure leads to power disruption.

Table 3-4 (continued): Active Power Filter Selection Matrix

Topology	Hybrid Active Power filters (Hybrid APFs)		
	Series APF + Shunt APF connected in series	Series APF + Shunt PPF	Shunt APF + Shunt PPF
Components	R, L, C + Semiconductor Devices	R, L, C + Semiconductor Devices	R, L, C + Semiconductor Devices
Circuit Layout			
Key Features	➢ Combination of series and shunt APFs. ➢ Combines merits of both topologies. ➢ Not commonly used topology due to complex control and high cost. ➢ Eliminates both voltage and current harmonics.	➢ Combination of series APF and shunt PPF. ➢ Series APF provides isolation of harmonic current between supply and load, and improves performance of the shunt APF. ➢ Shunt passive filters are usually of composite type (single-tuned 5^{th} and 7^{th} + 2^{nd} order high-pass filter). ➢ Little interest as series APF not preferred in industry.	➢ Combination of shunt APF and shunt PPF. ➢ Most popular and preferred in industry. ➢ Both filters connected in parallel into PCC. ➢ Shunt PPF eliminates low-order dominant harmonics and provides reactive power compensation.
Merits	➢ Better harmonic reduction performance can be achieved.	➢ Lower switching losses. ➢ Simple control because of shunt PPF presence.	➢ Better harmonic reduction performance. ➢ Significant reduction in filter cost. ➢ Handles harmonic components of current only. ➢ Simple control because of shunt PPF presence.
Demerits	➢ Special control algorithm is required. ➢ Complex control. ➢ High cost.	➢ Presence of series APF results in drawbacks for this topology.	➢ Requires high number of components. ➢ Higher power losses. ➢ Requires high number of components.

3.6 Summary

This chapter presented a critical review of power-system harmonics and harmonic-power filters. In the first part of the chapter, a brief historical and theoretical background of the harmonic phenomenon was introduced. Then, a classification of sources of power harmonics was introduced and the main classification categories were discussed. Next, the adverse effects of power harmonics were illustrated as per the main components of the power system. The first part of the chapter ended by presenting a detailed classification for existing solutions, mitigation techniques and international standards applied for harmonics.

The second part of this chapter introduced a general classification for power-harmonics filters. PPF topologies were explained in terms of circuit layout, operating principles, features and main applications. Similarly, APF topologies were discussed. The chapter concluded with an important comparison of PPF and APF topologies, addressing circuit layout, key features, advantages and disadvantages.

Based on this review, the composite PPF was proposed for optimum multilevel inverter design as it features a cost-effective harmonic-elimination solution, a simple structure, reliability and easy implementation. Furthermore, the composite passive filter has excellent harmonic-mitigation performance compared to other filters and does not require any complex control. In addition, the shunt-tuned and high-pass PPF do not carry full-load current, which considerably reduces power loss and component weight and size. More details on the trade-off optimisation model and optimum passive filter design will be discussed in Chapter Four.

CHAPTER 4: PROPOSED OPTIMUM TRADE-OFF MODEL

4.1 Introduction

For a given grid voltage, it is possible to design a CHB-MLI with either a low number of series-cascaded H-bridge cells featuring devices with high blocking voltage, or with a high number of cascaded cells featuring switching devices with low blocking voltage. The required size of the output filter is also affected by the number of inverter levels. While an inverter with few levels requires a larger filter, an inverter with many levels requires a smaller filter, or even eliminates the need for a filter. This trade-off in inverter levels and output-filter size is affected by several factors. This chapter proposes a generic genetic algorithm (GA)-based optimisation model to solve this trade-off problem and to determine the optimum design for the required application.

The chapter starts by defining the trade-off problem, the main factors affecting the problem and the main steps implemented for optimisation. Then, an overview of GA is presented, followed which, a generic GA-based model is proposed to solve the SHE problem in multilevel inverters. Next, the problem of power-loss evaluation in multilevel inverters is reviewed. A precise generic model for calculating conduction and switching losses in multilevel inverters is proposed and discussed in detail. The chapter concludes with an optimum GA model for passive power filter (PPF) implementation at the multilevel inverter output to optimize the trade-off.

4.2 Trade-off between Number of Cascaded H-Bridges and Size of Output Filter in CHB-MLIs

For medium-voltage grid-connected applications (typically 6–36 kV), renewable energy sources such as solar (PV) power plants are usually integrated into the power grid via a step-up transformer, which is bulky, heavy and space-consuming. This results in a significant increase in overall system cost, weight and size, as well as requiring more complex installation and maintenance. To overcome these drawbacks, multilevel voltage-source inverters might be a feasible solution. These multilevel inverters are capable of building a higher output voltage with low-voltage switching devices. The application of multilevel inverters for direct grid connection of PV power plants has attracted many researchers and

continues to gain attention. Among the three classical multilevel inverter topologies, the cascaded H-bridge is superior and has many attractive features. The modularity of this topology allows easy packaging, simple implementation and a higher number of levels with the lowest number of devices. The CHB-MLI is a well-established technology and commercially available up to 13.8 kV.

For the integration of renewable energy sources at a given power-grid voltage, there is always a trade-off between the number of inverter levels to be implemented and the size of the output filter. There are several factors affecting this trade-off. Integration can be achieved by using an inverter with a low number of levels (few cascaded cells) featuring switching devices with high blocking voltage, or an inverter with a high number of levels (many cascaded cells) featuring switching devices with lower blocking voltage. The inverter designed with a low number of levels will require higher switching frequency, a larger output filter, switching devices with higher blocking voltage, and it will experience worse switching losses. However, the inverter with a low number of levels implements the lowest number of devices and has better conduction-loss performance. Conversely, the inverter with many levels requires a lower switching frequency, a smaller output filter (or it eliminates the need for a filter), switching devices with lower blocking voltage, and it has better switching-loss performance. However, the inverter with many levels needs more devices and has higher conduction losses. The trade-off between the number of levels for multilevel inverters is summarized in Table 4-1 [61].

Table 4-1: Effect of Inverter's Number of Levels on the Trade-Off

Inverter with Low Number of Levels	Inverter with High Number of Levels
Few cascaded cells.	Many cascaded cells.
Devices with high blocking voltage.	Devices with low blocking voltage.
Higher switching frequency f_s.	Lower switching frequency f_s.
Less conduction loss.	More conduction loss.
Worse switching losses.	Better switching losses.
Higher %THD and needs large filter.	Lower %THD and needs small filter.
Few components required.	Many components required.

This chapter proposes a model to quantify and optimize the trade-off in the number of inverter levels and the size of the output filter based on GA. The model is applied to optimize the CHB-MLI for a given grid-voltage level and output-rated power. Table 4-2 summarizes the main steps that the optimisation model approach was based on. It is crucial to have a quantifying methodology that helps to determine the number of inverter levels and size of output filter for the required design. Figure 4.1demonstrates the general model architecture for the applied trade-off optimisation approach.

Table 4-2: Main Steps for Optimisation Approach

1	• A GA-based generic optimisation is proposed to address the SHE problem for controlling the inverter and minimizing THD.
2	• A precise model is proposed for conduction and switching loss calculations in multilevel inverters.
3	• A GA-based optimisation model is proposed for the output passive power filter design.
4	• Multi-objective function and constraints are defined.
5	• Optimum solution is obtained based on the considered design key measures values.

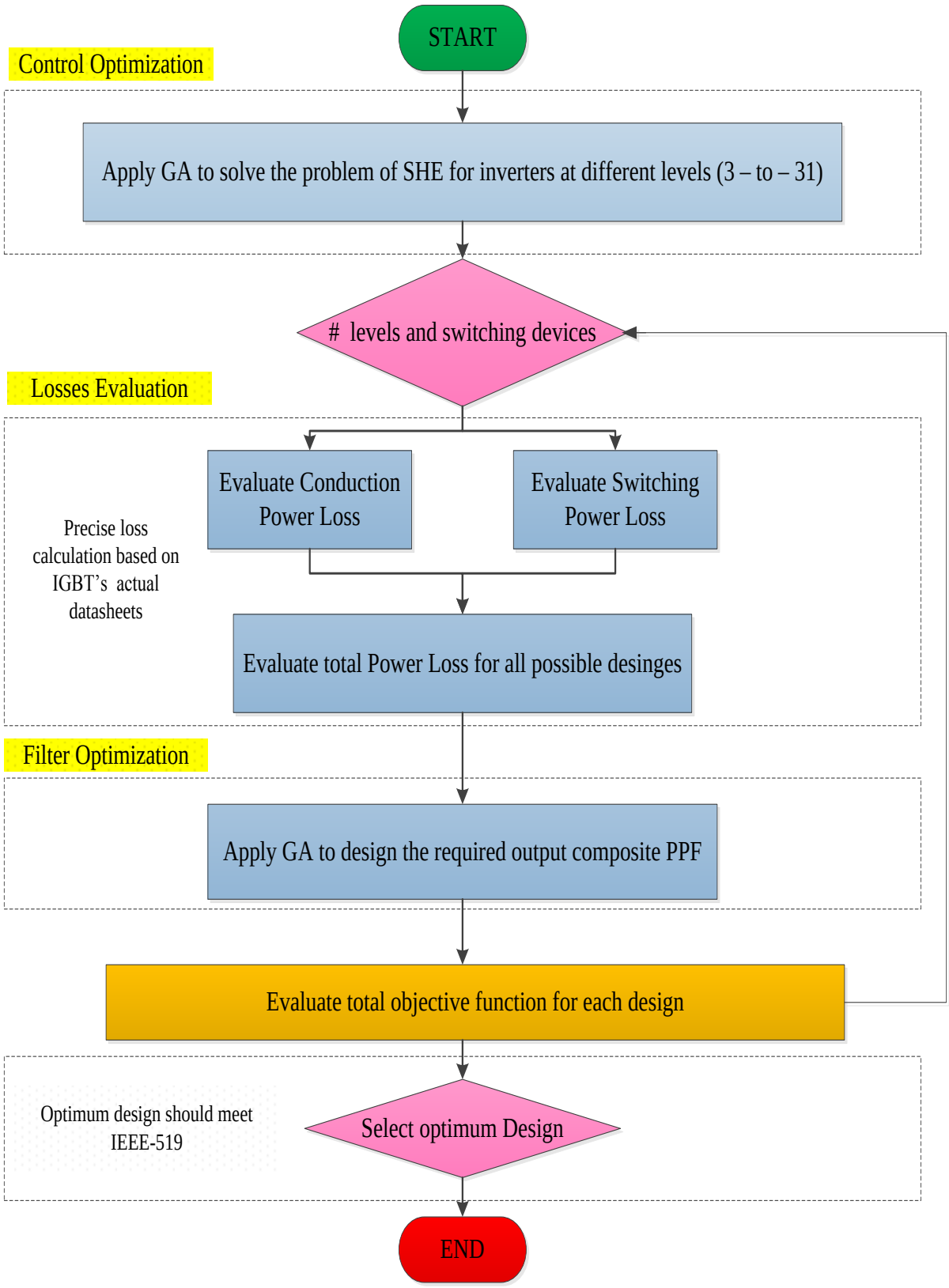


Figure 4.1: General model architecture for the applied trade-off optimization approach

4.3 Genetic Algorithm (GA)

4.3.1 Overview

The idea of applying evolution as an optimisation tool for engineering applications was considered by computer scientists in the 1950s and 1960s [62]. The basic concept is to generate a population of candidate solutions for the considered problem and apply operators according to natural genetic variation and natural selection.

A genetic algorithm (GA) is a heuristic global evolutionary optimisation algorithm that is based on the mechanics of natural selection and genetics. This algorithm was initially described by John Holland in the 1960s and was further developed by Holland and his colleagues and students in the 1960s and 1970s [63]. GA applies biological evolution in the process of optimisation. The key difference compared to other optimisation techniques is that GA searches by population rather than by an individual point search. GA has been successfully and widely applied to solve both constrained and unconstrained optimisation problems. In practice, most of the engineering problems are combinatorial problems that include minimisation or maximization of different objectives, with some applied constraints. Compared to conventional optimisation, heuristic techniques are more powerful, efficient and capable of finding the global optimum solution to such combinatorial problems. Table 4-3 summarizes the key attractions of GA over other artificial intelligence techniques [59, 64].

Table 4-3: Genetic Algorithm (GA) Key Attractions

Key Attractions of GA Optimisation
➢ GA deals with the coded form of the problem's parameters and not the parameters themselves.
➢ Rather than searching by a single point, GA starts searching in a group of points.
➢ GA optimizes the objective function itself and not its derivatives or other auxiliary information.
➢ The algorithm implements probabilistic and not deterministic rules in its choice.
➢ It is a robust algorithm.
➢ GA can handle a wide range of optimisation problems.

The process of any GA optimisation consists of four main steps: 1) initialization of the population, 2) evaluation of fitness function, 3) selection and 4) applying genetic operators. Figure 4.2 shows a general flow chart for GA optimisation. The algorithm starts by generating a random population of candidate solutions for the considered optimisation problem. Then, it moves from one generation to another by applying natural selection, with genetic operators for crossover and mutation. The algorithm stops when the applied stopping criterion is achieved. In the following subsections, a discussion of each step of GA optimisation is presented and discussed.

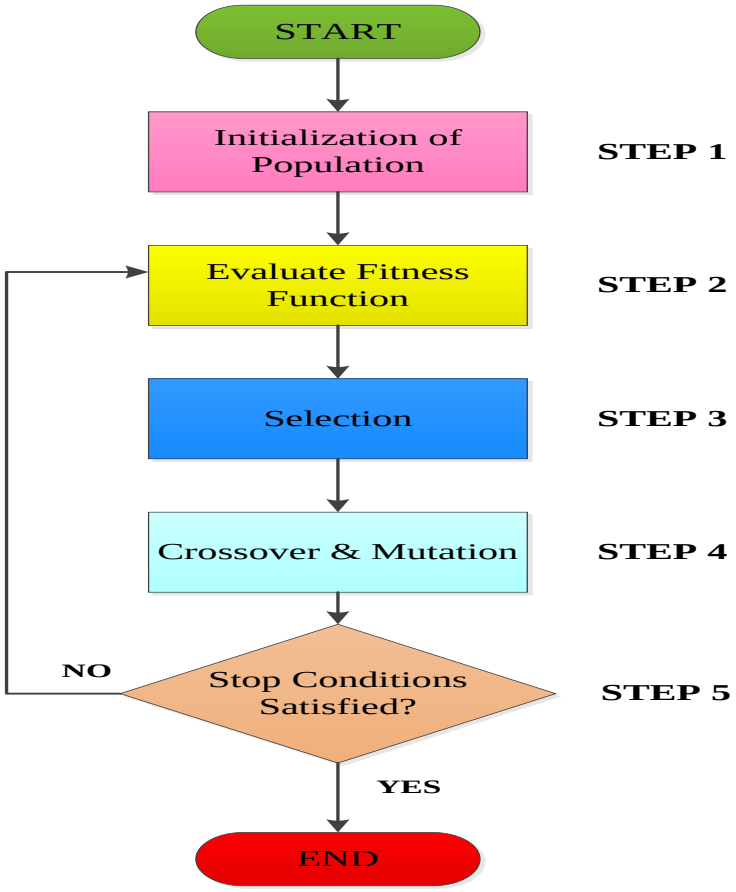


Figure 4.2: General flow chart for genetic algorithm (GA) optimisation.

4.3.2 Initialization of the Problem

A set of "genes" make up a "chromosome" in natural genetics. In GA, the optimisation parameters are considered to be "genes", and a "chromosome" represented by a "string" is made up from the problem "genes" [65]. At the start, the algorithm should be initialized. Each parameter "gene" of the optimisation problem is coded in a binary or floating-point "string". Then, a set of solutions is randomly generated, based on the coded parameters for

the specified size of population. This generated set of solutions is called the "initial population", P_i. Each individual feasible solution is considered a "chromosome". The number of generated solution "chromosomes" indicates the "population size", which should be defined in the design of the algorithm. The "population size" affects the performance of GA. It should not be either very small or very large as GA might perform poorly in such a scenario [66].

4.3.3 Evaluation of Fitness Function

An objective function must be defined as a measure to guide the algorithm through the optimisation process. This helps to evaluate the goodness of each generated solution string. The objective function plays a crucial role in the performance of GA optimisation and significantly affects the quality of the solution. Hence, it should be determined very carefully. In some optimisation problems, there are multi-objectives to be optimized. Practically, the range of values for the objective function varies from one optimisation problem to another. Accordingly, each individual string is evaluated and assessed by a measure, the so-called "fitness function", which normalizes the values of the objective function to a convenient range between (0 and 1) [67].

4.3.4 Selection

Based on the objective function, a "fitness function" (sometimes called "fitness score" or "fitness value") for each individual solution is determined, which indicates the goodness of the solution for the optimisation problem [64]. At selection stage, only those individuals with high fitness values are likely to survive, and those with low fitness function are eliminated when they "die". Parents for the next generation are selected according to selection rules (for example, roulette-wheel or tournament selection) to produce off-spring chromosomes. The selected parents are the main contributors to form the next generation. This means that strings with high fitness-function values in the old generation are most likely to contribute one or more off-spring in the next generation [65]. Figure 4.3 illustrates roulette-wheel selection for five individuals. The fittest individual has the largest share of the roulette wheel.

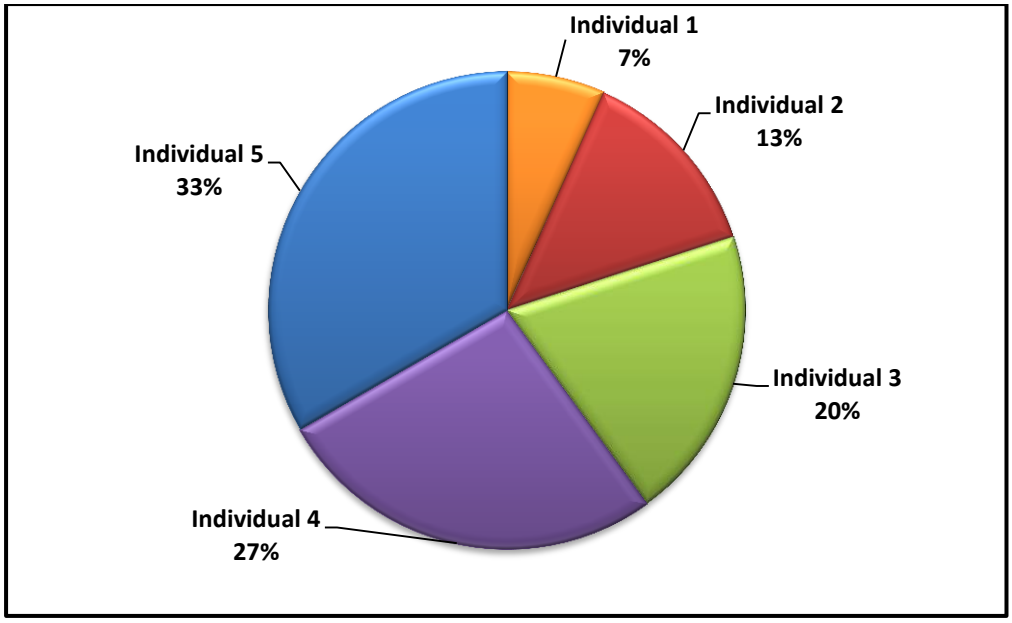


Figure 4.3: Sample roulette wheel and assigned areas for population individuals.

4.3.5 Crossover and Mutation

Crossover is a genetic operator that is applied, in which a number of bits are swapped between parents. The purpose is to differentiate the population so that new individuals are created in the next generation [59]. Essentially, in crossover, the two individuals that become the parents are selected randomly. Then, some genes are exchanged at the selected crossover point to form a new, improved combination and create two new individuals for the next generation. Crossover is considered an important and powerful genetic operator. Figure 4.4 illustrates an example of a one-point crossover.

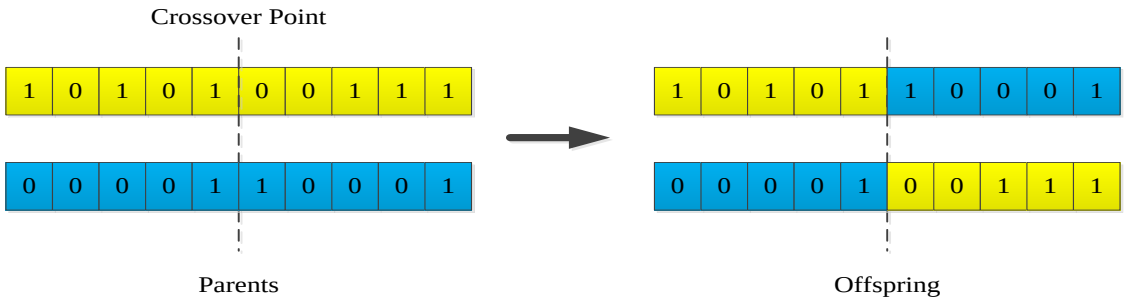


Figure 4.4: Example of an individual crossover.

After the crossover is performed, another operator is applied at low probability, which is called mutation. In this operator, genes are alerted and mutated. Mutation of individuals can be accomplished by changing a bit within a gene from 0 to 1, or from 1 to 0. Mutation expands the search space and prevents the algorithms from converging on local minima. Figure 4.5 shows a mutation example of a bit-by-bit flipping at a random position. Mutation is the last genetic operator to be applied and after that, off-spring generation is obtained, which is further improved from the previous parent generation.

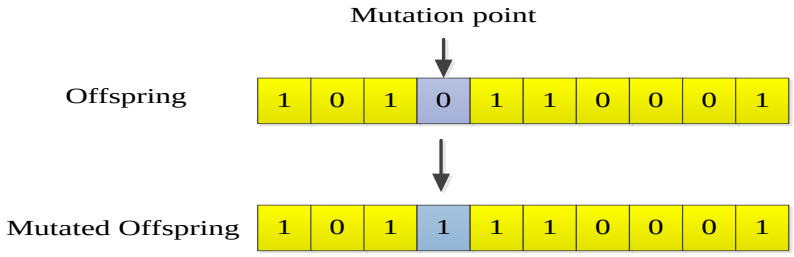


Figure 4.5: Example of bit-flip single mutation.

4.3.6 Stopping Criterion

When designing a GA-based optimisation, it is important to use a stopping criterion, whose purpose is to tell the algorithm when to terminate. To achieve this, the algorithm decides the optimum solution as an output of the optimisation problem. Typically, the algorithm is designed to stop after 100 generations are performed. In some cases, the algorithm might converge on a solution before 100 generations. In such cases, the GA should stop when the weighted average change in the objective function over 50 generations is less than a given tolerance function, for example ($\varepsilon = 1 \times 10^{-6}$).

4.3.7 Test of Applied GA

For evaluation of the GA performance based on the applied settings, Rastrigin's function of two independent variables is used which is mathematically represented by Equation 4.1.

$$Ras\,(x) = 20 + x_1^2 + x_2^2 - 10\,(\cos 2\pi x_1 + \cos 2\pi x_2) \qquad 4.1$$

Where the searching domain of the function is:

$$-5.12 \leq x_i \leq +5.12 \qquad 4.2$$

The 3D representation of this function is plotted in Figure 4.6. The Rastrigin's function has many local minima as shown in the plot, but has just one global minimum in which its value (0) and occurs at the point ($x_1 = x_2 = 0$) in the x-y plane. The applied GA was successful in finding the global optimum solution for the Rastrigin's function as shown in the GA performance in Figure 4.7

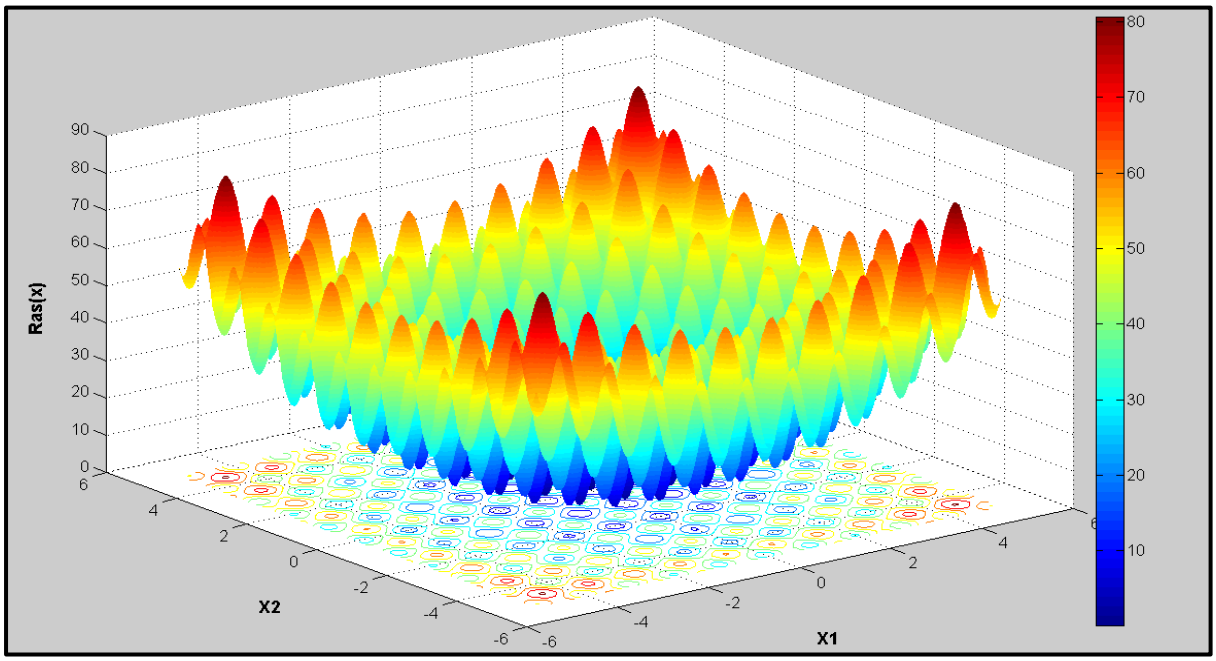


Figure 4.6: Rastrigin's function – 3D representation

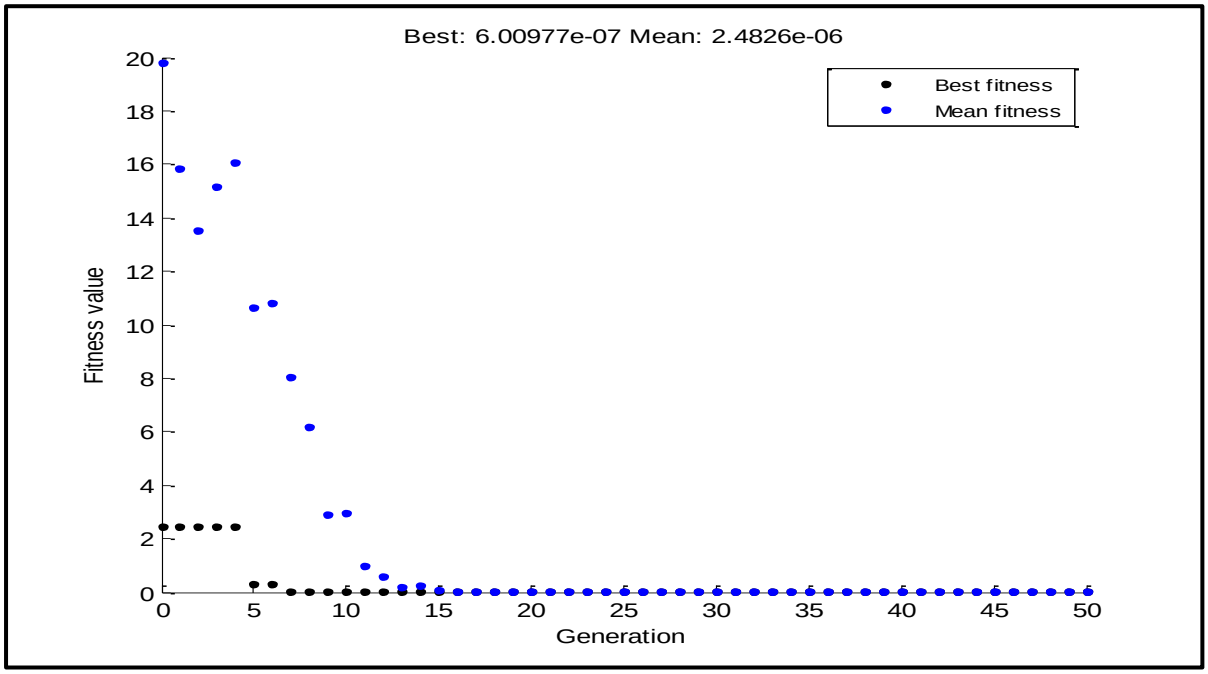


Figure 4.7: GA performance for Rastrigin's function optimisation

4.4 Genetic Algorithm for SHE control of CHB-MLI

This section discusses the implementation of GA for solving the switching angles of the selective harmonic elimination control problem. First, the mathematical model of SHE control for CHB-MLI is explained. Then, a critical review of the existing applied solutions for the SHE problem is discussed and compared. The main features, advantages and disadvantages for each solution's approach are presented. At the end of this section, there is a proposal for a GA-based generic optimisation to solve the SHE-control problem with any number of inverter levels.

4.4.1 Mathematical Model for the Problem of SHE in CHB-MLI

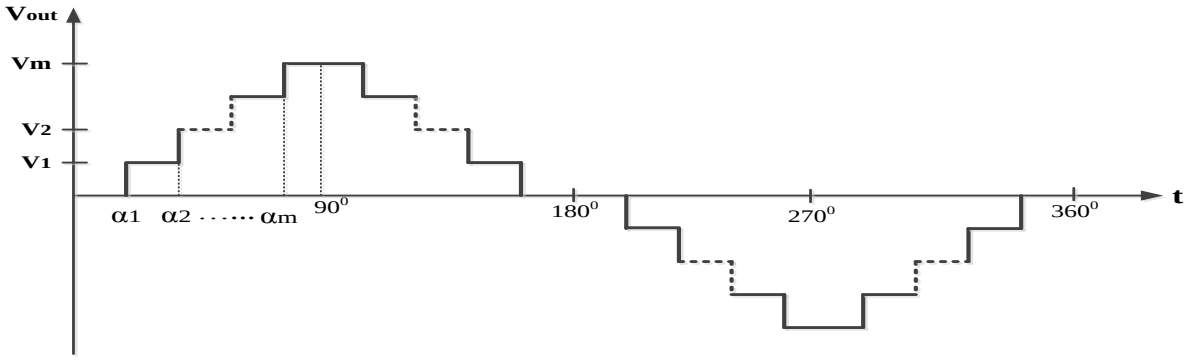


Figure 4.8 Generalized output stepped-voltage waveform for n-level inverter.

A generalized stepped-voltage waveform of n-level generated by CHB-MLI is illustrated in Figure 4.8. Applying Fourier's expansion, the stepped-voltage waveform can be expressed in terms of odd harmonics only as a result of quarter-wave symmetry as explained in Chapter Two (Section 2.5.2). Assuming a balanced three-phase system, all triplen harmonics will be zero [11]. The general equation of the output voltage given by Fourier's expansion can be written as:

$$v_{an}(\omega t) = \sum_{k=1,3,5,\ldots..}^{\infty} \frac{4V_{dc}}{k\pi}[cos(k \propto_1) + cos(k \propto_2) \ldots\ldots + cos(k \propto_s)]\, sin(k\omega t) \qquad 4.3$$

Where S is the number of switching angles to be calculated. In the case of CHB-MLI topology, S is equal to the number of series-connected H-bridge cells of the inverter. The magnitude of the fundamental component and the non-triplen odd harmonics expressed by Equation 4.4 and all switching angles are in ascending order and less than 90°.

$$\begin{aligned} V_1 &= cos(\theta_1) + cos(\theta_2) + \cdots\cdots\cdots + cos(\theta_S) = S \times M_i \\ V_5 &= cos(5\theta_1) + cos(5\theta_2) + \cdots\cdots\cdots + cos(5\theta_S) = 0 \\ V_7 &= cos(7\theta_1) + cos(7\theta_2) + \cdots\cdots\cdots + cos(7\theta_S) = 0 \\ &\vdots \quad \vdots \quad \vdots \\ V_h &= cos(h\theta_1) + cos(h\theta_2) + \cdots\cdots\cdots + cos(h\theta_S) = 0 \end{aligned} \tag{4.4}$$

$$\theta_1 < \theta_2 < \cdots\cdots\cdots < \theta_S < 90^{\circ} \tag{4.5}$$

Where: M_i is the modulation index.

$h = 3S - k$, is the highest harmonic order that can be eliminated. K takes the value of 1 for an even number of S, and takes the value of 2 for an odd number of S. [31]

Equations 4.4 and 4.5 form the mathematical model to solve the problem of selective harmonic elimination. In the next subsection, a critical literature review discusses the methods most applied to solve the SHE problem.

4.4.2 Critical Review of Applied Solution Techniques for the SHE Problem

The SHE system given in Equations 4.4 and 4.5, is a highly nonlinear system. In the literature, this equation system for calculating switching angles is called the "system of transcendental equations" or "SHE equations". For cascaded H-bridge multilevel inverters (CHB-MLI), the number of equations is equal to the number of H-bridge cells of the inverter. A survey of the literature on solving the SHE problem shows considerable interest in the last decade. Throughout the literature reviewed, many techniques and mathematical approaches were proposed and investigated to solve the SHE problem in multilevel inverters. In general, the proposed solution techniques can be classified into: 1) iterative techniques, 2) resultant theory techniques, or 3) heuristic optimisation techniques.

Newton Raphson (NR) is the most common iterative technique used in the literature [68]. It is widely applied and has been implemented to calculate switching angles in multilevel inverters. Two of the main advantages of NR are: 1) it is easy to implement and 2) it is efficient at eliminating low-order harmonics. However, it suffers from the following drawbacks: 1) it needs a good initial guess for switching angles to converge, 2) it does not find solutions over the entire range of the modulation index and 3) difficulty of converging with higher numbers of inverter levels.

Other authors have suggested the application of resultant theory to solve the SHE problem in multilevel inverters [69]. With this method, the transcendental equations are transformed to polynomial equations to be solved using resultant theory. The main drawback of this approach is that as the levels in the inverter increase, the number of transcendental equations to be solved increases. Consequently, the degree of the polynomials will be large; thus, the computation burden increases, and the problem becomes more difficult to solve.

A more recent approach is to solve the SHE problem by applying heuristic algorithms such as: particle swarm optimisation (PSO), genetic algorithm (GA), simulated annealing (SA), tabu search (TS) and so forth. Heuristic algorithms were found to be powerful and can solve the problem by applying artificial intelligence. The main idea here is to transform the SHE problem into an optimisation problem. The optimizer is designed to minimize the THD with maintaining the desired fundamental component and to eliminate dominant low-order harmonics as constraints on optimisation. Key advantages of heuristic algorithms in solving the SHE problem are: 1) as well as the elimination of low-order harmonics, it can minimize THD, 2) solving capability for the entire range of the modulation index and 3) an initial guess of switching angles is not required. In [70], GA was applied to find optimum switching angles, while paper [71] investigated PSO's capacity to solve the SHE problem.

As a preliminary study of this research work, the ability of NR, PSO and GA to solve the SHE problem of a seven-level CHB-MLI was investigated [72]. In this paper, the performance of GA and PSO was much better than NR as shown in Table 4-4, in which "**" indicates no convergence.

Table 4-4: Solving the SHE Problem Using Different Methods (NR-PSO-GA)

M_i	Θ_1			Θ_2			Θ_3			% THD		
	NR	PSO	GA	NR	PSO	GA	NR	PSO	GA	NR	PSO	GA
0.1	**	39.3	8.0	**	59.6	34.3	**	81.1	88.9	**	10.5	8.2
0.2	**	7.6	24.7	**	34.0	52.5	**	88.7	66.5	**	8.1	8.0
0.3	46.4	7.6	24.5	83	33.9	52.5	89.6	88.6	66.2	28.1	8.1	8.0
0.4	40.5	13.2	13.2	65.1	34.3	34.3	88.9	60.0	60.0	17.2	6.4	6.4
0.5	39.4	13.1	5.3	56.3	34.1	16.9	80.1	59.9	35.6	11.7	6.4	5.2
0.6	33.5	13.1	5.3	54.8	34.0	16.7	67.1	59.9	35.3	10.3	6.4	5.2
0.7	18.3	5.3	5.3	44.1	16.6	16.6	64.4	35.0	35.0	11.4	5.2	5.2
0.8	11.5	5.4	5.4	28.7	16.5	16.4	57.1	34.8	34.8	8.0	5.2	5.2
0.9	11.2	5.4	5.4	13.4	16.4	16.4	37.4	34.8	34.8	9.2	5.2	5.2
1	**	5.4	5.4	**	16.4	16.4	**	34.8	34.8	**	5.2	5.2

This PhD study set out to solve the SHE problem for different CHB-MLI levels. Due to its superiority over other conventional calculus methods, GA-based optimisation for solving the SHE problem was chosen for analysis. The next section presents a detailed explanation of how to apply GA-based optimisation to solving the SHE problem.

4.4.3 Implementation of GA to Determine Switching Angles in CHB-MLI

In order to implement GA for the SHE problem, MATLAB software was used as a simulation environment. Based on the basic flow chart of GA optimisation demonstrated in Figure 4.1, the main steps considered in the implementation of GA for solving the problem are:

- *STEP-1: Initialization*

In the design of a GA-based optimisation to solve the SHE problem in CHB-MLI, there are *S* number of switching angles to be determined in the solution. Each switching angle is considered a gene. The switching angles (genes) are coded in a binary string as the binary coding system was chosen for the problem. An individual solution or chromosome will be made from all genes – S switching angles in this case – where S is the number of cascaded H-bridges.

$$Chromosome = [\theta_1, \theta_2, \theta_{3,\ldots\ldots\ldots\ldots\ldots}, \theta_s] \quad 4.6$$

Where,

$$\theta_1 = [1\ 0\ 0\ 1\ 1], \theta_2 = [0\ 0\ 0\ 1\ 0], \ldots\ldots\ldots\ldots\ldots \theta_s = [1\ 0\ 1\ 1\ 0] \quad 4.7$$

In this study, the population size was chosen as (30). For n-level CHB-MLI, there will be S switching angles to be calculated. At the initial population, θ_1, $\theta_{2,\ldots}\theta_s$ are assumed randomly to start the solution. This is a constrained optimisation, with a constraint stating that angles should be in ascending order between 0° and 90°, as per Equation 4.5.

- *STEP-2: Evaluating Fitness Function*

As the objective function significantly affects optimisation performance, it should be defined carefully. The purpose of the proposed GA-based optimisation model for SHE is to have the desired fundamental component, eliminate the low-order dominant harmonics and minimize THD at the output of the inverter. The following objective function has been considered for analysis and found to be effective in eliminating the undesired low-order harmonics, while maintaining the required fundamental component [11, 72]:

$$Obj_F = |V_1 - SM_i|^4 + |V_5|^2 + |V_7|^2 + \cdots + |V_z|^2 + \%THD \quad 4.8$$

Where V_1, V_5 and V_7 are the amplitudes of the fundamental 5^{th} and 7^{th} harmonics, respectively, V_z is the highest odd harmonic that can be eliminated, S is the number of cascaded H-bridges. The objective function is used as a measuring tool to test the goodness of individual solutions generated at the first step.

- *STEP-3: Selection*

Here, the individuals with higher fitness values are selected from the population. In this investigation, the tournament-selection method was used.

- *STEP-4: Crossover and Mutation*

Crossover and mutation are the last genetic operators to be applied in the optimisation. The scattered and constraint-dependent functions were applied for crossover and mutation, respectively.

➢ *STEP-5: Stopping Criterion*

This determines when the algorithm stops. In the case of either of the following two conditions being satisfied, the algorithm should terminate: 1) the number of iterations reaches 100 generations, or 2) the weighted average change in the fitness-function value over 50 generations is less than the function tolerance of (1×10^{-6}).

4.5 CHB-MLI High-Voltage Power Switches

Power-semiconductor devices are used for switching and are considered to be the main building blocks of any power-electronics system. These devices are either uncontrolled (e.g. diodes), half-controlled (e.g. thyristors), or fully-controlled (e.g. insulated gate bipolar transistors (IGBTs), gate turnoff thyristors (GTOs) and integrated gate commutated thyristors (IGCTs)). They are commercially available at different ratings, characteristics and costs, so they can suit a wide range of power applications. Figure 4.9 presents the commercially available power-semiconductor devices [6].

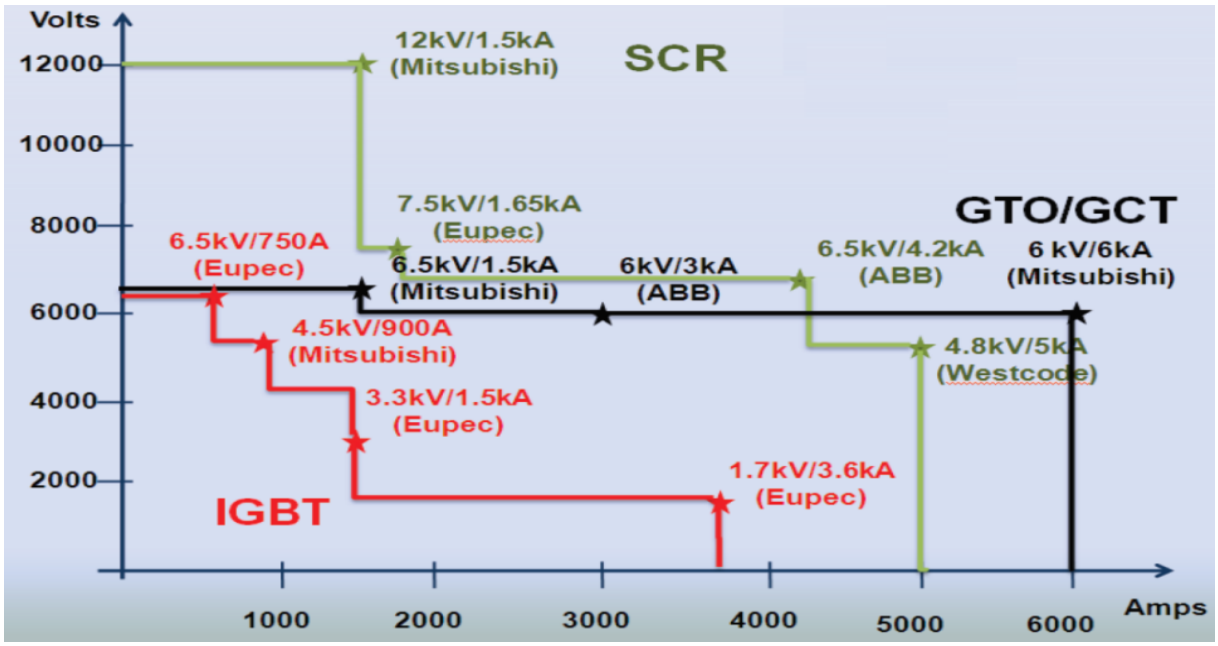


Figure 4.9: Commercially available power-semiconductor devices. [6]

The history of the power-semiconductor device revolution started in 1958 when silicon-controlled rectifiers (SCRs) became commercially available. Since then, there have been two milestone improvements in power-semiconductor devices: 1) when insulated gate bipolar transistors (IGBTs) were introduced in the 1980s and 2) the invention of integrated gate commutated thyristors (IGCTs) in the late 1990s, which is still considered to be recent technology. [6]

In practice, IGBTs are dominant and the most widely applied valve for medium-voltage–high-power multilevel VSI applications. High-voltage insulated gate bipolar transistors (HV-IGBTs) are replacing the gate turnoff thyristors (GTOs) for medium- and high-power applications. This is mainly due to feature advantages: 1) low on-state voltage drop, 2) superior on-state current, 3) modularity, 4) reduced cost, 5) easily controlled, 6) excellent forward and reverse blocking capability and 7) well-established mature device [73].

For this study, IGBTs were considered for CHB-MLIs power-semiconductor switches. Table 4-5 summarizes commercially available IGBT modules at different ratings, along with the associated cost for each module, which were considered in the analysis. Practically speaking, it is recommended that HV-IGBTs be operated at only 50–60% of blocking-voltage capability. This is to ensure a reliability of 100 FIT, where 1 FIT represents one failure in 10^9 operation hours [74].

Table 4-5: Selected IGBTs for Medium-Voltage–High-Power Applications

IGBT Device Ratings		Device Name	Manufacturer	Cost/Module (£)
Voltage (kV)	Current (A)			
1.7	400	FZ400R17KE3	Infineon	213
2.5	400	CM400DY-50H	Mitsubishi	375
3.3	400	FZ400R33KL2c-B5	Infineon	855
4.5	400	CM400HB-90H	Mitsubishi	1,125
6.5	400	FZ400R65KE3	Infineon	2,000

4.6 Precise Modelling for Power-Loss Calculation in Different-Level CHB-MLIs

Power dissipation in electronic devices, which involves switching semiconductors, is categorized into four types: 1) conduction losses, 2) switching losses, 3) off-state losses and 4) gate losses. The off-state and gate losses are small and are normally ignored [75]. Accordingly, only conduction and switching losses have been considered in the current research. The aim of this section is to propose a generic model for precise calculation of conduction and switching losses in CHB-MLI. The proposed model can be applied for any multilevel inverter topology, any number of levels and with any applied control techniques.
The model is based on an online calculation in which MATLAB-SIMULINK software was used for modelling. This section is based on the papers published by the author [76, 77].

4.6.1 Literature Review of Power-Loss Estimation in Multilevel Inverters

Compared to two-level inverters, the estimation of inverter-power losses is a complicated task for multilevel inverters. The usual conventional methods used to estimate losses in two-level inverters are not suitable for application in multilevel inverters. The main reason is that in multilevel inverters, each semiconductor device has a different current than other devices, which implies different power-loss behaviour for each device. This results from having a different on-state ratio for each device during one period of output-phase voltage. Furthermore, with a higher number of levels, the switching frequency of each device is different ,which adds more complexity to the estimation process.

In the literature, different methods have been suggested and applied to calculate power loss in multilevel inverters. Some of these methods are based on an online estimation from the simulated circuit, and some are based on deep mathematical analysis and evaluation. Ramu et al., proposed a method in which each IGBT was modelled with characteristic curves using curve-fitting exponential equations as a function of load current to calculate the losses [78]. Then, the power loss was calculated for a five-level CHB-MLI. This approach is not correct as it considers the same load current for all switches and antiparallel diodes. In practice, each power switch has its own current based on the applied switching function in multilevel inverters. Drofenkin and Kolar improved the procedure for loss-estimation in power electronic circuit simulations [79]. Their model is helpful for implementing the online estimation of conduction and switching losses in circuit simulations. In other paper, switching functions have been used to model inverter losses for a three-phase–nine-level

cascaded H-bridge inverter in which the load was assumed to be a mixed RL load and the modulation index was 0.85 [80]. The main drawback of this method is that it is not generic; it is only applicable for selective harmonic-elimination control and for a nine-level CHB-MLI circuit. In case the applied control technique or inverter levels were changed, different modelling is required.

Previous studies used online modelling to calculate losses by applying curve fitting to characterize the IGBT based on the device datasheet. However, another approach has been proposed for estimating power losses in multilevel inverters, which evaluates losses mathematically [81-83]. In this approach, a mathematical model is introduced in which the voltage across the switch is modelled by a threshold voltage and a series resistance. The main drawback in this approach is lack of accuracy as it only gives an approximation of the losses.

This section implements a new generic model for precisely calculating conduction and switching losses in CHB-MLIs, based on the method applied in [79], with some modification to make it suitable for application in multilevel inverters. A clear and efficient procedure is explained in detail, which should serve as a guide to loss evaluation for multilevel inverters. The proposed modelling will be based on an online simulation in which inverter losses are precisely calculated, with less computational effort. The proposed method is generic and can be applied to any multilevel topology with any number of levels. The complete general block diagram for the proposed model of loss calculation in CHB-MLIs is presented in Figure 4.10

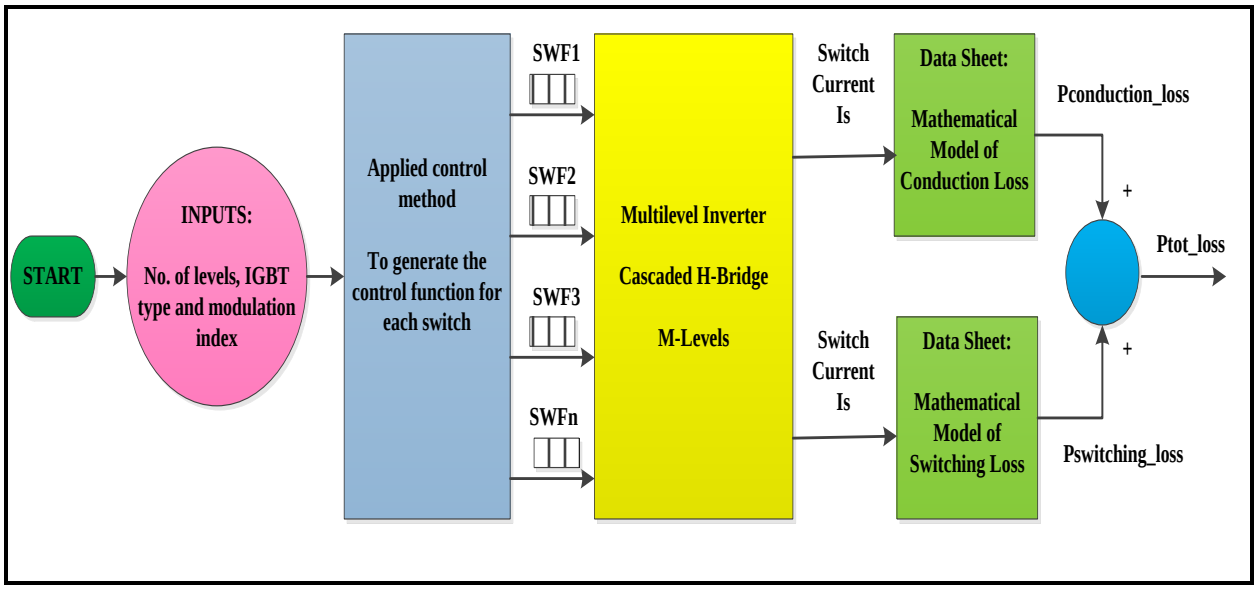


Figure 4.10: General flow model of proposed methodology for precise calculation of power losses in CHB-MLI.

4.6.2 Proposed Model for Conduction-Loss Calculation

For a semiconductor device, the power losses that occur while the power device is in the on-state and conducting current, is defined as the device-conduction power loss. In CHB-MLI, the conduction loss increases proportionally with the number of cascaded cells. At conduction, the power dissipation can be computed by multiplying the on-state saturation voltage by the on-state current, and this is illustrated in the next equation.

$$P_{Conduction} = |i_c| \, . \, v_{on} \qquad 4.9$$

The absolute value is taken as the conducting current is always positive for the device. Most of the literature has modelled on-state voltage by inserting a voltage source (V_o), representing the device's voltage drop (called threshold voltage), and a resistor (r_{on}), representing the current dependency in series with the ideal switch. The main drawbacks of this modelling approach are [76, 77, 79]:

1) Additional parameters to be added in series with the ideal switches, hence partially rebuilding the circuit.
2) The model might not be accurate as it is not based on actual curves given in the device datasheet.

In the proposed model, the power-conduction loss is computed more easily and efficiently. The on-state voltage is represented by a mathematical equation in terms of the on-state current. This mathematical equation is obtained by applying a curve-fitting tool to the actual characteristic device curves as given in the device datasheet. For each power device, there will be two mathematical equations, one for the IGBT switch and one for the antiparallel diode. Hence, in the MATLAB-SIMULINK model, the pure IGBT switch current and the pure diode current need to be obtained separately. This can be achieved by plotting the on-state device current, in which the positive portion of the power-switch current above zero representing the pure IGBT current, and the negative portion below zero representing the pure diode current. With these currents separated, the conduction loss for the IGBT switch and diode can be calculated by simply applying the power-conduction loss-calculation block shown in Figure 4.11.

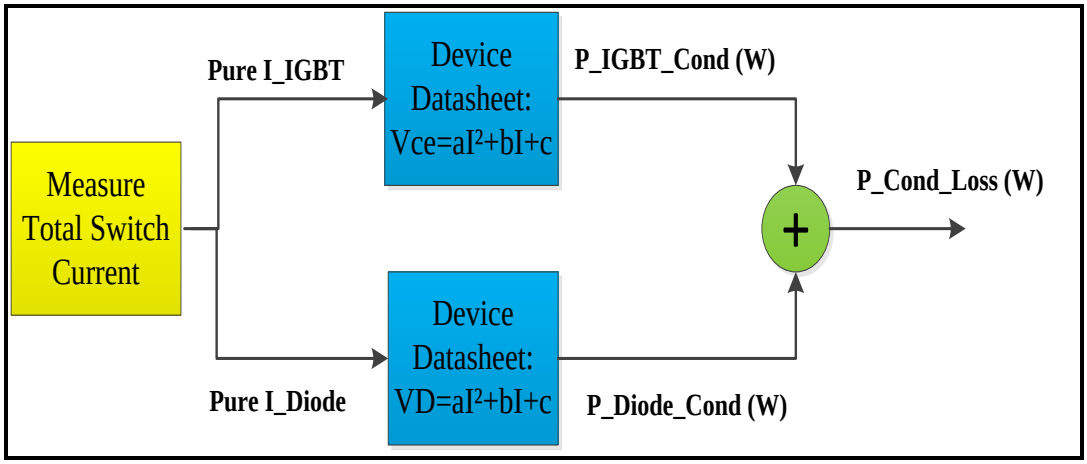


Figure 4.11: Conduction power-loss calculation block. [76, 77]

4.6.3 Proposed Model for Switching-Loss Calculation

Switching-power losses can be defined as the power dissipated during turnon and turnoff switching of the power-semiconductor device. It occurs in both the IGBT switch and the antiparallel diode. The power-switching loss is highly proportional to the switching frequency, and hence it substantially contributes to the inverter's total power losses, especially for inverters controlled by SPWM. For each power switch in the inverter, there is turnon energy loss (E_{on}) and turnoff energy loss (E_{off}). However, for the antiparallel diode, only turnoff (E_{rec}) energy loss is considered, while turnon loss is normally ignored due to fast conduction of the diode when it becomes forward biased. In modern diodes, the turnon loss is less than 1% compared to the turnoff loss [84].

In practice, five main factors affect the behaviour of switching loss: 1) current being switched, 2) blocking voltage, 3) junction temperature, 4) gate resistor and 5) wiring stray inductance [79]. Switching loss is considered a major drawback in multilevel inverters, causing significant increases in system cost and reducing efficiency in HVDC applications.

This study proposes an online estimation of switching-power losses based on the switching-energy curves in the semiconductor-device datasheet. Mathematically, switching-power losses are energy losses multiplied by switching frequency.

$$P_{IGBT\_Switching} = \left(E_{on} + E_{off}\right) \times f_{sw} \qquad 4.10$$

$$P_{Diode\_Switching} = E_{rec} \times f_{sw} \qquad 4.11$$

In the datasheet of a semiconductor device, three energy curves are given: IGBT turnon (E_{on}), IGBT turnoff (E_{off}) and diode turnoff (E_{rec}). This study considered the curves with the highest temperatures. These energy curves are given in terms of device current. First, an energy-factor curve (F) is introduced, which can be obtained when dividing energy by switching current.

$$F = \frac{E}{I} \qquad 4.12$$

This will result in three new curves for the energy factor in terms of current. Then, a curve-fitting tool is applied to model these energy-factor curves using a mathematical equation. Multiplying the energy-factor curve equation by the switching current should give the switching-energy losses, which are further multiplied by switching frequency to obtain switching-power loss. In case the blocking voltage is different, a normalization factor is applied to the switching-power loss block to consider this in the calculation. Figure 4.12 demonstrates the block implemented for the switching-power loss calculation.

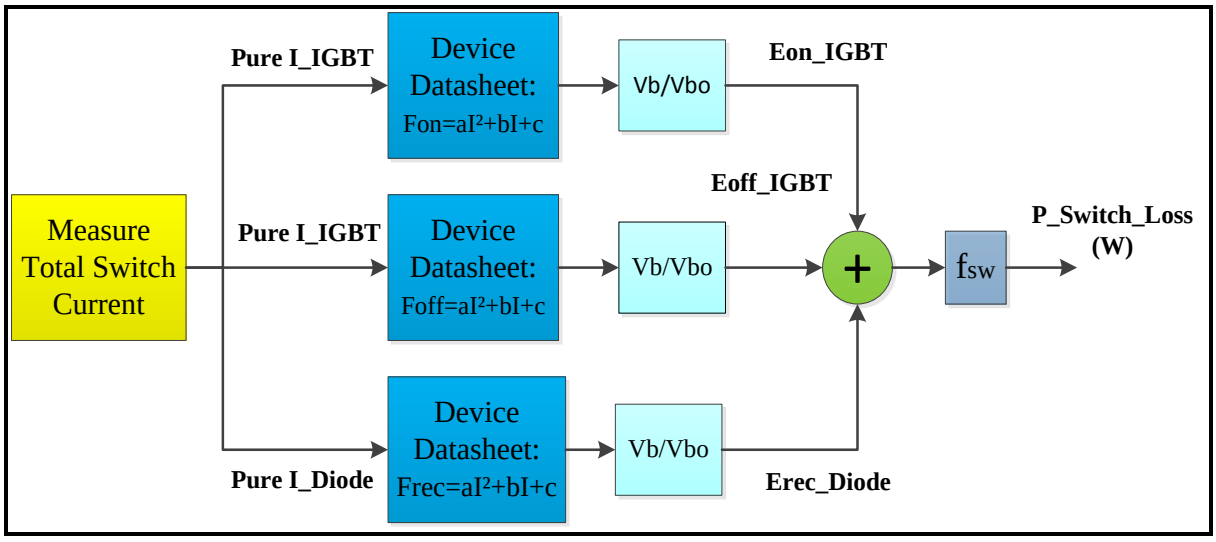


Figure 4.12: Switching-power losses calculation block. [76, 77]

4.7 Passive Power Filter (PPF) Optimisation

4.7.1 Overview of the Problem

While harmonics have adverse effects on both power utilities and customers, harmonic filtering is considered the most widely applied method among different harmonic-mitigation techniques. This section discusses the implementation of passive power filters (PPFs) at the output of investigated CHB-MLIs as PPFs are currently more economical and commonly applied than APFs, as discussed in Chapter Three. The function of the added shunt filter is to ensure that the harmonics profile is well below the recommended limits, as per the IEEE-519 power-quality standard. The proposed PPF should be based on cost-effective design.

First, the modelling of a composite PPF bank is demonstrated. Then, the key design parameters for a cost-effective PPF are illustrated. For PPF design, there are two main approaches, which either use a: 1) the conventional method, or 2) a heuristic method. The conventional approach is considered an old methodology in PPF design, but it suffers from several drawbacks and is not capable of finding the optimum design. The key design steps of this approach are illustrated, with the main drawbacks highlighted. Conversely, heuristic methods are powerful optimisation tools that can assure optimum design for PPF problems when properly applied.

The optimum design of PPF for electrical power systems should reduce the THD of currents and voltage at PCC below the recommended limits stated in power-quality standards. Furthermore, appropriate PPF design should minimize proposed filter costs. In this study, an optimisation model of PPF design based on genetic algorithm (GA) is proposed as a heuristic approach has many advantages over the conventional design approach. The essential design steps of successful GA optimisation for PPF design are addressed in this section to optimize the trade-off model for the assigned problem.

4.7.2 Implemented Model of Composite PPF Bank

PPFs are widely employed in electrical and industrial power systems compared to APFs because PPFs are simple in design, cheap and effective. There are different PPF topologies, which are classified into tuned and high-pass filters. These topologies were critically reviewed in Chapter Three. Among all PPF topologies, the composite topology is commonly applied for high-power applications to assure reduction of harmonics below IEEE-519 limits.

While the shunt single-tuned filters are to be tuned to eliminate low-order harmonics, the second-order high-pass filter eliminates most of the higher-frequency harmonics. The PPF provides a low-impedance path for the tuned-harmonics currents and provides reactive-power compensation at the fundamental frequency [85]. A typical circuit layout for the implemented composite PPF at the output of the CHB-MLI is demonstrated in Figure 4.13.

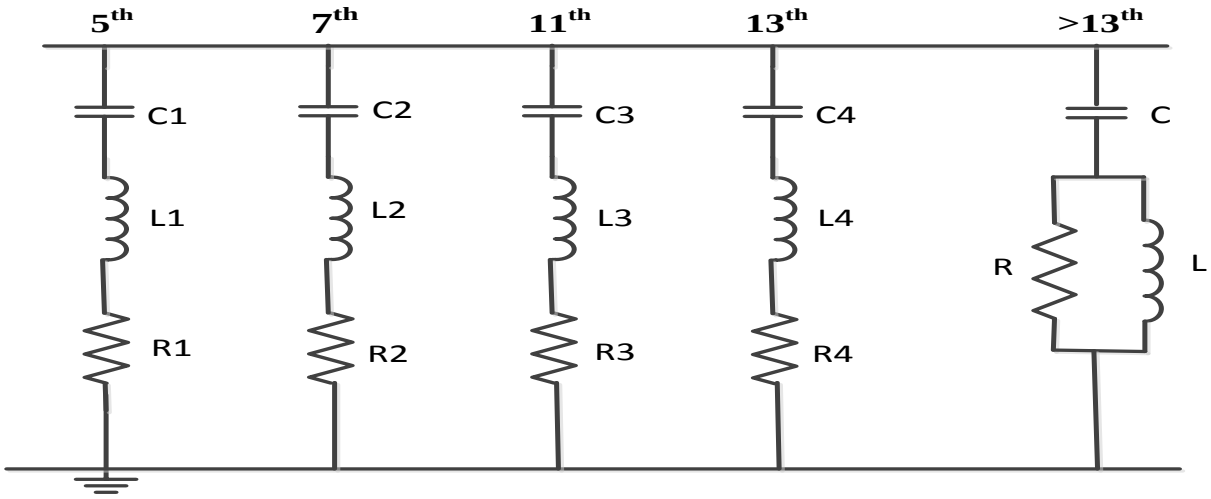


Figure 4.13: Proposed PPF circuit layout at the CHB-MLI output.

4.7.3 Key Design Principles and Considerations

PPF design is a complicated task as it should consider many parameters in the design stage such as: filter size, filter cost, power losses, system configuration and the harmonics limits defined in power-quality standards. Table 4-6 illustrates the key design principles and considerations for appropriate PPF design [53, 86].

Table 4-6: Key Design Principles and Considerations for Efficient PPF Design

- Filter-design parameters C, L and R should satisfy the filtering objective.
- The filter should compensate the system reactive-power demand at fundamental frequency.
- Lower harmonic contents of voltage and current at PCC below the limits recommended in power-quality standards.
- Minimize total filter cost.
- Higher power factor at PCC.
- Avoid series or parallel resonance between filter impedance and system impedance.

4.7.4 Conventional Versus Heuristic Methods for PPF Design

The design output should be the passive parameters of the filter R, L and C and the filter size. In this section the two main approaches for PPF design, namely 1) conventional approach and 2) heuristic approach, are illustrated.

4.7.4.1 Conventional Approach

In the conventional design, the PPF is designed based on several factors: 1) harmonics order to be eliminated, 2) reactive-power demand of the system and 3) system configuration [85]. The designer should have detailed system information, including system impedance, loads and harmonics profile. This design method is simple to apply. However, it does need engineering experience and might not result in the optimum design solution. PPF size can be defined as the reactive power generated by the filter at fundamental frequency. The conventional design method for a single-tuned PPF can be summarized in the following steps [40]:

1) Assign the system demand of reactive power and calculate the capacitor size C,

$$C = \frac{Q_{demand}}{w_o V^2} \tag{4.13}$$

2) Solve filter inductor size L in terms of capacitor value and tuned frequency,

$$L = \frac{1}{w_n^2 C} \tag{4.14}$$

3) Optimum quality factor Q, which gives the lowest harmonic voltage, is obtained by:

$$Q = \frac{Cos \emptyset_m + 1}{2 \delta sin\emptyset_m} \tag{4.15}$$

Where, $\emptyset_m$ is the maximum phase angle of network impedance, and δ is the relative frequency deviation and is given by:

$$\delta = \frac{\Delta f}{f_n} + \frac{1}{2}\left(\frac{\Delta L}{L_n} + \frac{\Delta C}{C_n}\right) \tag{4.16}$$

Here, f_n , C_n and L_n are the nominal values of frequency, capacitance and inductance.

4) The size of the filter resistor R, is then computed:

$$R = \frac{1}{w_n \, Q \, C} \tag{4.17}$$

The conventional PPF design approach essentially relies on engineering experience and requires more detail about the electrical power system under investigation. Furthermore, it does not achieve optimum filter design. Because of these drawbacks, researchers have investigated and applied more efficient methods to solve the problem.

4.7.4.2 Heuristic Approach

The problem of PPF design is considered to be a combinatorial optimisation problem that can be solved by applying artificial intelligence. In recent literature, heuristic methods have been extensively used to design PPFs. The problem is solved as an optimisation problem in which multi-objectives can be minimized in the design, subject to operational and technical constraints. Generally, multi-objective optimisation can be written as:

Minimize objective function, subject to equality and inequality constraints:

$Min.\,(\,f_1(x), f_2(x), \ldots\ldots\ldots f_k(x)\,)$,

Subject to: (4.18)

$x = (x_1, x_2, \ldots\ldots\ldots\ldots x_k) \in X$

Heuristic methods are powerful optimisation techniques and have many advantages such as: no requirement for detailed information about the power system and ability to achieve optimum PPF design compared to the conventional method. In addition, the cost of PPF implementation can be added to the optimisation objective, which is not considered in conventional design. Hence, design using heuristic methods is more practical, and the designed PPF will perform better and cost less compared to one designed using the conventional approach.

In the literature, many researchers addressed the PPF design problem and implemented heuristic optimisation to solve it. Simulated-annealing-based multi-objective optimisation has been applied for optimal planning of PPFs [87]. It has also been adopted to optimize the cost

of PPF as an objective function, with applicable constraints such as power factor, filters' lower and upper limits for VARs, THD and voltage at PCC [88]. Others papers suggested a genetic algorithm (GA) to optimize PPF design [89, 90]. Juan et al. found that the application of GA in the design of PPF results in better harmonics suppression and lower initial filter cost compared to the conventional design method [60]. In their optimisation model, two objectives were minimized in the design: 1) current total harmonic distortion (THD_i) and 2) filter cost. The reactive-power compensation was applied as a constraint for the optimisation. The multi-objective optimisation design of PPFs has also been solved using the particle swarm optimisation (PSO) method [91]. Huang et al. proposed an optimisation approach for optimal PPF design in a hybrid power filter based on PSO [86].

The heuristic design approach overcomes problems associated with PPF design using the conventional design approach. In this study, a GA-based optimisation model is implemented for PPF design at the output of the CHB-MLI. The detailed steps of the implemented GA optimisation for composite PPF design are presented in the following section.

4.7.5 GA-Based Optimisation for PPF Design

Improper parameter design of the PPF will result in poorer filtering, higher cost, resonance with system impedance and overcompensation of reactive power [91] . The size of filter elements is discrete in nature and this should be considered in the optimisation process. The problem of PPF design is a combinatorial optimisation, which has a non-differentiable objective function, with many constraints. This section proposes an optimized PPF design approach based on GA. The four optimisation objectives are: 1) initial investment cost, 2) power-loss cost, 3) THD filtering effect and 4) reactive-power compensation.

The filter to be optimized comprises multiple single-tuned filters in parallel with a 2nd order high-pass filter. The unknown variables are the fundamental reactive-power Q_{c1} injected by each filter branch. Once determined, the filter parameters can be easily calculated. The implemented GA optimisation for the single-tuned and the 2nd order high-pass filters are demonstrated below.

4.7.5.1 Single-Tuned PPF Design

In the design of shunt single-tuned PPF tuned for the n[th] harmonic order, the branch impedance Z_{SHn} can be expressed as follows [92]:

$$Z_{SHn} = R_{SH} + j\left(nX_{LSH} - \frac{X_{CSH}}{n}\right) \quad 4.19$$

First, the reactive power, Q_{SH1} supplied by the shunt single-tuned branch at fundamental frequency is determined. Based on the value of Q_{SH1}, the magnitude of the fundamental capacitive reactance of the shunt-tuned branch X_{CSH} can be calculated simply by applying the following formula:

$$X_{CSH} = 3 \times \frac{n^2}{n^2 - 1}\left(\frac{V_{L1}^2}{k * Q_{L1}}\right) = 3 \times \frac{n^2}{n^2 - 1}\left(\frac{V_{L1}^2}{Q_{C1}}\right) \quad 4.20$$

Where V_{L1}, is the fundamental voltage at the tuned shunt branch and Q_{L1} is the load-reactive-power demand at fundamental frequency. In practice, the shunt-capacitor components are available in discrete incremental steps of reactive-power ratings. In Equation 4.20, (k) is a factor that takes this into consideration and allows for incremental discrete steps of Q_{C1}. In this study, a step of 50 kVar was used as per recommendations for low-voltage industrial power application [92, 93].

Then, the magnitude of the fundamental inductive reactance X_{CSH} and the resistance R_{SH} of the shunt single-tuned branch can be calculated based on the value of the capacitance X_{CSH}, quality factor Q and the harmonic order as shown below:

$$X_{LSH} = \frac{X_{CSH}}{n^2} \quad 4.21$$

$$R_{SH} = \frac{X_{CSH}}{nQ} \quad 4.22$$

In a single-tuned PPF, it is important to choose the optimum value of the filter quality factor (Q), which indicates the tuning sharpening of the filter. Based on the literature and engineering experience, (Q) values range from 30 to 60 [91]. This study sets the value of the quality factor as 60 for all single-tuned filters to assure the best filter performance [60, 94].

4.7.5.2 High-Pass PPF Design

Similarly, for the high-pass filter branch, the impedance of the high-pass filter is given by [53]:

$$Z_{Hn} = -j\frac{X_{CH}}{n} + \left(\frac{1}{R_H} + \frac{1}{jnX_{LH}}\right) \quad 4.23$$

Once the injected fundamental reactive power Q_{c1} of the high-pass filter is determined, the magnitude of the fundamental capacitive reactance of the shunt high-pass filter branch X_{CH} can be calculated simply by applying the following formula:

$$X_{CH} = 3 \times \frac{n^2}{n^2-1}\left(\frac{V_{L1}^2}{k * Q_{L1}}\right) = 3 \times \frac{n^2}{n^2-1}\left(\frac{V_{L1}^2}{Q_{C1}}\right) \quad 4.24$$

Then, the magnitude of the resistance R_H, the fundamental inductive reactance X_{LH} and the shunt high-pass filter branch can be calculated based on the value of the capacitance X_{CH}, quality factor m and the harmonic order as shown below:

$$R_H = \frac{X_{CH}}{n} \quad 4.25$$

$$X_{LH} = \frac{m\,R_H}{n} \quad 4.26$$

Here, m is the damping-time constant ratio, which usually takes a value between [0.5, 2]. In this study, m is chosen to be equal to (0.5) as this results in minimum losses [60].

4.7.5.3 Objective Function and Constraints Formulation

In order to satisfy the key design principles and considerations given in Table 4-6, the following objectives have been set for the optimisation:

- Objective 1: Minimize the total harmonic distortion of the output voltage THD_v

$$f_1 = Min.THD_v \quad (4.27)$$

$$THD_v = \sqrt{\sum_{n=2}^{\infty}\left(\frac{U_n}{U_1}\right)^2} \quad (4.28)$$

Where:

THD_v is the total harmonic distortion of output voltage.

U_n is the n^{th} harmonic of output voltage.

U_1 is the fundamental of output voltage.

- Objective 2: Minimize the system-capital cost and energy-loss cost.

$$f_2 = Min.\left(f_{Capital\_Cost} + f_{Operating\_Cost}\right) \quad (4.29)$$

Richards et al. presented a method to compute the total capital-investment cost of a single-tuned PPF [95]. Here, the capital-investment cost of the filter is calculated based on the size MVAR ratings of the filter. In this study, the cost of a single-tuned and high-pass filter is calculated as follows:

$$f_{Filter\_Cost}(£) = U_C \times Q_C + U_L \times Q_L \quad (4.30)$$

Where, U_C and U_L are the unit cost of capacitor and inductor in (£/MVARs), respectively. In this optimisation, both cost of capacitor and inductor are assumed to be equal in order to maintain simplicity and obtain generic optimisation, so that $U_C = U_L = 10{,}000\ £/\text{MVAR}$ [96].

The other capital cost to be included in the trade-off optimisation is the total capital cost of purchasing IGBT valves for the inverter. This cost is not fixed and will change as the inverter's number of levels change; it can generally be calculated as follows:

$$f_{IGBT\_Capital\_Cost}\ (£) = IGBT_{Cost}\ (£) \times\ Total\ No.of\ IGBTs \qquad 4.31$$

However, the operating cost of the system is mainly the cost of energy losses. It is calculated in terms of equivalent annualized capital cost by applying the present value factor as shown below [96]:

$$f_{Operating\_Cost}\ (£) =\ H\ \times U_{Energy} \times \frac{(1+i)^y - 1}{i(1+i)^y} \times\ P_{loss} \qquad 4.32$$

Where:

H : is total operating hours annually (h/year)

U_{Energy} is the energy cost in (£/kWh),

i : is the annual interest rate for capital cost, which is assumed to be 5%,

y : is the levelaization period or system lifetime (years), which is assumed to be 15 years.

The interest rate for the cost of integration system for renewable energy was assumed to be 5 %. This was an assumption to test the developed trade-off model. However, in reality the cost of debt and the required return on equity, as well as the ratio of debt-to-equity, varies between individual projects and countries depending on a wide range of factors. The model is generic and depending on the project in which it was applied, accurate interest rate can be added.

- Objective 3: Maximize the generated fundamental reactive power supplied by the filter. This will give the maximum possible power factor for the optimisation.

$$f_3 = Max. \sum Q_i \qquad 4.33$$

Where Q_i is fundamental reactive power supplied by the i^{th} filter.

In order to combine all three objectives into one function and simplify the fitness function, a weighted multi-objective technique is implemented. The three objectives are transformed into one objective function as shown below:

$$Min.\,[\,w_1 f_1 + w_2 f_2 + w_3 (C - f_3)] \tag{4.34}$$

Here, C is a large constant to ensure that $(C - f_3)$, is always a positive number. In this equation, the weighting factors w_1, w_2 and w_3 are given the values 0.5, 0.4 and 0.1, respectively.

GA will minimize the objective function stated previously. However, there are some constraints for the optimisation that should be considered, as follows:

- *IEEE-519 Standard*

  Based on the standard, for voltage levels up to 69 kV, THD_v should be kept under 5%, and non-individual voltage harmonics should exceed 3%. Similarly, THD_i follows the standards limits according to the system short-circuit ratio.

- *Load Power Factor*

  PPF compensation for reactive power should maximize the power factor, and at the same time, the system should not be overcompensated. For this reason, there are compensation limits for a minimum and maximum reactive power that can be supplied by the filter, according to the desired load power factor. In this optimisation, the power factor is targeted to be between 92% and 98%.

$$Q_{min} \leq \sum Q_i \leq Q_{max} \tag{4.35}$$

4.8 Summary

This chapter addressed an important existing problem for the trade-off of multilevel inverter's number of levels and size of output filter in PV power-plants for medium-voltage-high-power applications. A general trade-off model was proposed. The model considered the key evaluation measures: 1) the %THD, 2) power losses, 3) filter size and 3) cost. To optimize the inverter control, GA was implemented to solve switching angles for the SHE problem. The main reason is that heuristic techniques are able to find a solution over the complete range of the modulation index and also to minimize THD. Furthermore, heuristic techniques can solve the SHE problem, even for a higher number of levels when iterative or resultant theory solutions are not able to converge, or become complicated.

Evaluation of power losses in multilevel inverters is a complicated task. The author proposed a generic model based on an actual device datasheet for power-loss evaluation in a multilevel inverter, which can be applied for any multilevel inverter topology and at any number of levels. The proposed model is an important tool for evaluating a key measure of the trade-off optimisation, which is power loss.

To ensure optimum design of the inverter output filter, a GA design approach based on filter cost and efficiency was considered part of the proposed optimum trade-off model for the inverter composite PPF design. The proposed optimisation model is generic in nature, which can be applied for any application and can achieve optimum design in the early planning stages.

The next chapter illustrates all the simulation results of the proposed models for SHE optimisation, power-loss calculations and filter GA optimisation.

CHAPTER 5: MODELLING AND SIMULATION OF THE PROPOSED OPTIMUM TRADE-OFF MODEL

5.1 Introduction

The rapid growth in medium voltage PV power plants has increased the potential to improve the efficiency of the integration system of the DGs that are connected to a grid. Voltage source multilevel inverters have become an attractive and efficient technology in this field. In Chapter 4, the author proposed a generic trade-off optimisation model for optimizing the number of levels and the size of the output filter used in a medium voltage CHB-MLI. The proposed model is based on the main key measures: %THD, power losses and system cost. Chapter 4 presented the detailed mathematical formulations of the trade-off problem.

This chapter presents the simulation results of the author's proposed model. The obtained results are analysed and discussed to show the performance validity of the proposed model. Matlab/Simulink was used to set the simulation environment.

5.2 Optimum Selective Harmonic Elimination for Different Number of Inverter Levels

5.2.1 GA performance in the SHE problem versus NR and PSO

As discussed in Chapter 4, the problem of SHE is solved efficiently by applying heuristic algorithms compared to other solution using iterative methods or resultant theory. Table 5-1 presents a comparison of the main approaches to solving the problem of SHE.

Table 5-1: Comparison of main approaches to solving the SHE problem

Iterative Methods	Resultant Theory	Heuristic Algorithms
➢ Easy to implement, but require good initial guess. ➢ Eliminate low-order harmonics efficiently. ➢ Do not find solutions over the entire range of modulation index. ➢ Difficult to converge for higher number of levels.	➢ The transcendental equations are transformed into polynomials to be solved using resultant theory. ➢ The degree of polynomial increases as the inverter level increases, which makes it difficult to solve.	➢ In addition to eliminating the low-order harmonics, they minimise the THD. ➢ Initial guess of switching angles is not required. ➢ Capable of finding a solution over the entire range of the modulation index.

The GA is superior in solving the problem of SHE, which was found in a primarily study conducted on 7-level CHB-MLI [72]. Figure 5.1 demonstrates the minimum THD obtained in this study by using NR, GA and PSO as solution methods. NR was not able to find a solution over the entire range of the modulation index, whereas both heuristic methods, GA and PSO, were able to find a solution over the entire range of the modulation index. Moreover, the performance of GA in solving the problem was better than that of PSO.

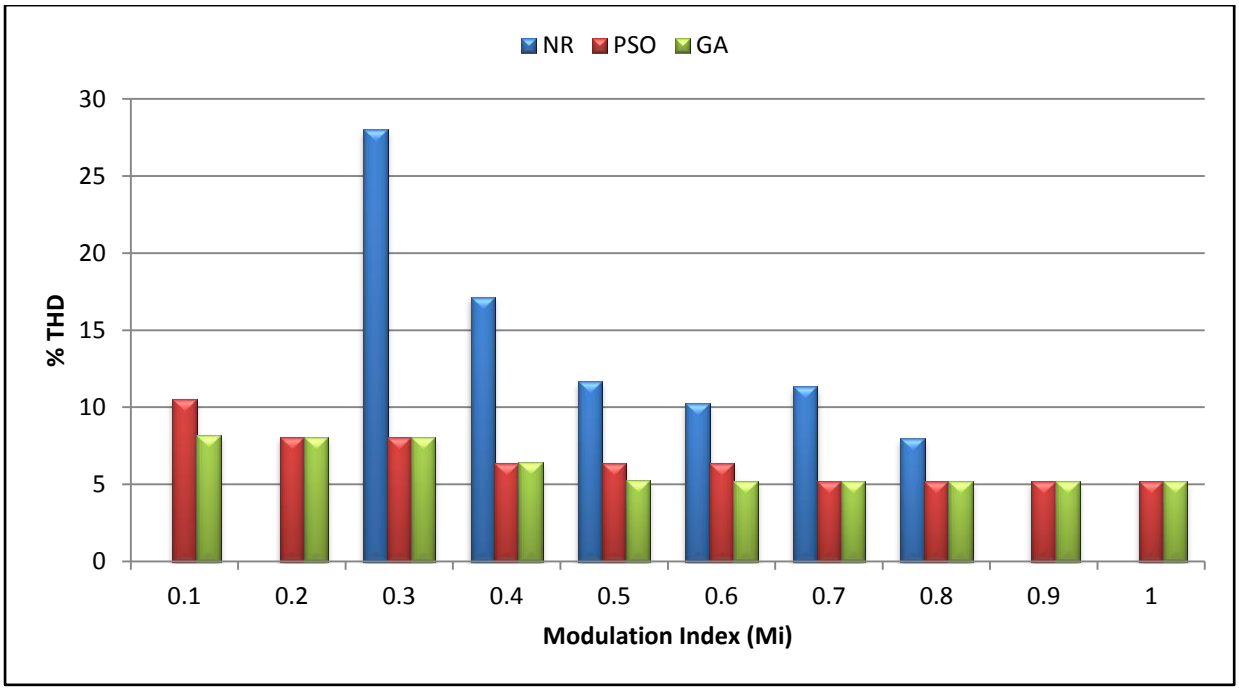


Figure 5.1: Minimum THD obtained for solving the SHE Problem Using NR-PSO-GA

5.2.2 GA solution of SHE problem for different inverter levels

In this section, the problem of SHE is investigated in multilevel inverters for levels 3–31 when the modulation index is varied. The problem is solved based on the proposed GA optimisation model, which was explained in Chapter 4. MATLAB software is used to perform all the required simulations. The objective is to eliminate the low-order harmonics and minimise the %THD.

Tables 5-2 to 5-11 present the optimum switching angles and the lowest %THD, which were obtained applying the SHE control technique to different levels of inverters (3 levels–31 levels). The results are shown are approximated to two decimal places. Modern digital control systems applying DSP can easily generates switching angles and such accuracy. The solution was generic for these levels at different modulation indices. The method applied to solve the problem of SHE was successful, and it minimised the %THD. Figure 5.2 illustrates the GA optimisation performed to solve the switching angles of the 11-level inverter. The proposed GA could solve the switching angles even in higher levels, which iterative methods cannot solve feasibly. The subsequent Tables 5-2 to 5-11, which show the switching angles, could be used by researchers to simulate and implement the optimal SHE control for different inverter levels.

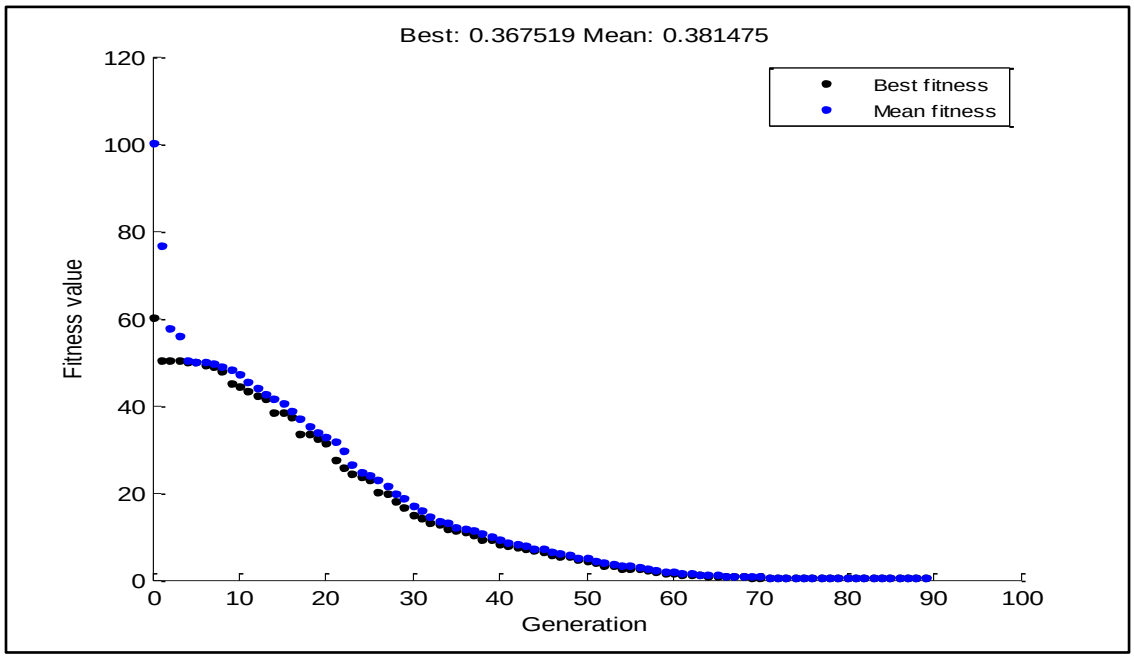


Figure 5.2: GA performance in solving SHE Problem in 11-level CHB-MLI

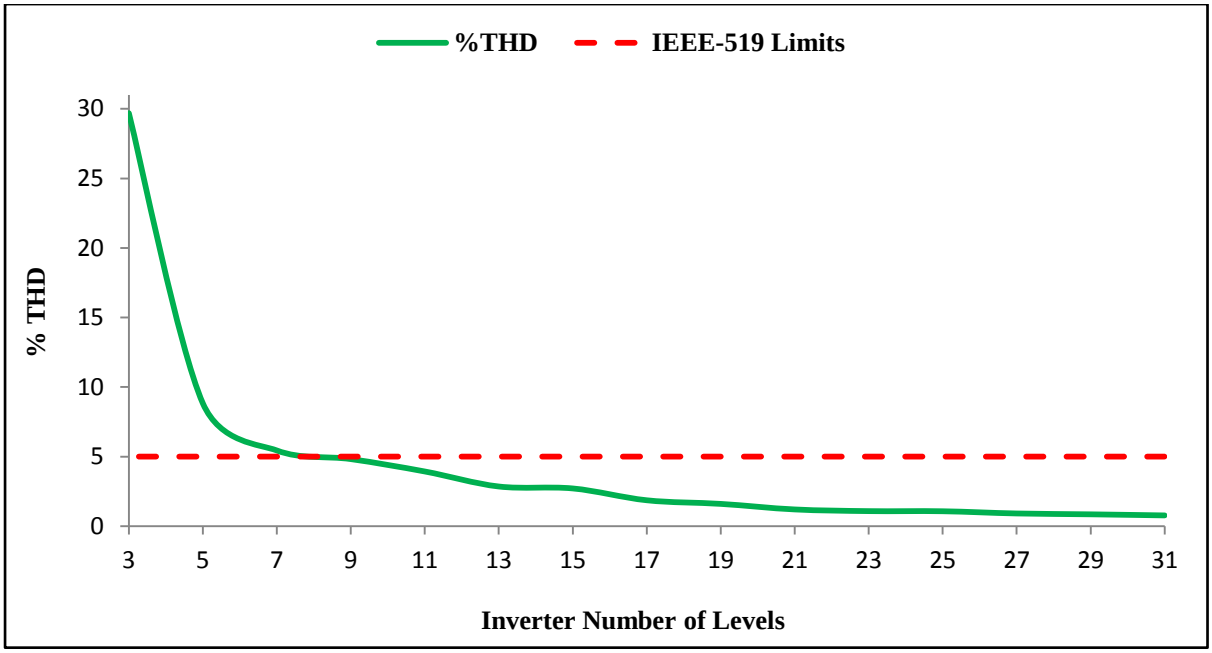


Figure 5.3: %THD versus inverter number of levels in the Modulation Index 0.9

Figure 5.3 shows an example of the %THD versus the inverter number of levels at modulation index 0.9. The simulated results indicated that as the number of levels increased, the THD at the output of the inverter decreased. It was observed that %THD was decreased gradually between adjacent levels as the number of levels increased. However, the reduction in %THD was saturated and became very slight between the higher levels. For example, the %THD declined by around 21% when the number of inverter levels increased from three to five. However, the %THD value dropped only by 0.08% when the number of inverter levels increased from 29 to 31. The curve fitting tool was applied to represent the relationship between the minimum obtained %THD and the number of inverter levels, as shown in Equation 5.1 where m is the number of inverter levels.

$$\%THD_{Min} = 121.62 \times m^{-1.479} \qquad 5.1$$

Figure 5.3 shows that when the SHE control was applied, the %THD of the inverter was less than 5%, which is the recommended IEEE-519 standard for a nine-level inverter and above. However, multilevel inverters with levels three, five or seven had %THD of above 5% at its output; hence, the output filter was required.

Table 5-2: Optimum SHE Switching Angles for Different Inverter Levels (M_i =0.95) Solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	29.67	9.11	5.56	5.30	3.13	3.54	3.27	2.91	3.82	1.12	2.34	1.62	1.25	1.79	0.72
$\propto_2$		26.73	16.68	11.80	8.89	8.55	7.83	5.54	4.29	5.12	3.87	3.96	4.03	2.91	3.26
$\propto_3$			35.81	23.07	18.18	12.86	9.65	10.04	8.52	7.95	7.32	7.04	5.69	5.83	5.73
$\propto_4$				38.67	27.31	23.08	18.65	14.96	13.44	11.65	10.65	9.22	9.10	8.13	7.17
$\propto_5$					41.00	28.83	23.01	19.95	17.25	14.68	13.01	12.66	10.57	10.63	10.10
$\propto_6$						42.35	31.62	26.18	22.44	20.24	17.36	14.93	14.12	12.25	11.52
$\propto_7$							41.49	32.66	27.73	23.69	21.13	18.97	16.94	16.19	14.78
$\propto_8$								42.39	34.28	28.88	25.34	22.67	20.62	17.74	16.13
$\propto_9$									43.20	35.12	30.01	26.76	23.54	22.30	20.03
$\propto_{10}$										43.50	35.80	31.71	27.83	24.22	22.58
$\propto_{11}$											43.10	36.55	31.72	28.74	25.93
$\propto_{12}$												43.46	36.94	32.26	29.26
$\propto_{13}$													43.53	37.44	33.05
$\propto_{14}$														43.41	37.73
$\propto_{15}$															43.18
%THD	29.78	8.80	5.31	4.70	3.66	2.31	2.71	1.79	1.76	1.31	1.06	1.01	0.95	1.00	1.08

Table 5-3: Optimum SHE Switching Angles for Different Inverter Levels (M_i =0.90) solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	29.69	9.03	5.09	3.29	3.67	4.19	1.52	2.74	2.79	1.23	2.70	0.94	0.64	1.22	1.69
$\propto_2$		26.82	16.92	13.24	8.79	8.25	8.48	6.10	4.67	4.65	3.56	4.63	4.15	3.20	2.95
$\propto_3$			35.71	23.14	19.89	13.08	10.46	9.80	9.44	9.47	8.00	6.51	6.40	6.71	5.54
$\propto_4$				39.36	25.81	23.89	18.63	16.32	13.23	10.56	10.29	9.80	8.53	7.74	8.32
$\propto_5$					41.92	28.32	24.21	20.89	18.65	16.28	15.02	13.04	12.91	11.17	9.43
$\propto_6$						43.14	32.32	27.07	23.07	20.37	18.24	17.02	14.93	14.80	13.03
$\propto_7$							42.88	34.55	28.89	24.75	22.38	19.82	18.65	16.52	15.80
$\propto_8$								44.94	35.78	30.61	26.97	23.93	22.03	20.26	18.25
$\propto_9$									45.24	36.34	31.83	28.20	25.42	23.35	21.84
$\propto_{10}$										45.11	38.32	32.77	29.87	26.80	24.05
$\propto_{11}$											46.82	39.04	34.25	31.10	28.32
$\propto_{12}$												47.21	40.53	35.14	31.63
$\propto_{13}$													48.39	41.30	36.08
$\propto_{14}$														48.83	41.46
$\propto_{15}$															47.86
%THD	29.78	8.83	5.28	4.70	3.45	2.85	2.97	1.68	1.34	0.99	0.96	0.74	0.63	0.64	0.45

Table 5-4: Optimum SHE Switching Angles for Different Inverter Levels (M_i = 0.85) Solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	29.71	5.62	5.47	5.40	4.41	5.56	5.90	4.34	4.41	3.33	3.46	2.70	2.68	2.63	2.79
$\propto_2$		40.31	17.57	12.70	9.65	6.63	8.75	8.29	7.25	7.26	5.92	5.99	5.28	4.80	6.24
$\propto_3$			36.80	23.07	20.41	17.59	15.62	13.81	11.54	10.08	9.65	8.48	8.09	7.72	8.39
$\propto_4$				39.83	28.95	23.63	22.21	18.53	17.38	15.92	13.92	12.50	12.02	11.01	10.14
$\propto_5$					44.58	33.71	28.87	25.53	21.29	19.03	17.63	16.23	14.75	13.77	14.32
$\propto_6$						47.65	40.37	31.96	27.55	24.93	21.97	19.66	18.09	16.93	16.56
$\propto_7$							58.07	42.45	34.34	29.20	26.61	23.69	21.93	20.15	19.40
$\propto_8$								58.65	44.17	36.83	31.83	28.33	25.59	23.58	22.82
$\propto_9$									59.17	46.23	38.85	33.39	30.30	27.37	25.93
$\propto_{10}$										59.62	47.61	39.77	35.01	31.52	30.03
$\propto_{11}$											59.86	48.20	41.37	36.54	34.01
$\propto_{12}$												60.13	49.96	42.70	39.47
$\propto_{13}$													60.09	50.84	46.79
$\propto_{14}$														60.26	57.26
$\propto_{15}$															61.74
%THD	29.74	10.95	5.75	4.87	3.93	3.70	3.01	1.89	1.52	1.18	1.12	0.85	0.81	0.80	0.58

Table 5-5: Optimum SHE Switching Angles for Different Inverter Levels (M_i = 0.80) Solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	29.67	19.79	12.15	9.45	5.84	7.36	4.98	4.68	5.62	4.92	6.39	5.30	5.94	4.10	7.24
$\propto_2$		55.78	32.99	18.81	18.56	11.69	13.58	12.27	10.62	10.08	10.91	9.69	11.44	10.52	8.01
$\propto_3$			59.66	35.31	25.74	23.15	18.67	16.24	15.57	13.72	13.33	12.39	12.82	11.25	13.34
$\propto_4$				58.63	43.22	29.43	26.95	23.74	21.42	18.83	18.93	16.66	18.09	15.97	14.53
$\propto_5$					61.18	45.69	36.47	30.28	26.95	23.36	23.47	20.69	21.52	19.05	18.59
$\propto_6$						61.67	51.19	40.51	35.02	29.34	28.90	24.87	26.12	22.83	21.77
$\propto_7$							63.01	54.06	44.99	36.41	34.97	30.00	30.57	27.12	25.81
$\propto_8$								63.15	57.14	46.33	43.07	35.85	36.52	31.87	29.50
$\propto_9$									62.28	57.23	54.91	44.01	44.01	36.91	34.51
$\propto_{10}$										62.89	60.49	54.76	53.00	43.69	40.47
$\propto_{11}$											62.22	59.91	59.04	52.35	48.02
$\propto_{12}$												62.70	59.61	57.69	56.11
$\propto_{13}$													65.16	60.50	59.13
$\propto_{14}$														65.69	61.06
$\propto_{15}$															63.39
%THD	29.89	11.92	6.67	4.96	4.45	4.04	3.2	2.63	1.76	1.62	1.28	1.04	0.90	0.74	0.69

Table 5-6: Optimum SHE Switching Angles for Different Inverter Levels (M_i =0.75) solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	29.84	22.97	12.33	14.91	9.41	3.44	10.73	9.09	9.08	9.24	9.69	11.48	9.87	11.18	7.37
$\propto_2$		59.07	33.50	32.02	20.60	18.84	18.05	15.25	13.00	14.40	12.63	12.81	12.76	12.62	11.85
$\propto_3$			59.83	52.33	33.00	29.10	25.74	21.60	20.02	19.25	18.23	18.71	17.92	18.02	16.22
$\propto_4$				64.79	51.08	42.21	36.52	29.76	24.93	25.11	22.59	23.28	21.03	21.95	19.48
$\propto_5$					64.51	51.72	51.69	39.32	32.85	31.35	29.60	28.86	25.88	25.57	23.79
$\propto_6$						71.21	59.45	52.84	43.14	40.62	35.26	34.86	31.29	30.60	28.55
$\propto_7$							64.20	59.70	55.56	51.91	43.40	42.85	37.72	36.59	32.94
$\propto_8$								64.14	59.44	57.40	54.28	52.92	45.52	43.79	38.47
$\propto_9$									63.92	60.96	57.84	55.31	53.77	52.71	45.04
$\propto_{10}$										65.26	61.82	59.34	56.84	54.45	50.15
$\propto_{11}$											64.25	63.32	59.13	57.76	55.40
$\propto_{12}$												66.54	64.29	60.93	58.18
$\propto_{13}$													64.58	63.70	61.32
$\propto_{14}$														66.68	63.98
$\propto_{15}$															70.22
%THD	29.79	12.00	6.87	5.65	5.00	4.11	3.69	2.72	1.96	1.74	1.33	1.17	0.98	0.84	0.74

Table 5-7: Optimum SHE Switching Angles for Different Inverter Levels (M_i =0.70) Solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	30.08	23.49	13.73	16.35	20.96	7.86	14.32	14.06	14.36	14.99	14.21	13.03	5.67	13.89	12.91
$\propto_2$		59.49	37.28	29.05	36.79	28.35	22.51	21.77	21.31	20.97	20.25	18.51	16.23	18.22	17.60
$\propto_3$			61.90	55.43	51.68	40.04	32.87	30.06	28.87	27.02	25.47	23.34	20.96	22.99	21.04
$\propto_4$				60.63	58.43	47.13	46.80	42.20	37.97	35.38	32.50	30.07	25.48	27.87	25.77
$\propto_5$					68.67	61.82	55.95	52.21	48.42	45.98	41.25	36.13	31.08	33.48	30.55
$\propto_6$						77.42	60.08	57.19	54.34	52.56	49.57	45.01	37.98	39.21	35.99
$\propto_7$							68.02	61.79	58.34	55.12	52.92	51.22	45.40	47.01	43.38
$\propto_8$								68.53	63.69	60.15	57.12	55.02	48.85	51.62	49.29
$\propto_9$									68.89	64.89	61.14	57.00	52.93	53.26	52.17
$\propto_{10}$										69.19	65.00	63.33	59.07	57.16	54.60
$\propto_{11}$											69.86	64.20	61.18	59.71	58.07
$\propto_{12}$												70.67	68.31	63.53	60.15
$\propto_{13}$													72.90	66.10	64.55
$\propto_{14}$														70.40	66.00
$\propto_{15}$															70.11
%THD	30.06	12.09	8.31	6.43	6.17	4.26	3.76	2.97	2.23	1.92	1.42	1.58	1.03	0.94	0.82

Table 5-8: Optimum SHE Switching Angles for Different Inverter Levels (M_i = 0.65) Solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	30.56	23.84	23.36	16.85	22.46	18.38	10.92	20.02	19.53	17.95	19.85	18.36	17.43	18.29	18.23
$\propto_2$		59.89	50.04	37.22	39.51	30.62	27.87	29.31	27.85	24.66	25.78	24.32	22.53	23.34	22.64
$\propto_3$			64.50	53.86	52.43	45.17	38.68	41.41	38.01	32.75	33.09	30.10	28.30	28.96	27.53
$\propto_4$				67.14	59.70	55.28	45.23	48.47	46.46	42.68	42.26	38.25	34.76	34.83	33.38
$\propto_5$					71.20	60.37	58.02	53.87	51.04	49.54	47.37	46.31	42.66	41.82	39.95
$\propto_6$						70.09	61.71	59.65	55.99	52.48	51.08	48.22	48.01	47.05	45.55
$\propto_7$							77.56	65.87	61.72	57.94	54.97	53.69	50.49	48.74	47.70
$\propto_8$								72.66	66.69	62.10	59.87	55.66	54.33	52.85	50.99
$\propto_9$									73.28	66.96	62.98	60.90	57.75	55.55	54.05
$\propto_{10}$										72.66	68.74	64.10	61.21	59.24	56.84
$\propto_{11}$											73.33	68.16	65.15	62.51	60.43
$\propto_{12}$												73.10	68.85	66.33	63.01
$\propto_{13}$													73.45	70.20	66.85
$\propto_{14}$														73.85	70.08
$\propto_{15}$															74.09
%THD	30.19	12.25	8.79	6.58	6.97	5.07	3.83	3.10	2.66	2.25	1.76	1.74	1.09	0.99	0.83

Table 5-9: Optimum SHE Switching Angles for Different Inverter Levels (M_i = 0.60) Solved by GA

No. of Levels	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	31.10	43.62	33.22	35.11	28.23	21.85	26.63	26.27	22.16	26.78	20.64	24.36	25.13	24.22	23.34
$\propto_2$		64.20	54.65	47.84	46.25	36.53	39.45	37.53	31.07	36.35	28.38	30.73	31.67	29.68	28.85
$\propto_3$			66.75	59.92	50.43	48.10	46.14	45.10	41.61	41.60	36.48	38.31	38.62	36.99	34.74
$\propto_4$				75.15	64.09	55.94	52.88	48.92	47.06	46.13	43.64	43.76	41.85	41.37	40.95
$\propto_5$					73.12	62.45	59.90	56.99	52.02	50.32	48.29	46.69	46.06	44.45	43.02
$\propto_6$						73.07	67.71	61.52	57.20	56.17	51.29	51.90	49.24	47.76	47.42
$\propto_7$							76.07	69.58	62.71	60.16	56.76	53.93	53.04	51.10	48.65
$\propto_8$								76.24	68.61	66.17	59.95	59.31	56.56	55.09	53.44
$\propto_9$									75.13	71.64	65.60	62.85	60.64	57.95	55.69
$\propto_{10}$										78.17	69.90	67.83	64.67	62.43	60.76
$\propto_{11}$											75.30	71.86	68.91	64.93	61.19
$\propto_{12}$												77.81	73.28	69.80	66.57
$\propto_{13}$													78.62	73.73	69.82
$\propto_{14}$														78.76	74.19
$\propto_{15}$															78.23
%THD	30.12	17.65	10.42	7.27	6.60	5.61	3.87	3.18	2.86	2.43	1.80	1. 91	1.12	1.02	0.88

Table 5-10: Optimum SHE Switching Angles for Different Inverter Levels (M_i = 0.55) Solved by GA

No. of Level	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	31.82	43.49	35.16	33.24	34.44	29.77	30.57	32.23	32.48	32.86	27.12	27.33	29.20	29.49	31.18
$\propto_2$		64.19	54.36	49.08	44.84	43.04	41.56	39.53	37.98	36.96	35.50	35.14	36.06	36.12	35.60
$\propto_3$			68.80	58.90	54.29	48.21	45.50	44.82	43.57	42.69	41.39	40.80	39.35	37.87	37.49
$\propto_4$				75.00	64.96	58.28	54.73	51.74	48.92	46.85	44.28	42.58	43.56	42.30	41.52
$\propto_5$					77.29	66.23	60.85	57.71	54.86	52.25	49.65	48.43	47.15	45.48	44.39
$\propto_6$						77.01	69.90	65.13	60.80	57.85	53.56	51.10	50.55	48.85	48.29
$\propto_7$							78.71	72.40	67.35	62.98	58.71	56.22	54.56	52.88	51.55
$\propto_8$								81.38	74.23	69.41	63.28	60.20	57.99	56.27	55.12
$\propto_9$									82.52	75.41	68.53	65.28	63.36	60.56	58.58
$\propto_{10}$										83.22	74.10	69.73	67.13	64.15	62.13
$\propto_{11}$											80.38	75.32	71.55	68.87	66.01
$\propto_{12}$												80.41	76.42	73.11	70.20
$\propto_{13}$													82.32	77.95	74.73
$\propto_{14}$														83.14	79.74
$\propto_{15}$															84.78
%THD	29.82	17.57	10.89	8.95	6.59	5.69	4.92	3.81	2.90	2.66	1.92	1.88	1.22	1.05	0.93

Table 5-11: Optimum SHE Switching Angles for Different Inverter Levels (M_i = 0. 50) Solved by GA

No. of Level	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
$\propto_1$	32.6	42.06	39.34	36.44	35.77	37.34	34.59	34.14	33.29	31.73	32.32	32.58	32.43	31.78	32.60
$\propto_2$		77.68	56.22	48.27	45.56	39.45	39.99	38.48	38.45	38.36	37.45	36.58	35.68	35.94	35.02
$\propto_3$			80.02	62.23	57.32	52.63	48.99	46.58	44.26	42.56	42.12	41.11	40.36	39.33	39.04
$\propto_4$				78.31	69.65	59.48	55.71	51.96	50.55	48.66	47.41	45.66	43.56	43.55	42.18
$\propto_5$					85.19	71.39	64.88	59.86	56.53	53.76	52.22	50.29	48.18	47.06	46.28
$\propto_6$						82.41	73.63	66.94	63.06	59.89	58.25	55.05	52.18	51.15	49.10
$\propto_7$							85.15	75.66	70.00	65.46	62.64	59.73	56.72	55.38	53.50
$\propto_8$								85.75	78.06	72.41	68.98	65.03	60.82	59.60	56.59
$\propto_9$									87.18	79.79	75.39	70.34	65.55	63.81	61.07
$\propto_{10}$										88.59	82.79	76.33	70.56	68.62	65.01
$\propto_{11}$											89.60	83.45	76.21	73.45	69.19
$\propto_{12}$												89.49	82.00	78.83	73.61
$\propto_{13}$													88.37	84.93	78.75
$\propto_{14}$														89.99	84.63
$\propto_{15}$															89.56
%THD	29.55	17.31	11.63	9.51	7.51	6.51	5.40	3.91	2.95	2.78	1.91	1.52	0.90	1.03	0.94

5.3 Simulation Modelling Results for CHB-MLI Using the SHE Control

In order to validate the results of the optimal switching angles, the output voltage waveforms for different levels of inverters (3–31) were modelled and simulated. The value of the modulation index was selected as 0.9 for the simulation. The three-phase line-to-line voltage waveforms and the associated harmonic profile are demonstrated in Figures 5.4 to 5.18 for CHB-MLI at levels (3–31). The output voltage is given in per-unit (pu) values in order to ensure that the simulation is generic. The modelling of these CHB-MLI circuits will be used in the evaluation %THD, conduction and switching power losses, which are considered the key measure values in the optimisation of the trade-off model. Furthermore, the Simulink models of different levels of inverter circuits are used for the optimisation of the trade-off model.

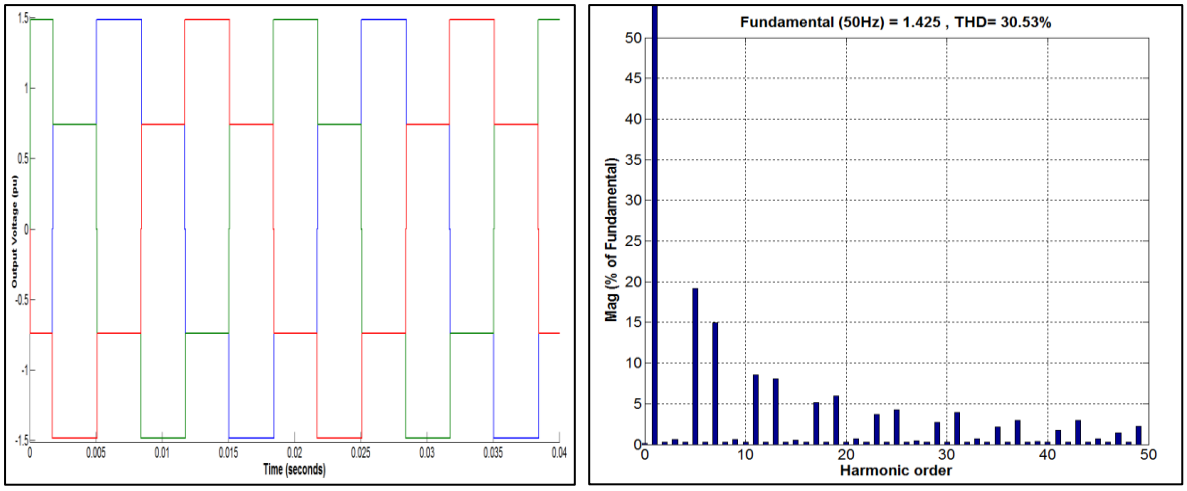


Figure 5.4: Simulated three-phase output voltage and harmonic distortion analysis for three-level CHB-MLI

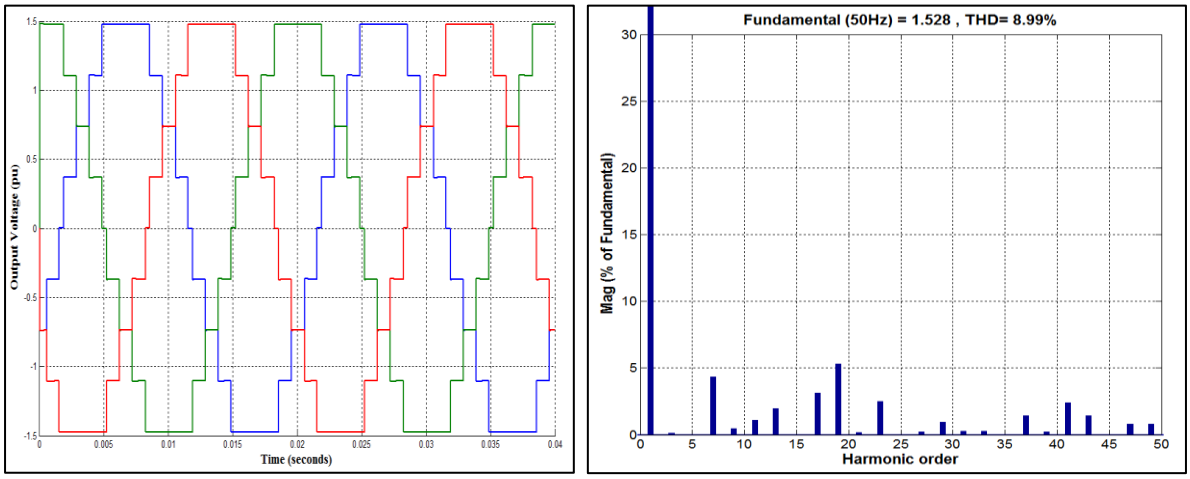


Figure 5.5: Simulated three-phase output voltage and harmonic distortion analysis for five-level CHB-MLI

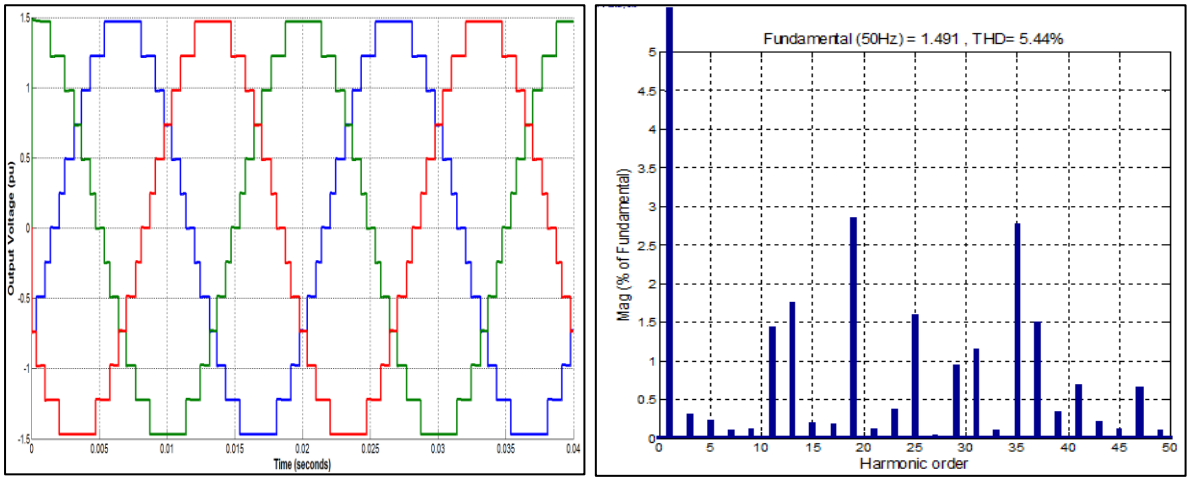


Figure 5.6: Simulated three-phase output voltage and harmonic distortion analysis for seven-level CHB-MLI

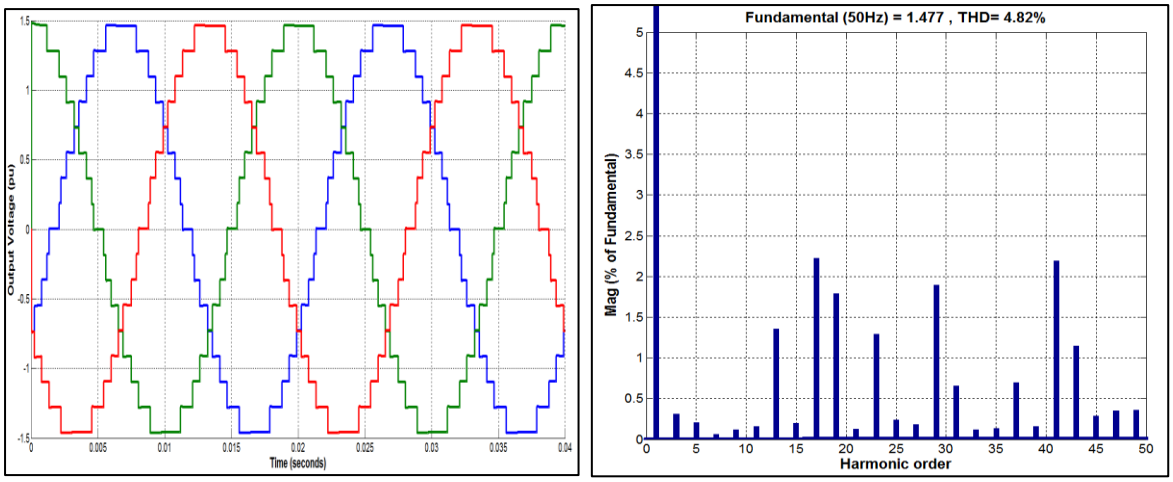


Figure 5.7: Simulated three-phase output voltage and harmonic distortion analysis for nine-level CHB-MLI

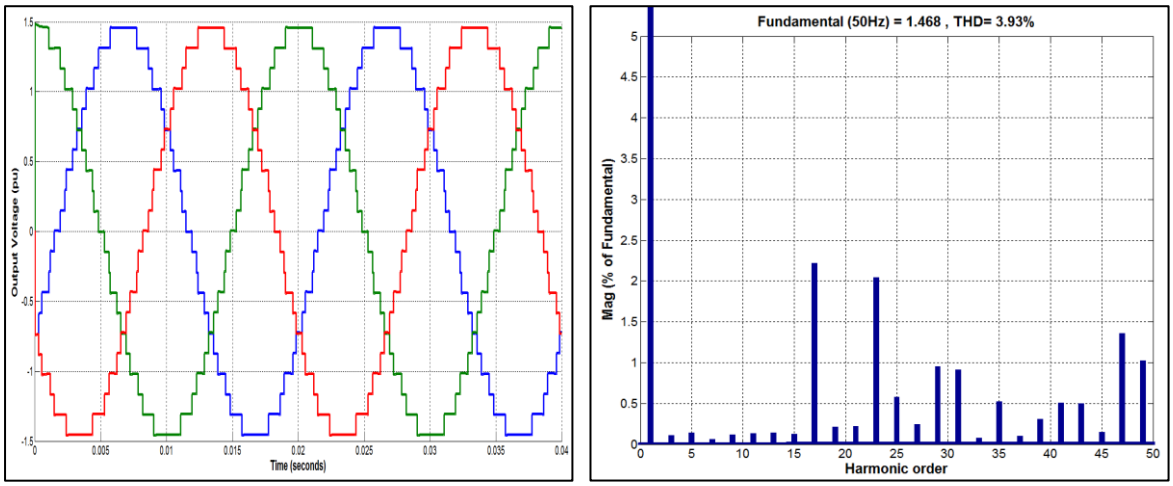


Figure 5.8: Simulated three-phase output voltage and harmonic distortion analysis for 11-level CHB-MLI

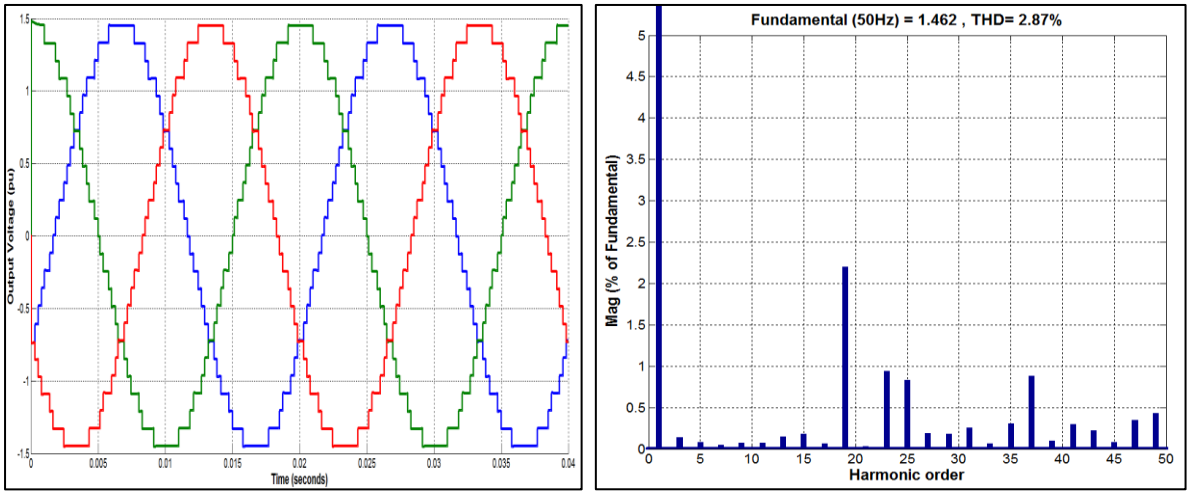


Figure 5.9: Simulated three-phase output voltage and harmonic distortion analysis for 13-level CHB-MLI

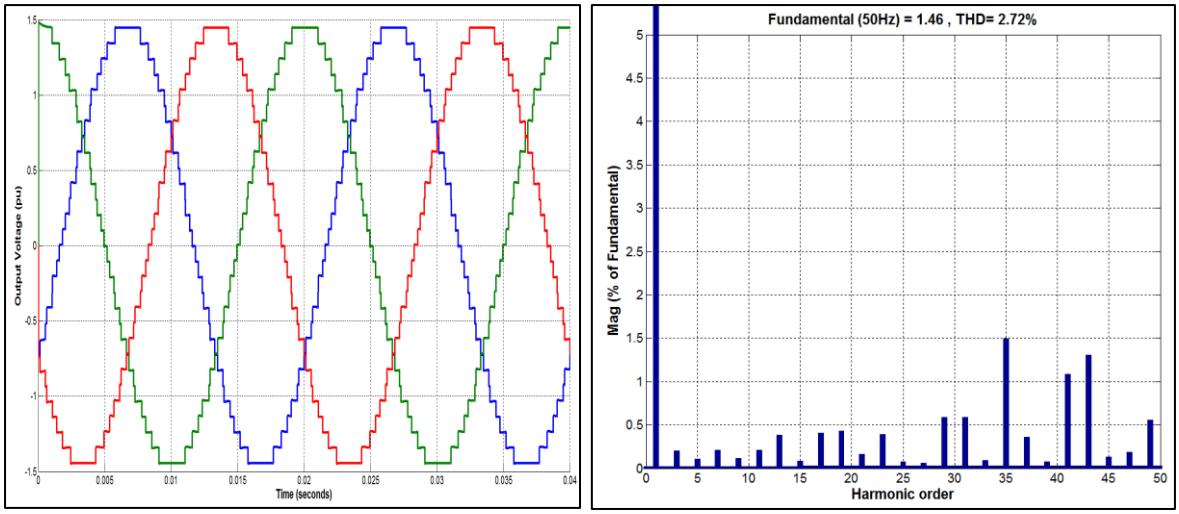


Figure 5.10: Simulated three-phase output voltage and harmonic distortion analysis for 15-level CHB-MLI

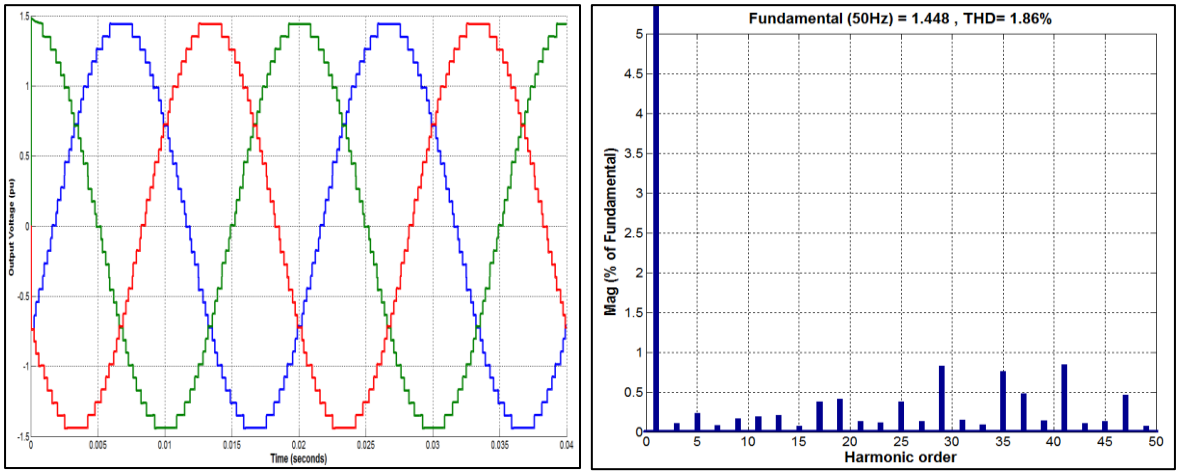


Figure 5.11: Simulated three-phase output voltage and harmonic distortion analysis for 17-level CHB-MLI

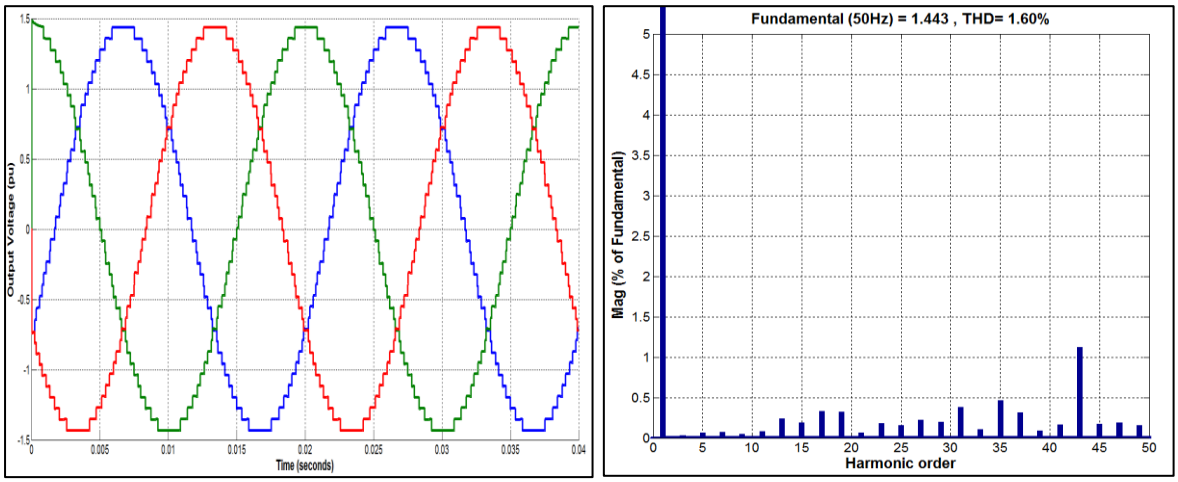


Figure 5.12: Simulated three-phase output voltage and harmonic distortion analysis for 19-level CHB-MLI

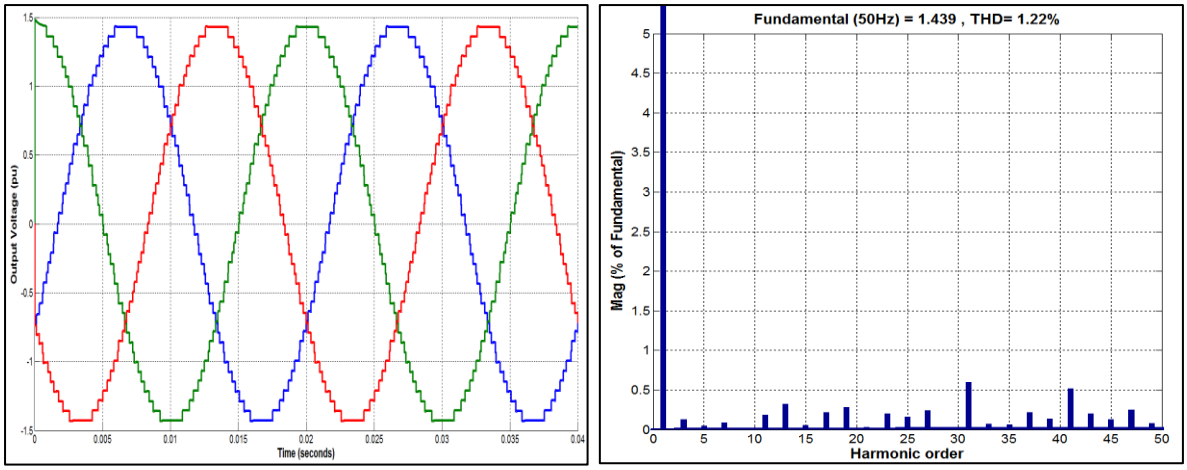


Figure 5.13: Simulated three-phase output voltage and harmonic distortion analysis for 21-level CHB-MLI

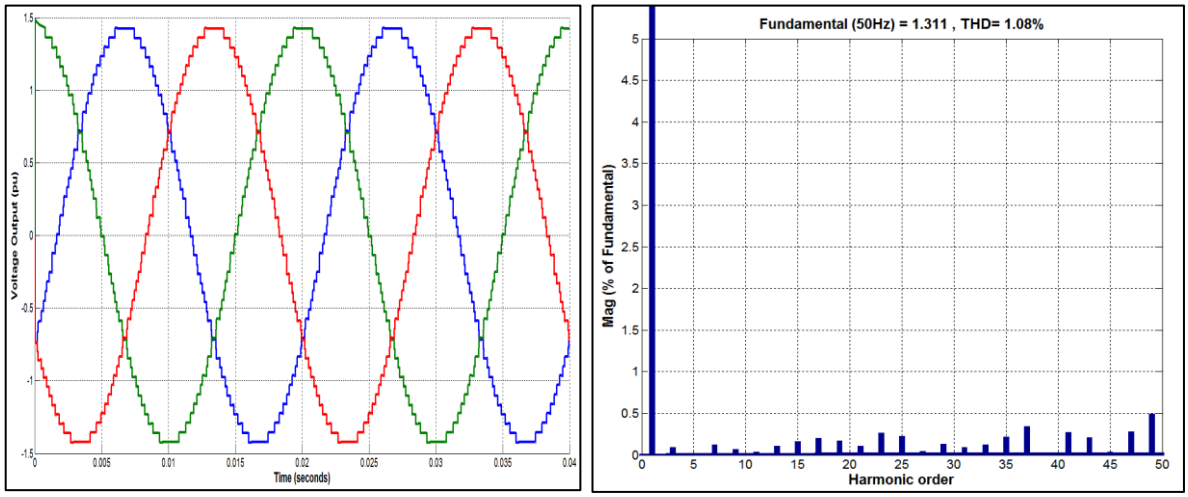


Figure 5.14: Simulated three-phase output voltage and harmonic distortion analysis for 23-level CHB-MLI

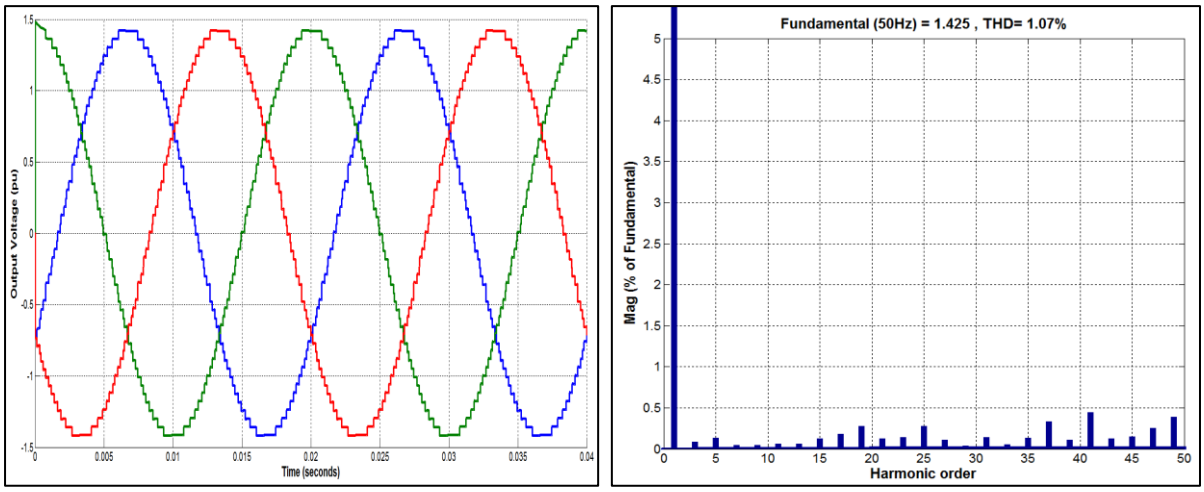


Figure 5.15: Simulated three-phase output voltage and harmonic distortion analysis for 25-level CHB-MLI

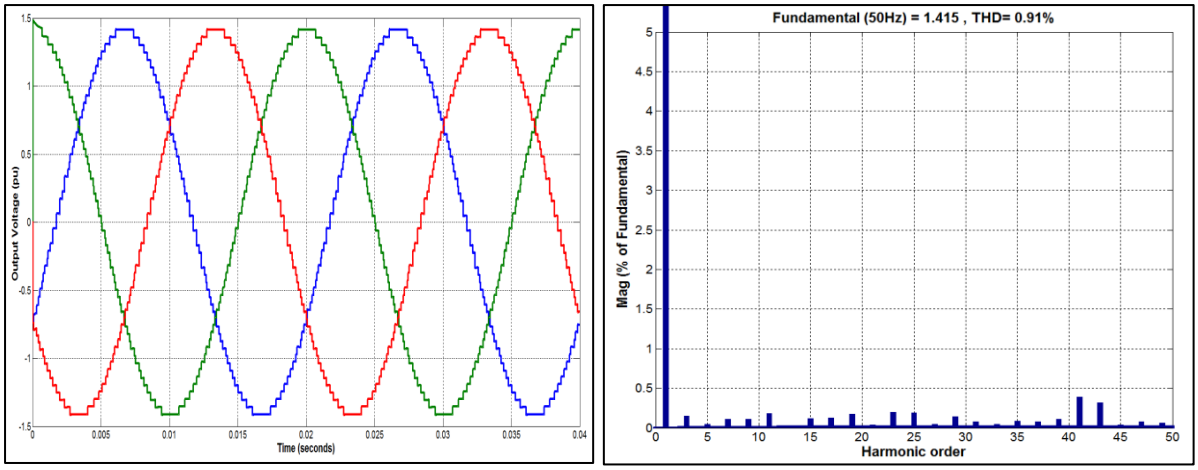


Figure 5.16: Simulated three-phase output voltage and harmonic distortion analysis for 27-level CHB-MLI

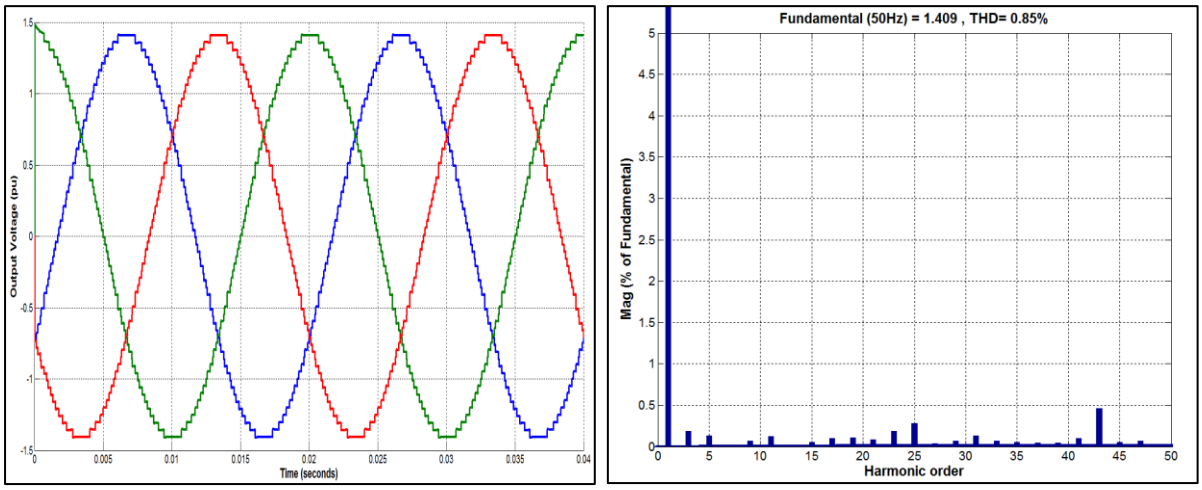


Figure 5.17: Simulated three-phase output voltage and harmonic distortion analysis for 29-level CHB-MLI

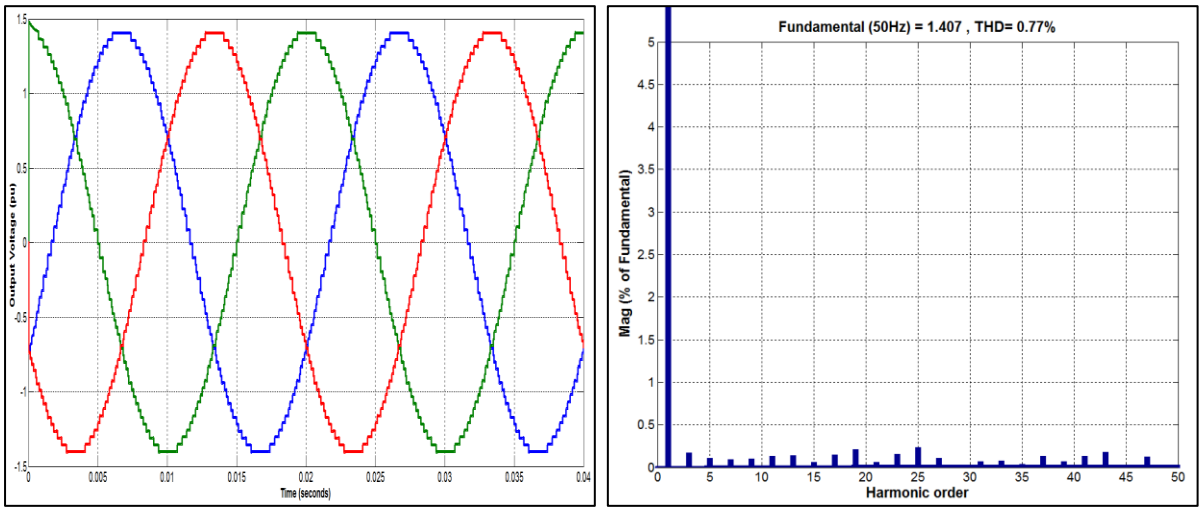


Figure 5.18: Simulated three-phase output voltage and harmonic distortion analysis for 31-level CHB-MLI

5.4 Simulation Modelling Results for CHB-MLI Using the SPWM Control

For the purpose of the comparison study, the author modelled different CHB-MLI circuits that are controlled by high frequency SPWM. The simulated levels were from (3–31). Different SPWM level-shifting controls were applied. These models were used to investigate the THD and the power loss. Figures 5.19 to 5.21 demonstrate the three-phase voltage for the simulated CHB-MLI circuits at different levels. Different switching frequencies and different SPWM controls are shown.

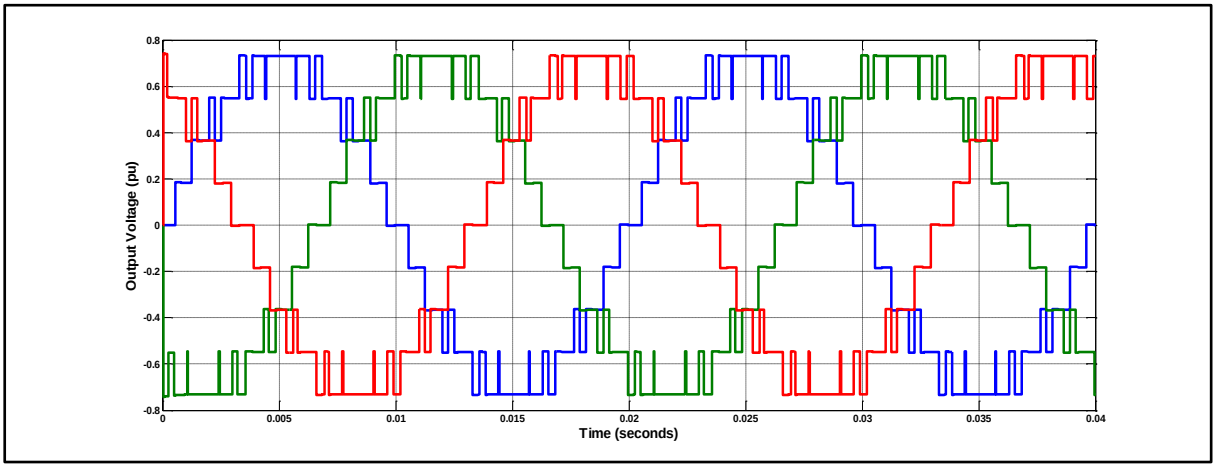


Figure 5.19: Output voltage for nine-level CHB-MLI controlled by PD-SPWM at switching frequency 1500 Hz

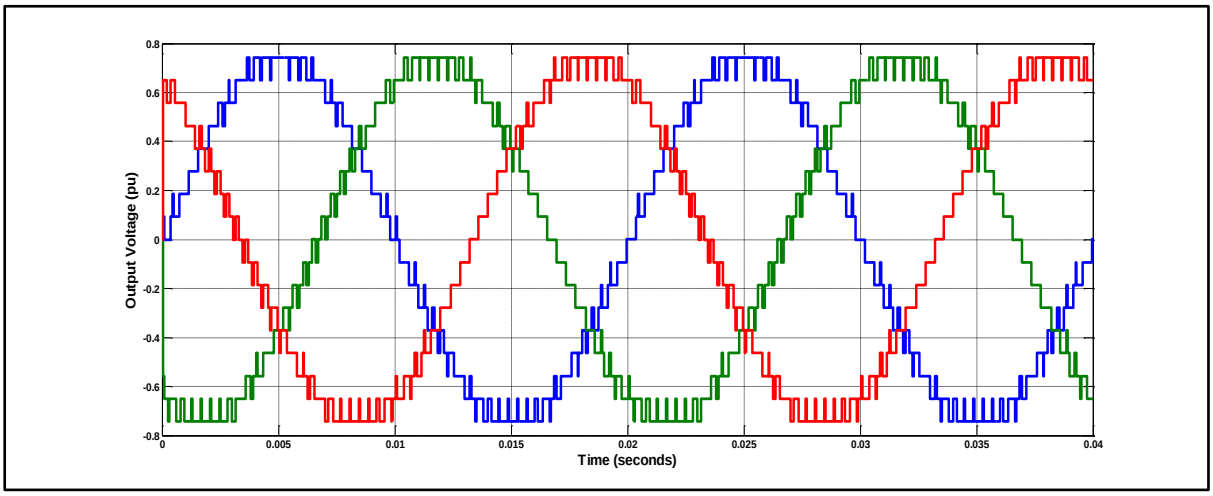


Figure 5.20: Output voltage for 17-level CHB-MLI controlled by POD-SPWM at switching frequency 2500 Hz

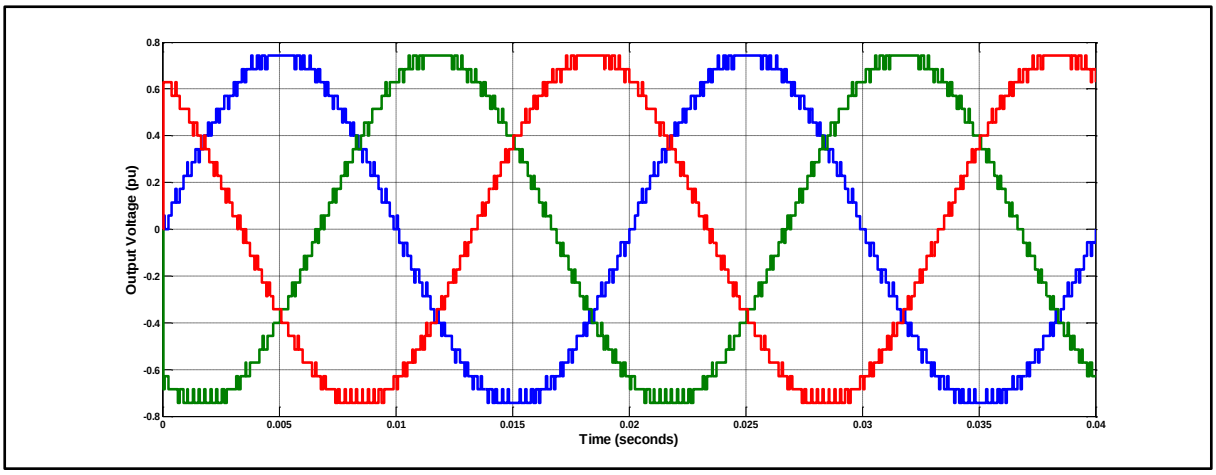


Figure 5.21: Output voltage for 27-level CHB-MLI controlled by APOD-SPWM at switching frequency 4000 Hz

5.5 THD Comparison Study of SHE and SPWM Control

The output THD is a very important index factor that is used to measure the harmonic distortion in an electrical signal. In this section, THD for different inverter levels (3–31) are analysed. In this analysis, SHE and SPWM are applied to control the inverter, as these techniques are considered the most widely used in the industry. The objective of this investigation is to study the effects of increased inverter levels on the value of THD using different control methods.

Figure 5.22 shows the %THD versus the number of inverter level in the case of the SHE control applied. The %THD was found to decrease as the number of levels increased. However, the reduction was saturated when the number of levels was above 21. In Figure 5.22, the red dashed line indicates the recommended limit of 5% according to the IEEE-519 standard.

Figure 5.23 presents an important and interesting comparison of %THD versus the number of inverter levels for CHB-MLI implementing SHE and for those implementing SPWM control. In this comparison, the multicarrier switching frequency for SPWM control was 2.5 kHz. The comparison showed that SHE controlled inverters had lower %THD profile compared to those controlled with SPWM.

In a further investigation, the CHB-MLI was simulated when applying different SPWM controls at the different switching frequencies of 1 kHz, 2.5 kHz, 3 kHz and 4 kHz. The results of this investigation are demonstrated in Figures 5.24 to 5.26, which show that at low

number of inverter levels, a better harmonic distortion profile was obtained at a high switching frequency. However, the value of %THD was not reduced considerably when the switching frequency increased at higher numbers of inverter levels.

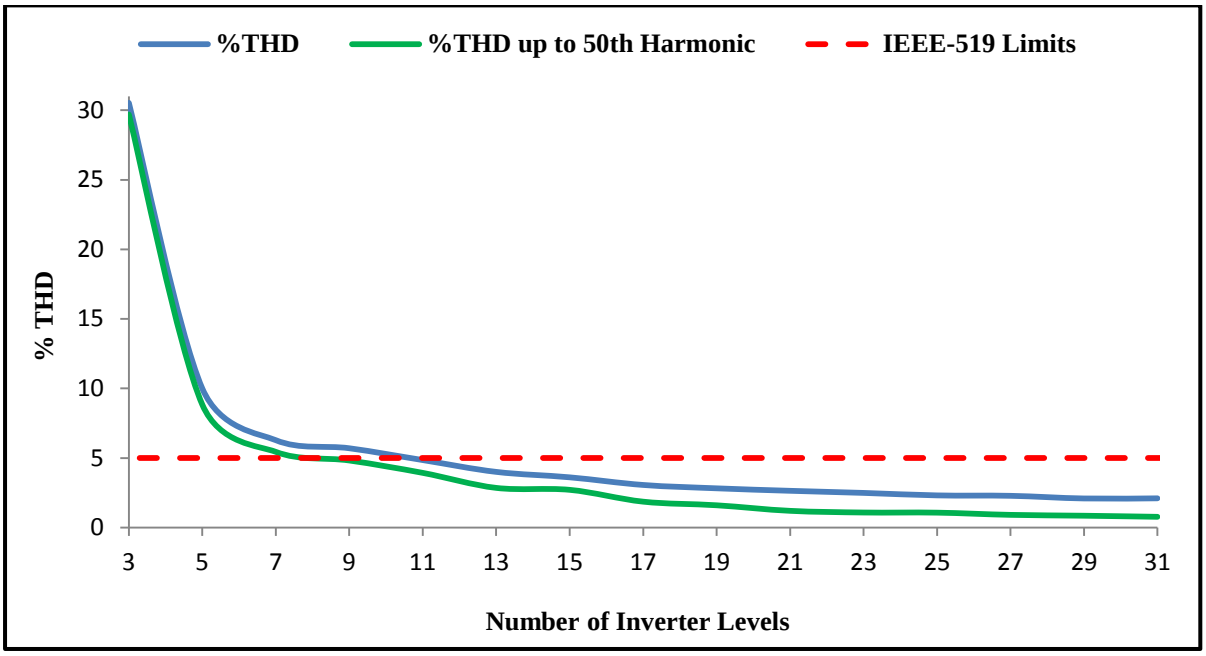


Figure 5.22: Total harmonic distortion versus the number of inverter levels in applying SHE control

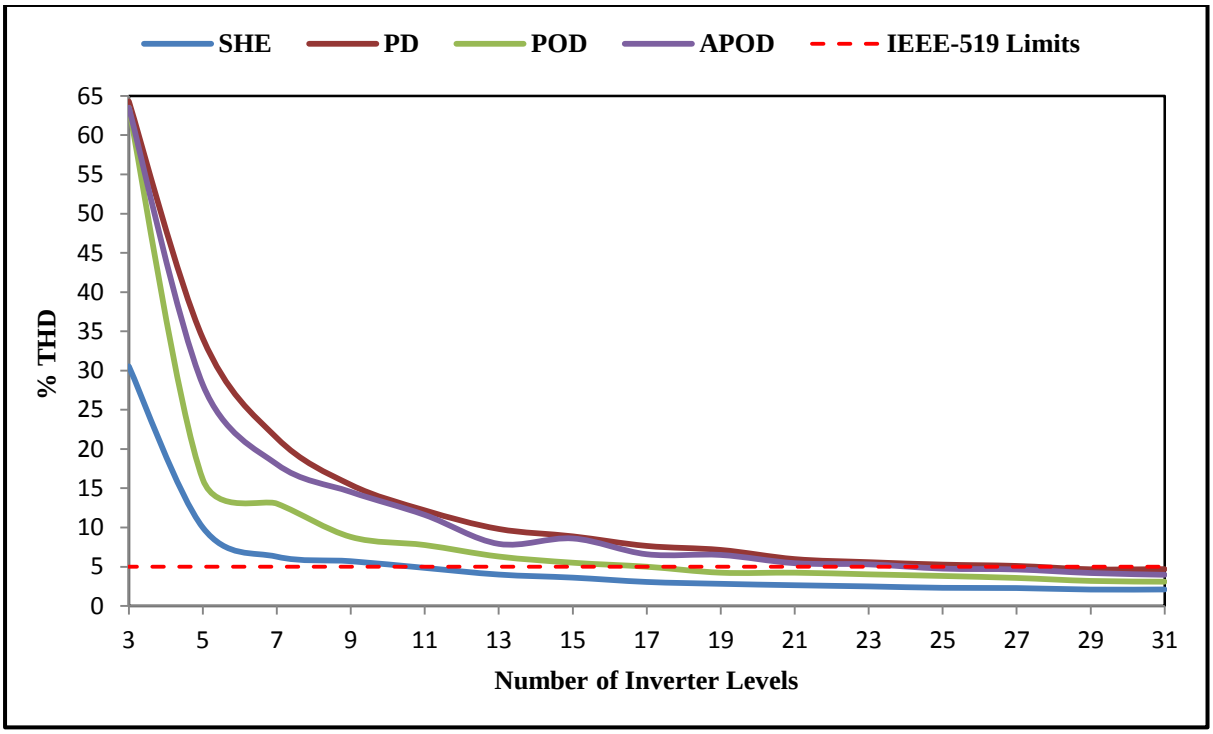


Figure 5.23: Total harmonic distortion versus number of inverter levels in applying different controls

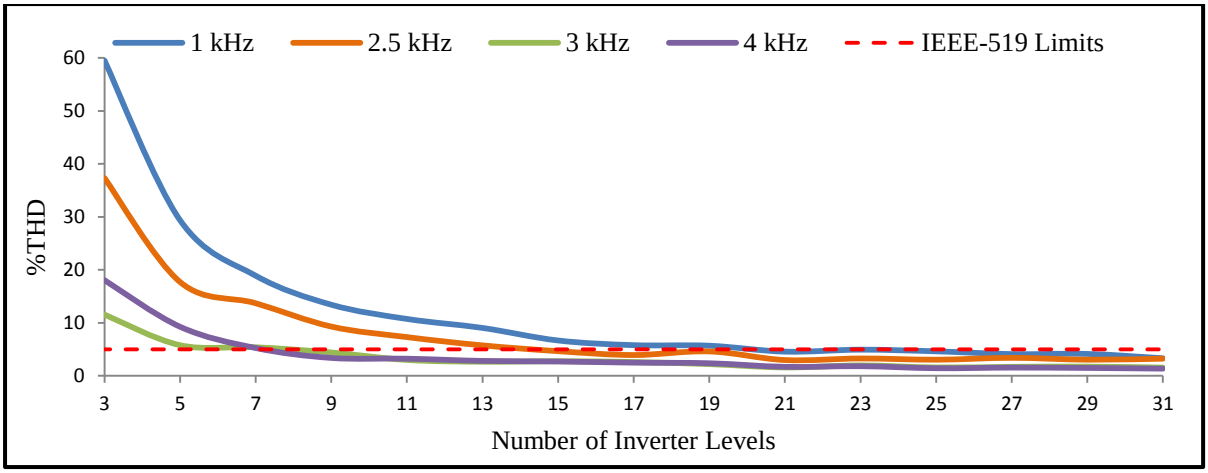


Figure 5.24: THD versus the number of inverter levels controlled by SPWM-PD at different switching frequencies

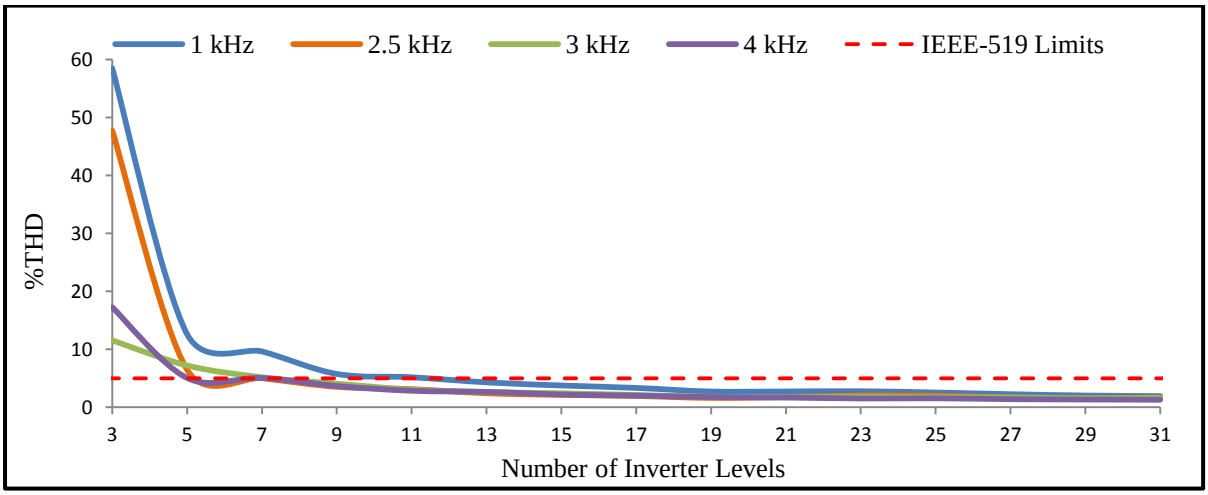


Figure 5.25: THD versus the number of inverter levels controlled by SPWM-POD at different switching frequencies

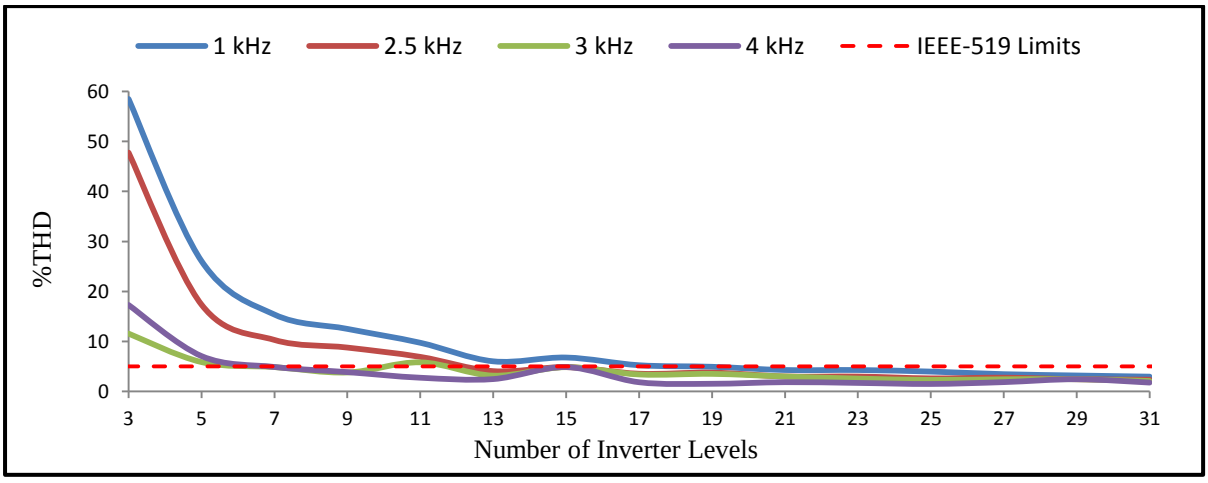


Figure 5.26: THD versus number of inverter levels controlled by SPWM-APOD at different switching frequencies

5.6 Curve Fitting for the Considered IGBT's Data Sheets

As shown in Table 4-5, five IGBT's modules were considered in the analysis. The blocking voltages of these devices were 1.7, 2.5, 3.3, 4.5 and 6.5 kV. Based on the proposed model for power loss, which was explained in Chapter 4, the power losses of conduction and switching in multilevel inverters are calculated based on the actual data sheets of the considered devices. In this section, the curve fitting tool of Microsoft Excel is applied to generate accurate mathematical equations of the voltage and energy curves for each IGBT. Tables 5-12 to 5-16 show the mathematical equations generated based on the data sheets by applying the curve fitting tool. The data sheet of each device was modelled by five equations. The first two equations represent the on-state voltage of IGBT and the antiparallel diode in terms of current, respectively. The last three equations are for the IGBT on-off switching energy and the switch off energy for the freewheeling diode.

Table 5-12: Curve Fitting Equations for Device IGBT FZ400 R17KE3

$v_{ce} = -1 \times 10^{-6} I_c^2 + 0.0047 I_c + 0.7416$	5.2
$v_D = -2 \times 10^{-6} I_D^2 + 0.0041 I_D + 0.6399$	5.3
$K_{IGBT-on} = 1 \times 10^{-6} I_c^2 - 0.0009 I_c + 0.5207$	5.4
$K_{IGBT-off} = 5 \times 10^{-7} I_c^2 - 0.0007 I_c + 0.5107$	5.5
$K_{Diode-rec} = 6 \times 10^{-7} I_D^2 - 0.0009 I_D + 0.5105$	5.6

Table 5-13: Curve Fitting Equations for Device IGBT CM400DY-50 H

$v_{ce} = -4 \times 10^{-10} I_c^3 - 2 \times 10^{-6} I_c^2 + 0.0062 I_c + 1.3903$	5.7
$v_D = -2 \times 10^{-6} I_D^2 + 0.0058 I_D + 1.0711$	5.8
$K_{IGBT-on} = -4 \times 10^{-8} I_c^3 + 4 \times 10^{-5} I_c^2 - 0.011 I_c + 1.8941$	5.9
$K_{IGBT-off} = 2 \times 10^{-5} I_C^2 - 0.0107 I_C + 2.9087$	5.10
$K_{Diode-rec} = 1 \times 10^{-5} I_D^2 - 0.0067 I_D + 1.4343$	5.11

Table 5-14: Curve Fitting Equations for Device IGBT FZ400 R33KL2C-B5

$v_{ce} = -2 \times 10^{-6} I_c^2 + 0.0073 I_c + 1.1701$	5.12
$v_D = -3 \times 10^{-6} I_D^2 + 0.0061 I_D + 0.7479$	5.13
$K_{IGBT-on} = 8 \times 10^{-6} I_c^2 - 0.0064 I_c + 4.2836$	5.14
$K_{IGBT-off} = 3 \times 10^{-6} I_c^2 - 0.0031 I_c + 2.2269$	5.15
$K_{Diode-rec} = 8 \times 10^{-6} I_D^2 - 0.0098 I_D + 3.8363$	5.16

Table 5-15: Curve Fitting Equations for Device IGBT CM400HB-90 H

$v_{ce} = -1 \times 10^{-6} I_c^2 + 0.0049 I_c + 1.5364$	5.17
$v_D = -3 \times 10^{-6} I_D^2 + 0.0075 I_D + 1.1413$	5.18
$K_{IGBT-on} = -7 \times 10^{-6} I_c^2 + 0.0076 I_c + 3.1898$	5.19
$K_{IGBT-off} = 4 \times 10^{-5} I_c^2 - 0.0374 I_c + 10.382$	5.20
$K_{Diode-rec} = 1 \times 10^{-6} I_D^2 - 0.0018 I_D + 1.1044$	5.21

Table 5-16: Curve Fitting Equations for Device IGBT FZ250 R65KE3

$v_{ce} = -1 \times 10^{-5} I_c^2 + 0.0128 I_c + 1.2882$	5.22
$v_D = -7 \times 10^{-11} I_D^4 + 1 \times 10^{-7} I_D^3 - 5 \times 10^{-5} I_D^2 + 0.016 I_D + 0.7468$	5.23
$K_{IGBT-on} = -4 \times 10^{-7} I_c^3 + 0.0004 I_c^2 - 0.1097 I_c + 16.984$	5.24
$K_{IGBT-off} = 7 \times 10^{-6} I_c^2 - 0.0048 I_c + 6.511$	5.25
$K_{Diode-rec} = -3 \times 10^{-7} I_D^3 + 0.0003 I_D^2 - 0.0944 I_D + 13.37$	5.27

The above equations were validated point-by-point for the sake of accuracy. In the next step, these mathematical equations are implemented in the calculation blocks of conduction and switching power losses. The results of the power loss analysis are presented in the next section.

5.7 Investigation of Power Loss in 11 kV CHB-MLI

Power loss is considered a critically important measurement factor in the performance of any DG's integration system because it has a significant effect on the system's cost and efficiency. The purpose of this section is to investigate the behaviour of power loss in CHB-MLIs featuring different high-voltage IGBT devices. In the case study, the inverter output line-to-line voltage is considered 11 kV. Based on the IGBT blocking voltage, several cascaded H-bridge cells are required to synthesize the required output voltage. Nevertheless, the evaluation of power loss in multilevel inverters is a complicated task. In Chapter 4, the author proposed a generic model for precisely calculating conduction and switching power loss in CHB-MLIs. In this section, the detailed simulation of the proposed power loss model is carried out. The conduction and switching loss are analysed for different levels of CHB-MLIs using SHE as a low frequency control and SPWM as a high frequency control.

5.7.1 Design of 11 kV CHB-MLI using different ratings of IGBTs

The IGBTs considered for the inverter design, based on market availability, had the blocking voltages: 1.7, 2.5, 3.3, 4.5 and 6.5 kV. To ensure their reliability, in practice, the HV-IGBTs are operated at only 50–60% of their blocking voltage capability. Based on the blocking voltage capabilities, the design options for 11 kV CHB-MLI are presented in Table 5-17.

Table 5-17: 11 kV CHB-MLI Design using Different High-Voltage IGBT Devices

Number of levels	IGBT Blocking Voltage (V)	DC Voltage V_{DC} (V)	Device Counts (three-phase)
7	6,500	2,722	36
9	4,500	2,042	48
11	3,300	1,633	60
13	3,300	1,361	72
15	2,500	1,167	84
17	2,500	1,021	96
19	1,700	907	108
21	1,700	817	120

5.7.2 Inverter power losses in the case of SHE control

In a semiconductor device, the power loss of conduction is defined as the loss that occurs while the power device is in the on-state and is conducting current. In contrast, the switching power loss can be defined as the power that dissipates during the turn-on and the turn-off switching of a semiconductor device. In this section, detailed investigations of conduction and switching power losses in CHB-MLI are carried out. The inverter is controlled by low frequency SHE modulation. Figures 5.27 to 5.29 demonstrate the conduction, switching and total power losses for different high-voltage IGBTs at variable load current. While the Mitsubishi 2.5 kV and Infineon 1.7 kV had the worst performances in conduction losses, the Mitsubishi 4.5 kV and Infineon 6.5 kV had minimal conduction losses, as shown in Figure 5.27. However, the opposite results were found for switching losses, as shown in Figure 5.28. The results showed that IGBT devices with higher blocking voltages experienced higher switching losses compared to those with lower blocking voltages.

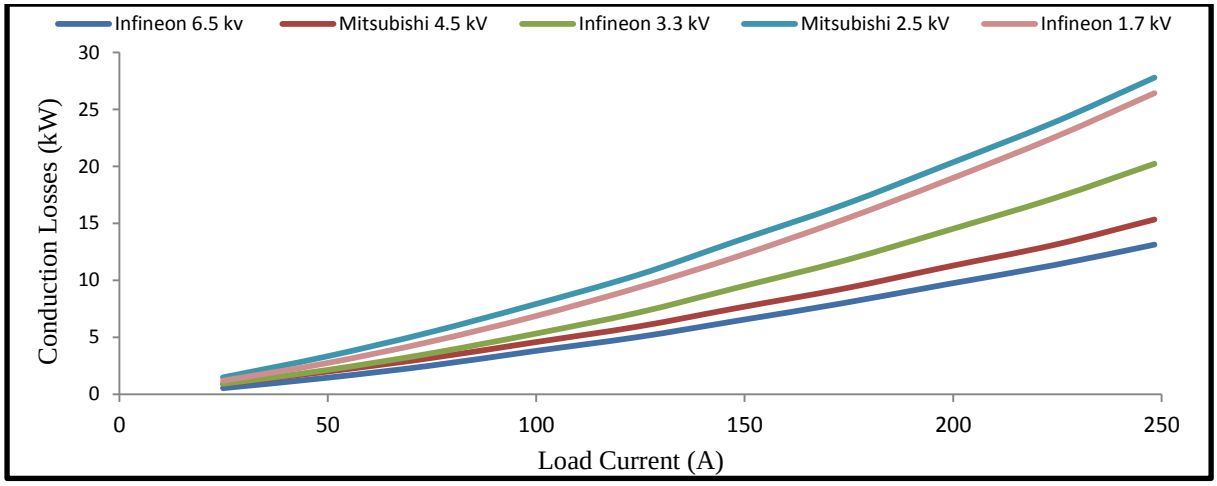


Figure 5.27: Conduction power loss profile for different high-voltage IGBT devices (SHE control)

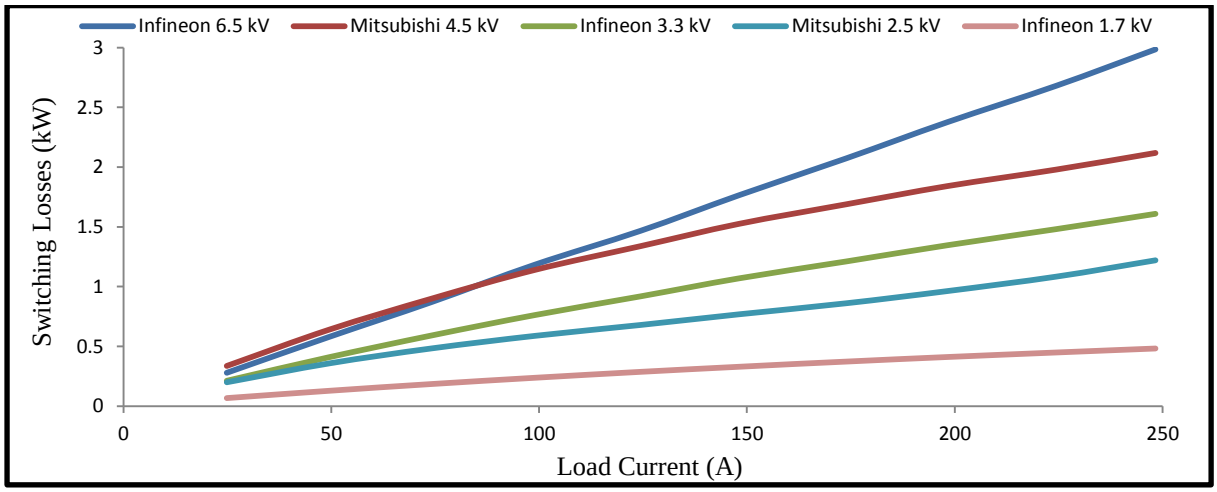


Figure 5.28: Switching power loss profile for different high-voltage IGBT devices (SHE control)

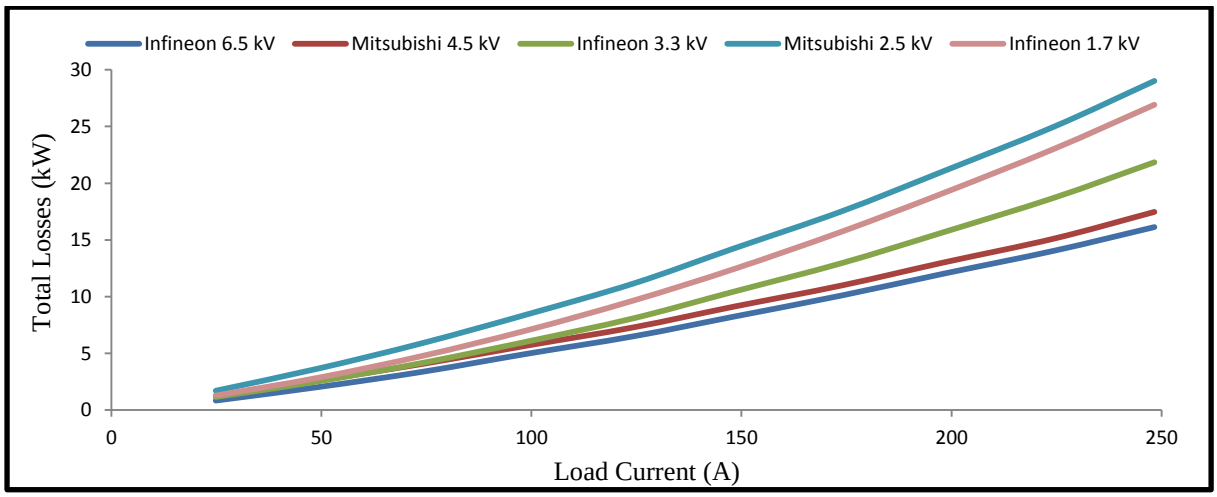


Figure 5.29: Total power loss profile for different high-voltage IGBT devices (SHE control)

A main objective of this power loss investigation was to examine the power loss behaviour in CHB-MLIs with respect to number of inverter levels. Figures 5.30 to 5.32 demonstrate comparisons of conduction, switching and total inverter power losses at different inverter levels.

Figure 5.30 shows that the conduction power loss increased gradually as the number of inverter level increased. This result is justifiable because the number of devices per inverter increased. However, at a high number of inverter levels (i.e., 19 and 21), the conduction loss was found to be reduced compared to the previous levels. The reason for this reduction is that in the 19 and 21 levels, a device with the blocking voltage of 1.7 kV was used. According to the data sheet, this device has the very low power dissipation of almost 50% lower compared to the other power devices used in this study. Therefore, it is experiencing lower conduction power losses, despite of the high number of inverter levels. Based on this result, it can be concluded that in CHB-MLIs controlled by SHE, the conduction power loss depends on the number of devices and the ratings of these devices. Overall, the conduction loss increased as the inverter number of level increased, but this increase was saturated at higher levels.

Figure 5.31 demonstrates the switching power loss versus the number of inverter levels. The figure clearly shows that the switching power loss decreases sharply as the number of levels increases. Hence, despite the increase in the number of devices in CHB-MLI, the switching loss always decreased when the blocking voltage of the switching devices was lower for inverters controlled by SHE at a low-switching modulation.

Figure 5.32 shows the total inverter power loss with respect to the number of inverter levels. The major part of the power loss was through conduction. The reason is that the inverter was controlled at a low frequency in which each power device was conducting for a long time before it was switched off. The total power losses increased as the number of levels increased. Except 19 and 21 levels, it decreased when the implemented device had very low power dissipation.

A further analysis was carried out to investigate the relation between conduction and switching power loss based on the high-voltage IGBTs available in the market. The results of this investigation are illustrated in Figure 5.33. The analysis showed that as the blocking voltage device decreased the contribution of switching power loss was considerably reduced.

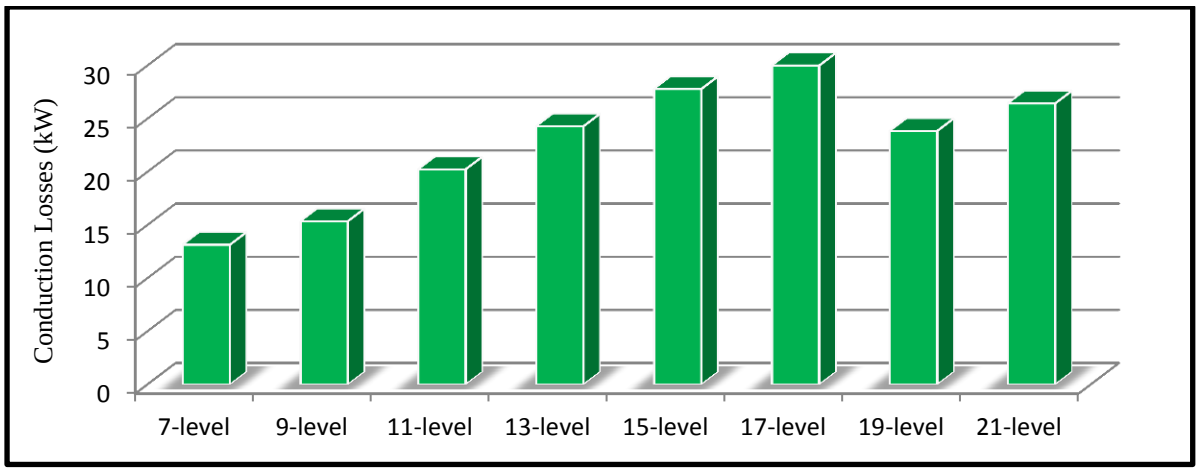


Figure 5.30: Conduction power loss profile for different numbers of inverter levels (SHE control)

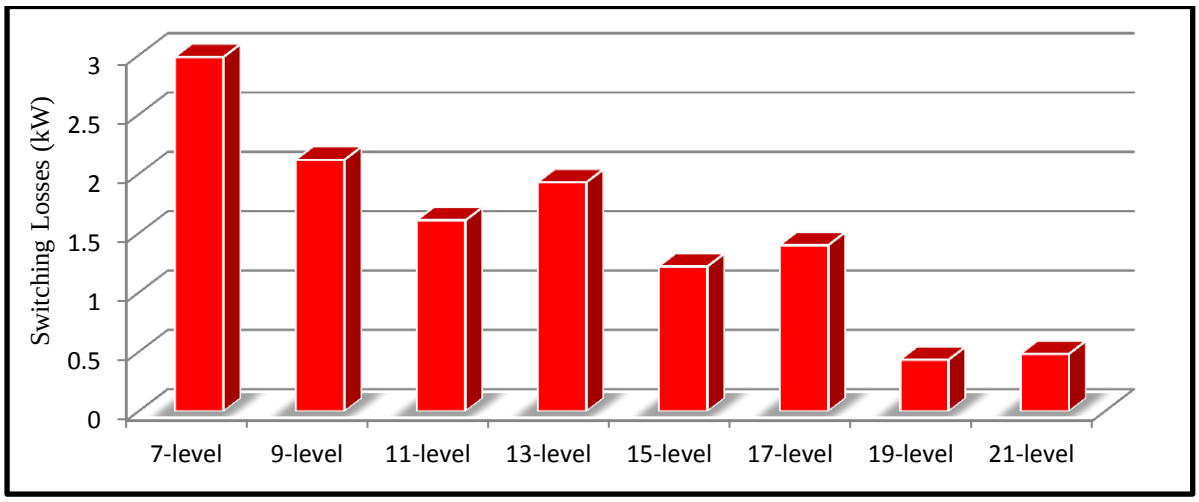


Figure 5.31: Switching power loss profile for different numbers of inverter levels (SHE control)

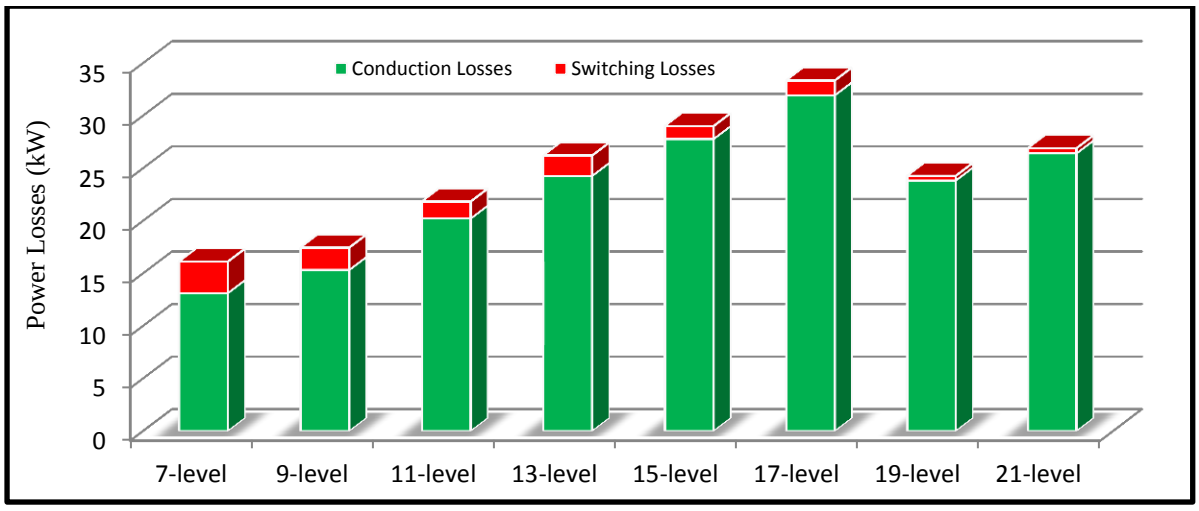
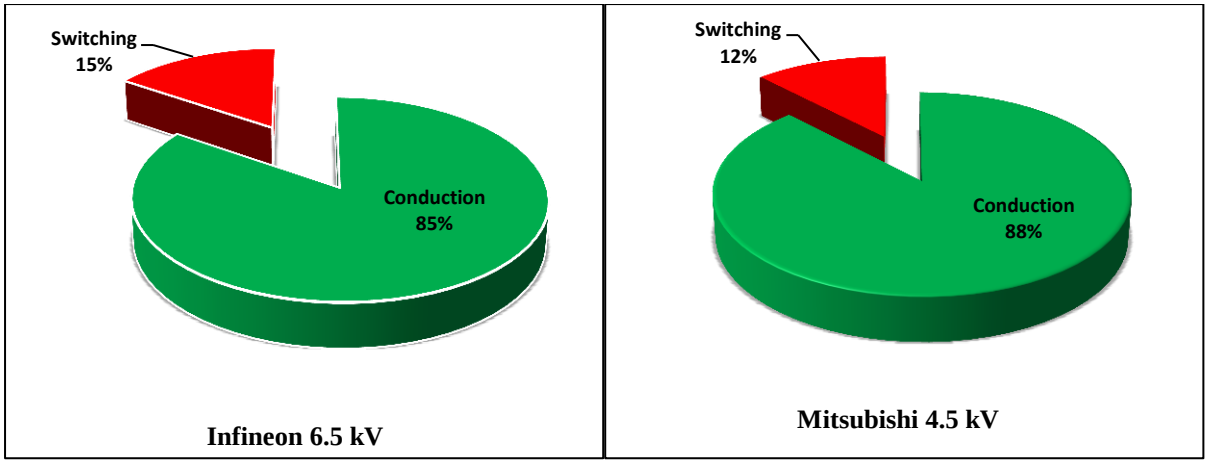
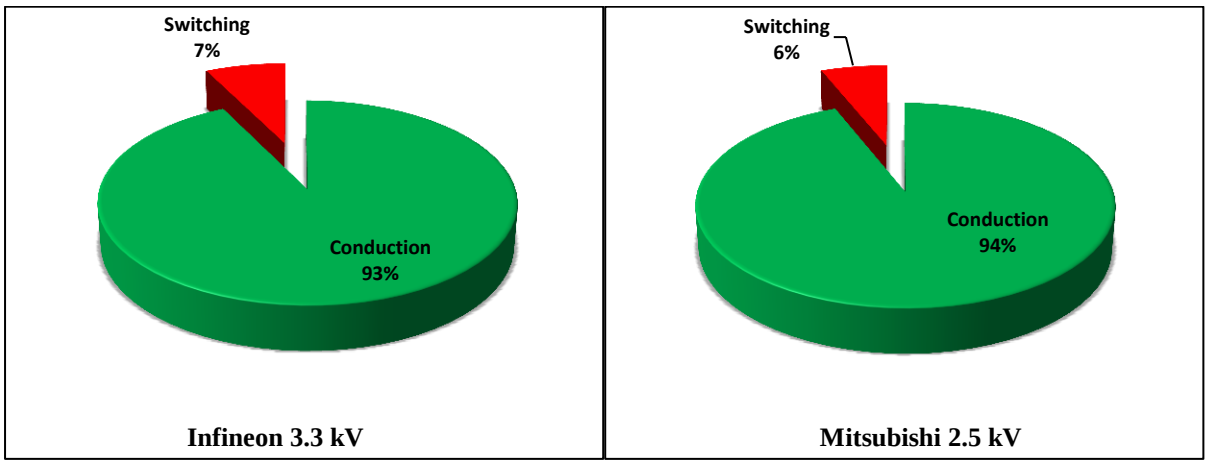


Figure 5.32: Total power loss profile for different numbers of inverter levels (SHE control)



(a) (b)



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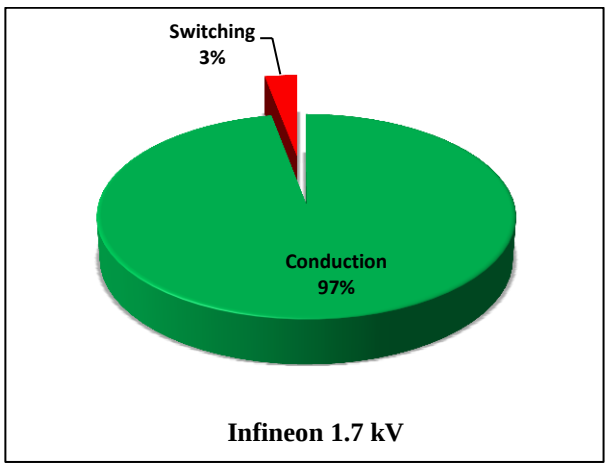


(e)

Figure 5.33: Pie chart showing conduction and switching losses in different high-voltage IGBT devices controlled using SHE (11 kV CHB-MLI) a) FZ400R65KE3 (7-level); b) CM400HB-90H (9-level); c) FZ400R33KL2c-B5 (13-level); d) CM400DY-50H (15-level); e) FZ400R17KE3 (21-level)

5.7.3 Inverter power losses in the case of SPWM control

For the purpose of comparison, a further power loss investigation was carried out to apply SPWM as a high frequency control. The simulation results for conduction, switching and total power losses in the investigated IGBTs at variable load currents are displayed in Figures 5.34 to 5.36. In this investigation, the applied switching frequency was 2500 Hz. The simulation results showed that the power devices Mitsubishi 2.5 kV and Infineon 1.7 kV experienced the highest conduction losses but the lowest switching losses. In contrast, designing the CHB-MLI with the Infineon 6.5 kV and Mitsubishi 4.5 kV power devices reduced the conduction power loss significantly, but the inverter still experienced higher switching power loss compared with the other devices. As shown in Figure 5.36, the total inverter power loss in the IGBT devices with lower blocking voltage ratings was lower compared to the IGBT devices that featured high blocking voltage.

The next step was to investigate the behaviour of power losses with respect to the change in the number of inverter levels at the output voltage. Figure 5.37 depicts the conduction power loss at different inverter levels. The figure shows that generally the conduction power loss increased as the inverter number of levels increased, but it depended on the characteristics of the power switching device.

Similarly, Figure 5.38 presents the changes in switching power loss with respect to the inverter number of levels. Generally, the switching power loss was reduced significantly by increasing the number of levels at the output voltage. The switching power loss in the 21-level inverter was found to be about seven times less than the switching power loss in the seven-level inverter. This result indicates that to reduce switching power loss, the CHB-MLI should be designed with a high number of levels. In this study, the switching power loss was highly proportional to the switching frequency; hence, it contributed substantially to the inverter total power loss, especially in inverters controlled by SPWM. The total power loss in different numbers of inverter levels is demonstrated in Figure 5.39. The switching power loss was found to be dominant except for inverters with high levels. Figure 5.40 shows the percentage share of conduction and switching power loss in different high-voltage IGBT power devices. Based on this result, it could be concluded that in IGBT devices with high blocking voltage, the switching loss is dominant. However, when applying IGBTs with lower blocking voltage, the total losses in conduction and switching were almost equal.

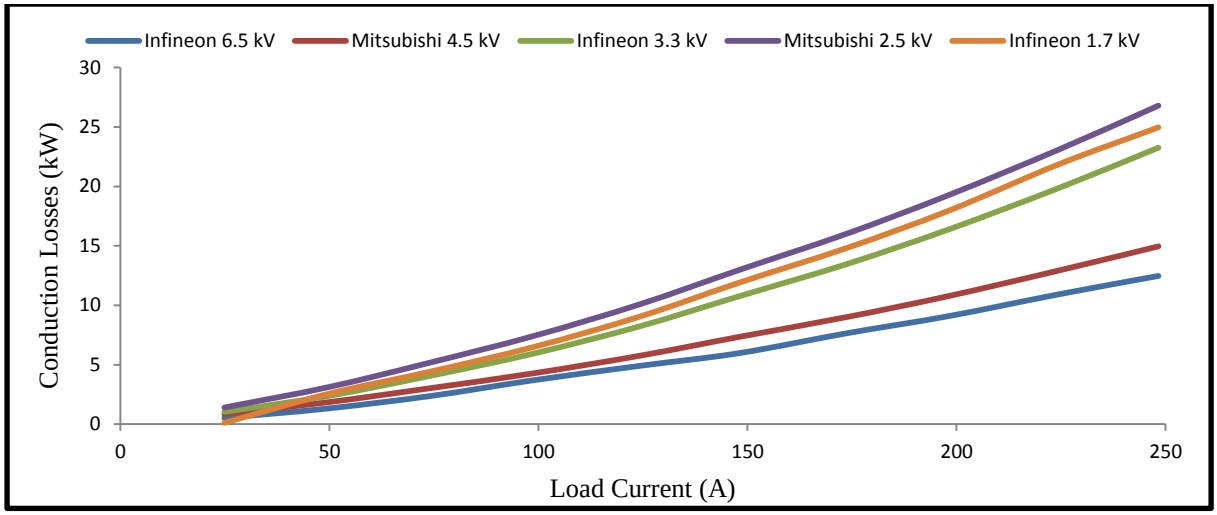


Figure 5.34: Conduction power loss profile for different high-voltage IGBT devices (SPWM control)

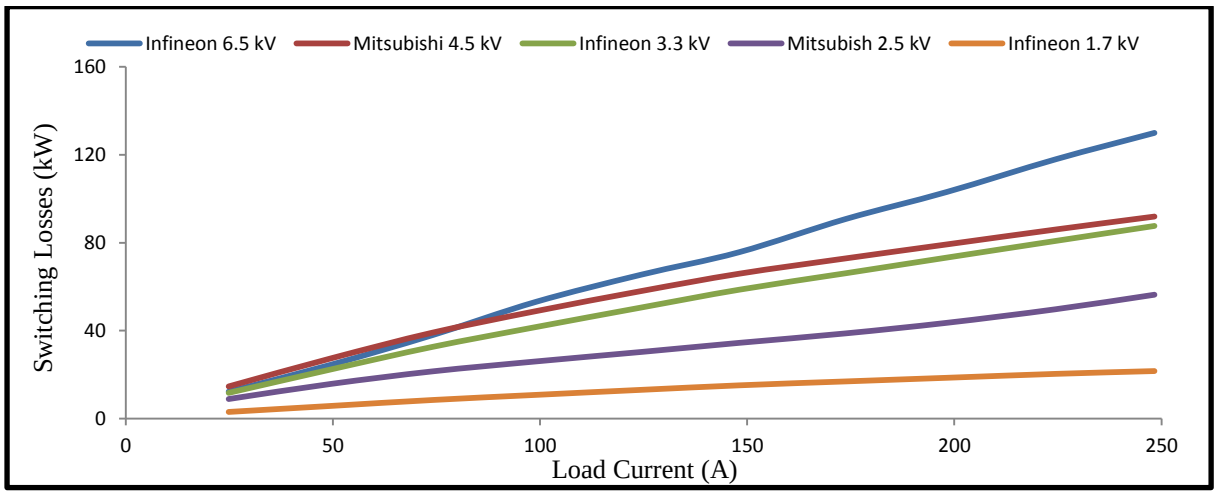


Figure 5.35: Switching power loss profile for different high-voltage IGBT devices (SPWM control)

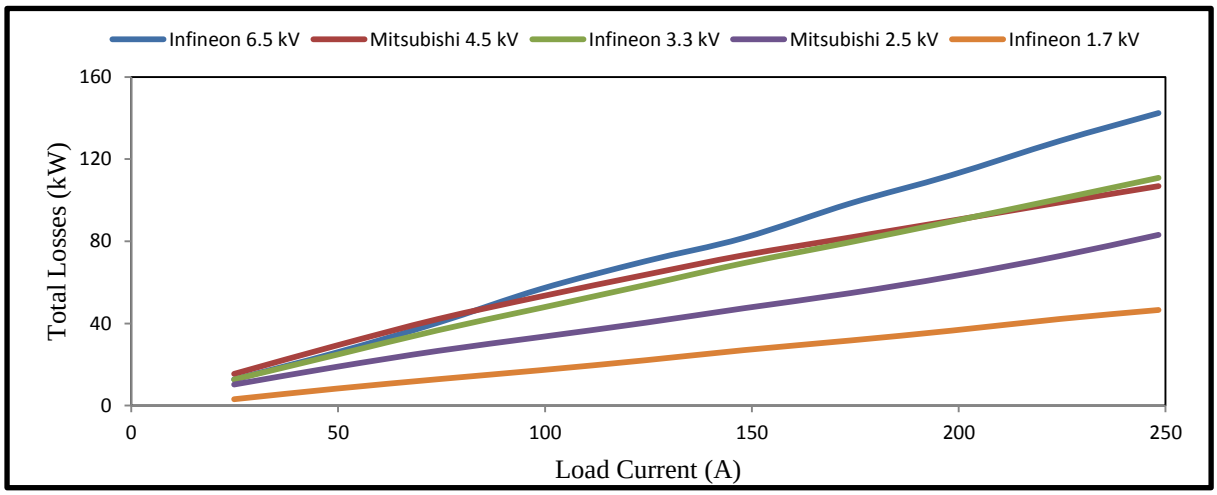


Figure 5.36: Total power loss profile for different high-voltage IGBT devices (SPWM control)

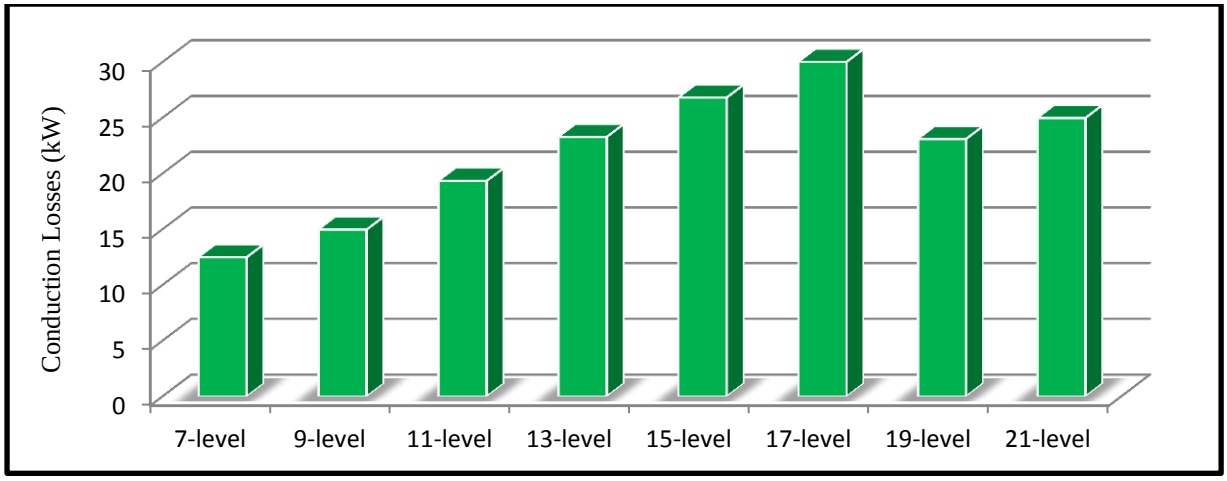


Figure 5.37: Conduction power loss profile for different numbers of inverter levels (SPWM control)

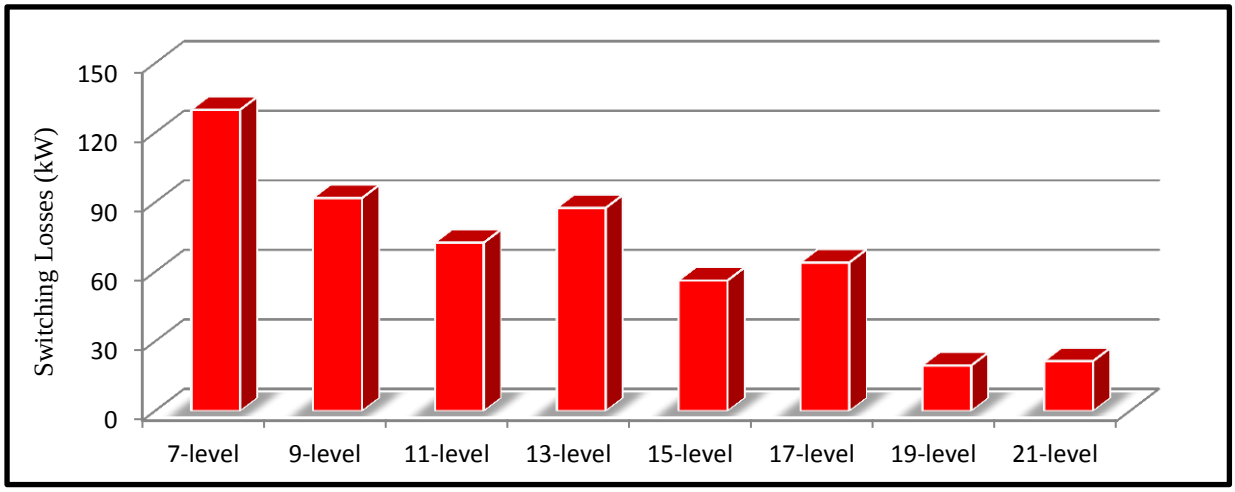


Figure 5.38: Switching power loss profile for different numbers of inverter levels (SPWM control)

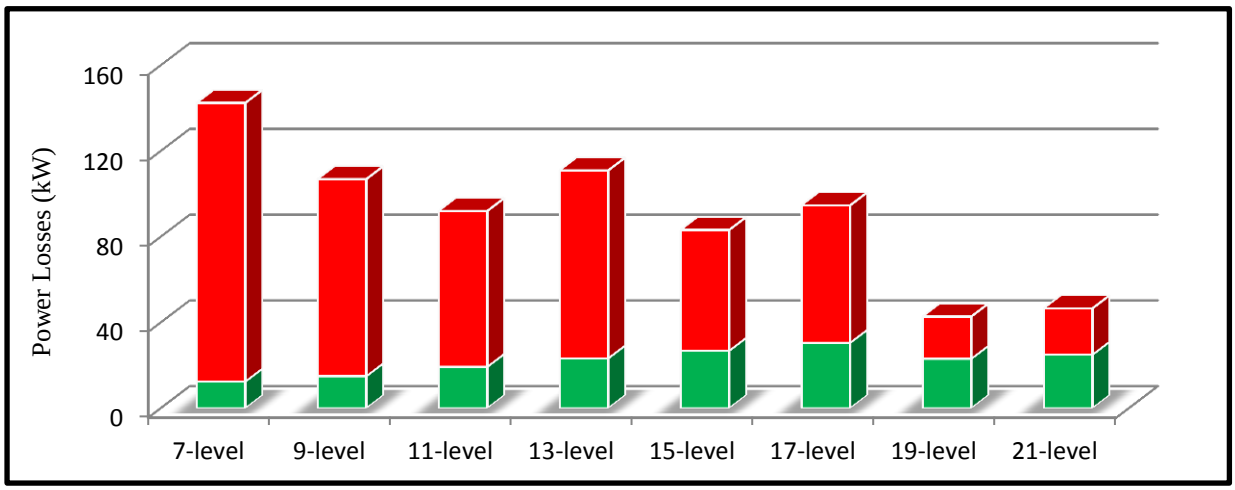
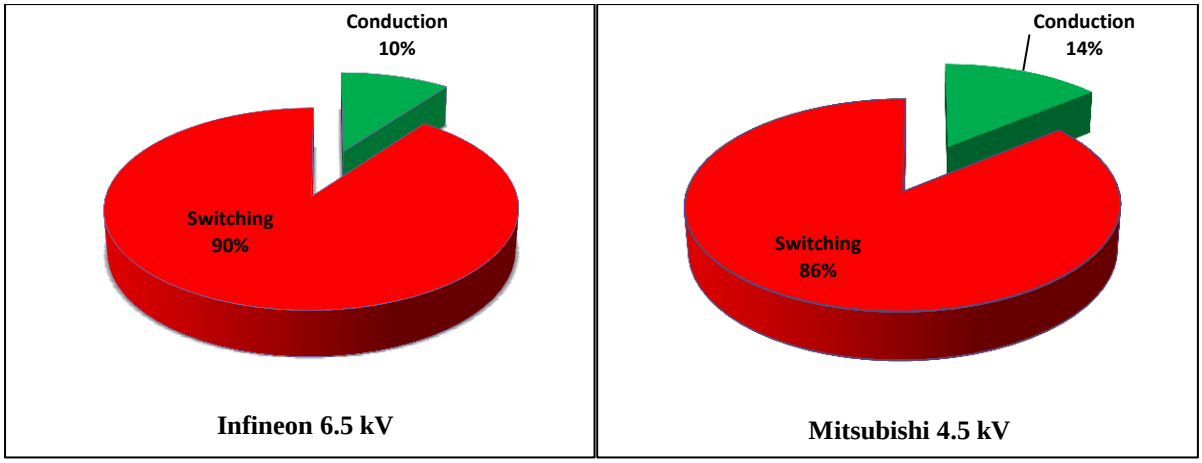
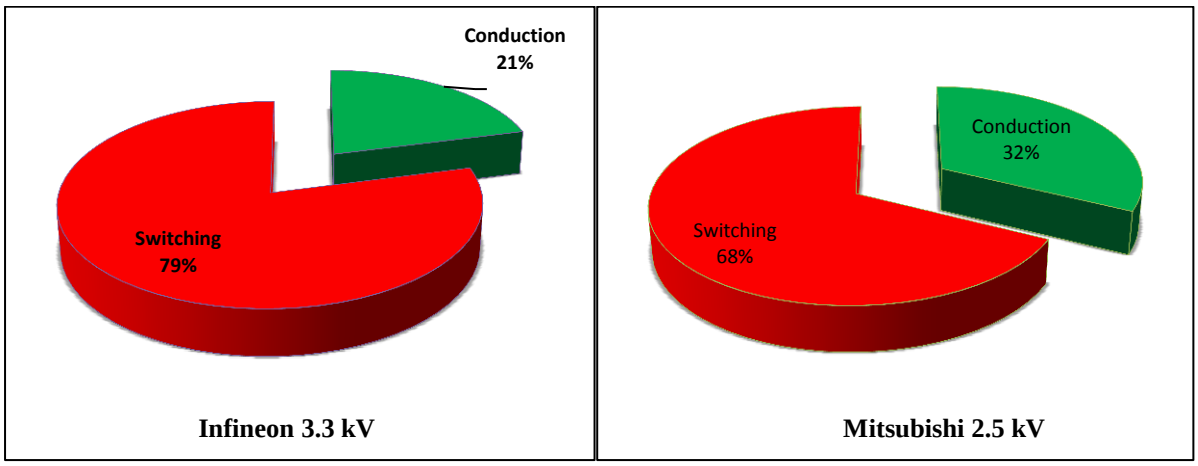


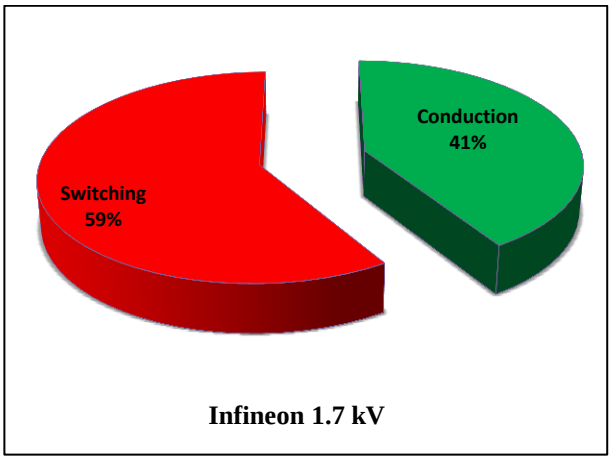
Figure 5.39: Total power loss profile for different numbers of inverter levels (SPWM control)



(a) (b)



(c) (d)



(e)

Figure 5.40: Pie chart showing conduction and switching losses for different high-voltage IGBT devices controlled using SPWM (11 kV CHB-MLI): a) FZ400R65KE3 (7-level); b) CM400HB-90H (9-level); c) FZ400R33KL2c-B5 (13-level); d) CM400DY-50H (15-level); e) FZ400R17KE3 (21-level)

5.8 Trade-Off Optimisation

5.8.1 Optimum trade-off for inverter's number of cascaded H-bridges without considering the output filter

To achieve an efficient and cost-effective CHB-MLI design in direct grid-connected applications, there is a trade-off in the number of inverter levels (i.e., the number of H-bridges cascaded in series) that can be implemented. The trade-off is based on key measures, such as the following: 1) THD, 2) switching devices cost, 3) conduction power loss, 4) switching power loss and 5) device count. The purpose of this section is to find the optimal number of inverter levels in direct grid-connected 11 kV PV power plants in which the designed inverter has the best performance at minimal cost. At this stage, the output filter is not considered in the analysis.

Figure 5.41 illustrates the THD and device counts versus the number of inverter levels. The device count measures the complexity of the inverter design. In Figure 5.41, the THD decreases as the inverter number of levels increases, which mean that at high number of levels, it is possible to connect the inverter directly to the grid and eliminate the need for an output filter. However, the results showed that the number of IGBTs required for the inverter increased linearly as the inverter number of levels increased. The lower the number of inverter levels, the higher the blocking voltage required in the device to synthesize the output voltage. However, at higher numbers of inverter levels, switching devices with lower blocking voltage are capable of synthesizing the required output voltage. Power switching devices with high blocking voltage are more expensive than devices with lower blocking voltage are.

Figure 5.42 depicts the total cost of the IGBTs, the conduction and switching power losses per inverter design versus the number of inverter levels. Increasing the number of levels produced a marginal reduction in %THD, switching power loss and the cost of the IGBTs. However, this increase results in higher conduction power loss and greater complexity in control and device counts.

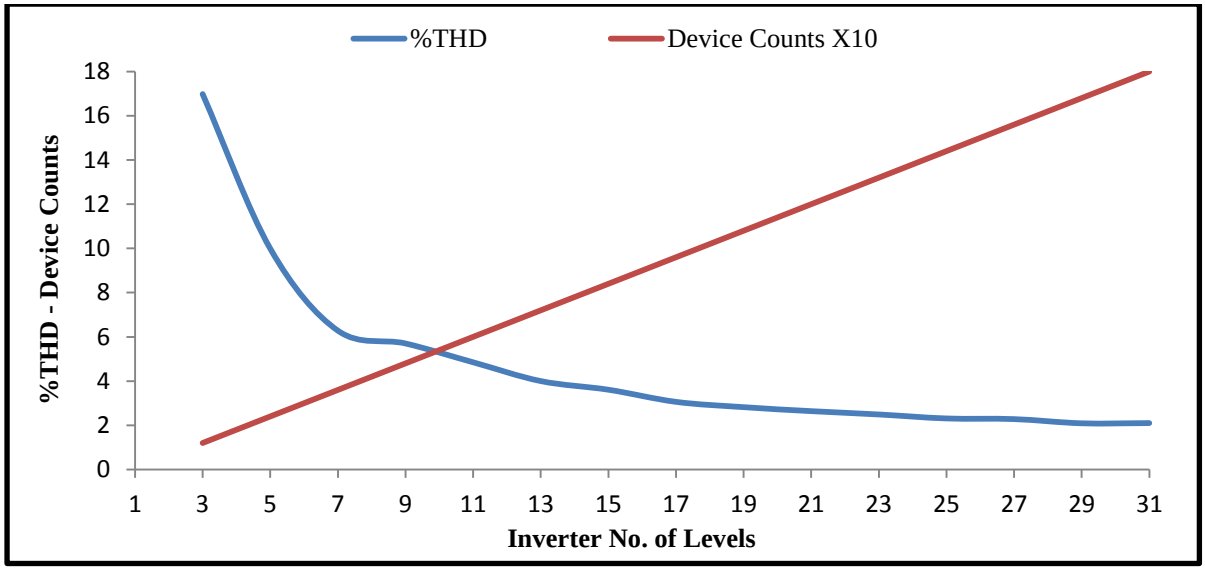


Figure 5.41: The change in %THD and device counts versus number of inverter levels

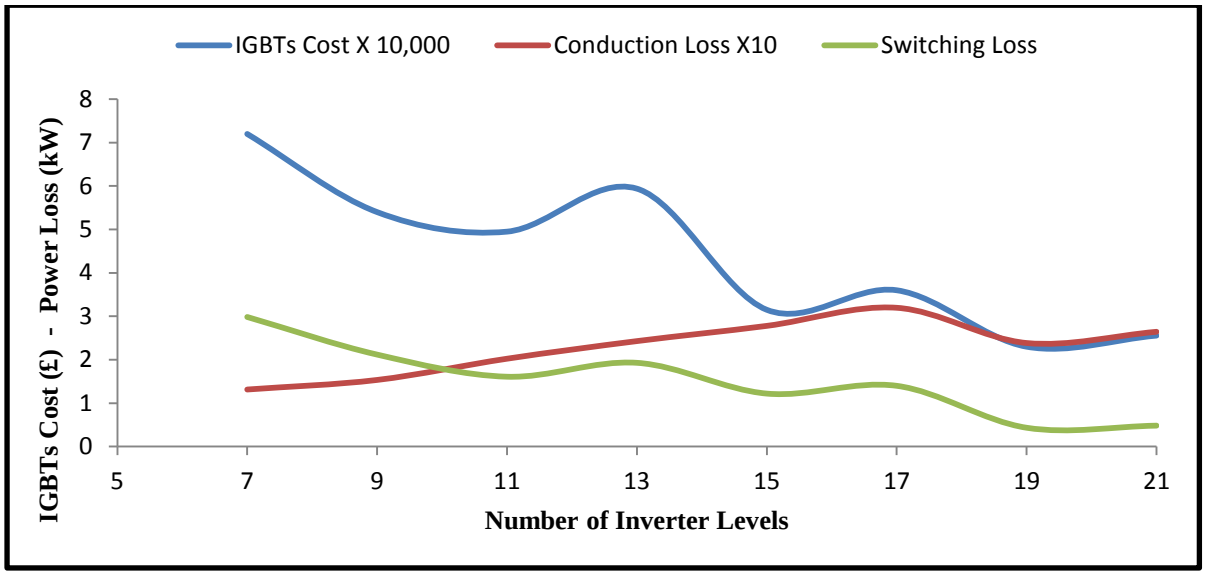


Figure 5.42: The change in IGBT cost and power loss versus number of inverter levels

In order to quantify the trade-off, the key measures are calculated and tabulated for each design. Table 5-18 demonstrates the key measures of each designed inverter for an 11 kV system. The cost of power losses is calculated in terms of equivalent annualised capital cost by applying the present value factor as follows:

$$P_{loss\_cost}\ (£) = H \times U_{Energy} \times \frac{(1+i)^y - 1}{i(1+i)^y} \times P_{losss} \qquad 5.30$$

where H is the total annual operating hours of PV power plant, assumed to be 4,380 hours at 12 hours per day.

U_{Energy} is the energy cost (0.11 £/kWh),

i is the annual interest rate for capital cost which is assumed to be 5%, and

y is the levelized period or system lifetime (years), which is assumed to be 15 years.

Table 5-18: Key Measures of Performance Calculated for Designed Inverters at Different Levels

No. Levels	5	7	9	11	13	15	17	19	21
Device Counts	48	36	48	60	72	84	96	108	120
% THD	9.95	6.28	5.7	4.85	4	3.61	3.06	2.82	2.64
P_{loss} (kW)	17.431	16.128	17.467	21.847	26.219	29.018	33.363	24.28	26.92
P_{loss} Cost (£)	87,171	80,657	87,351	109,255	131,119	145,117	166,846	121,422	134,625
IGBT Cost (£)	54,000	72,000	54,000	51,300	61,560	31,500	36,000	23,004	25,560
Total Cost (£)	141,171	152,657	141,351	160,555	192,679	176,617	202,846	144,426	160,185

These measure values are normalized, and a total measure value that combines all the normalized key measures is introduced based on the weighted averages of each quantity as follows:

$$Tot._{Measure\_Value} = 0.4 \times THD + 0.4 \times \left(P_{loss_{cost}} + IGBT_{Cost}\right) + 0.2 \times Device\ Counts \qquad 5.29$$

The structure of the cost function composes of three main measure factors as per the study optimization purpose: 1) quality of output signal (%THD), 2) system cost based on (losses and switching device cost) , and 3) system complexity measured by device count. In order to test the developed trade off optimization model, The assigned weighs for these factors was 40% , 40% and 20%. However, it depends on the application and the case understudy. The planning engineer should decide what the weights for each factor are in the objective function. Both the reliability and the system cost should be considered in the optimization. It is required to minimize the cost to meet reliability standards as constraints for the optimization. In applications that reliability in more important the objective function can be modified to reflects this in the optimization.

Figure 5.43 shows the total normalized value of different inverter designs. According to the calculated measure values, the optimal design for the 11 kV cascaded H-bridge multilevel inverter applying SHE control was found to be the nine-level inverter. The THD for the 50th harmonic was within the IEEE-519 limits. The performance of the 19-level inverter was very close to that of the nine-level design because it implemented low-cost IGBTs that featured low power dissipation characteristics, compared with the other devices. Compared to the nine-level inverter, the 19-level design had very low THD. However, it required more than double the number of devices implemented in the nine-level inverter and showed higher losses by 40%. Following the optimal solution, the 11-level and 21-level inverters showed the best performance. The five-level and 13-level designs were found to have the worst performance. The five-level inverter can implement many devices because it uses two 4.5 kV IGBTs in series and has a high THD value. The 13-level experienced higher losses with a high number of required devices and did not show a significant reduction in THD. The optimum solution, that is, the nine-level inverter, had the lowest power losses after the seven-level design. In the case of minimal power loss only, the seven-level inverter was the best compared to the other designs. Based on these results, it can be concluded that the optimal solution differs from one application to another and is based on the system designer's objectives in applying different weights to calculate the total measure value. In the next section, after the implementation of the output passive power filter (PPF), the optimal design of an 11-kV inverter will be investigated.

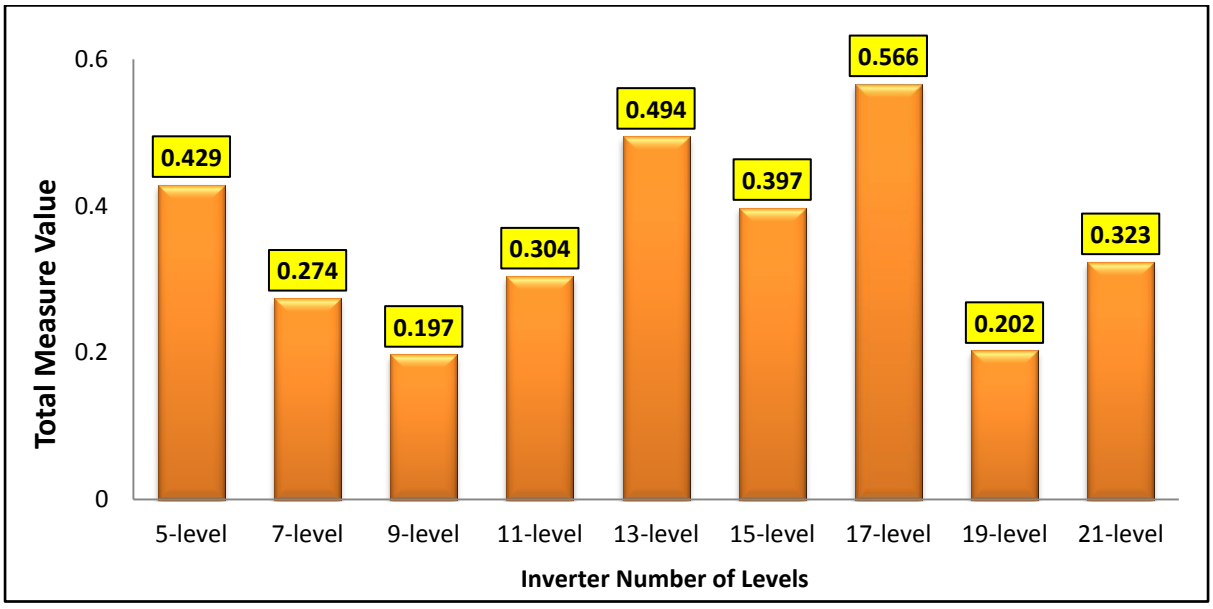


Figure 5.43: Normalized total measure performance value for multilevel inverters designed at different levels

5.8.2 Optimum Trade-off for Inverter's Number of Cascaded H-Bridges and Size of Output Filter

In the case study, a 5 MW load at a lagging power factor of 0.8 is assumed at the output of CHB-MLI with a rated line-to-line voltage of 11 kV. The aim is to propose a design for a composite PPF at the output of different levels of CHB-MLI topologies. The implemented PPF should improve the lagging power factor to between (0.92 and 0.98) and reduce the %THD at the output of the inverter. In addition, the total cost of the system, including filter cost and energy loss should be minimised. Such compensation cases require the implemented PPF to inject a total reactive power between 1.6 and 3.7 MVAR. Based on the optimisation model for the PPF design explained in Chapter 4, this section presents the results of the GA optimisation for the design of the output PPF at different levels of CHB-MLIs. The proposed designs minimise the overall cost of the system, improve the power factor and minimise the %THD.

Tables 5-19 to 5-27 present the simulation results and performances of the GA optimisation of the PPF design in different levels of CHB-MLI topologies. In this optimisation, the quality factor was 60 in single-tuned filters and 5 in high pass filters to ensure the best performance of the PPF. The five-level CHB-MLI is compensated with three ST branch filters tuned to the 7^{th}, 11^{th} and 13^{th} harmonics. A HP filter is tuned to harmonics of the 17^{th} order and higher. In contrast, the seven-level CHB-MLI has two ST branches tuned to eliminate the 11^{th} and 13^{th} harmonics. In addition, a HP filter is tuned to the harmonics beyond the 17^{th} order. The 9-level and 11-level CHB-MLIs implement one ST filter and one HP filter. All other inverters at levels 13, 15, 17, 19 and 21 apply only a HP filter for the high-order harmonics because the low-order harmonics already have been eliminated by the SHE control.

The GA proposed for the PPF designs improved the power factor as required and resulted in a significant reduction in the THD with a minimum of power loss. The three-phase line-to-line voltage before and after the filter implementation is depicted in Figures 5.44 to 5.61, which clearly show that the effects of the filter significantly improved the quality of the output voltage.

Table 5-19: GA Performance for Optimum Design of Composite PPF for a five-level CHB-MLI (11 kV L-L)

Proposed Passive Power Filter (PPF)				
Filter Type	ST	ST	ST	HP
Order	7^{th}	11^{th}	13^{th}	$>17^{th}$
Size (kVar)	450	600	450	2,450
C (µF)	3.94	5.26	3.94	21.5
L (mH)	52.4	15.9	15.2	1.63
R (Ω)	1.92	0.92	1.03	8.7
Quality Factor	60	60	60	5
Total Filter Size (kVar)			3,950	
THD Before Filter (%)			9.99	
THD After Filter (%)			4.99	

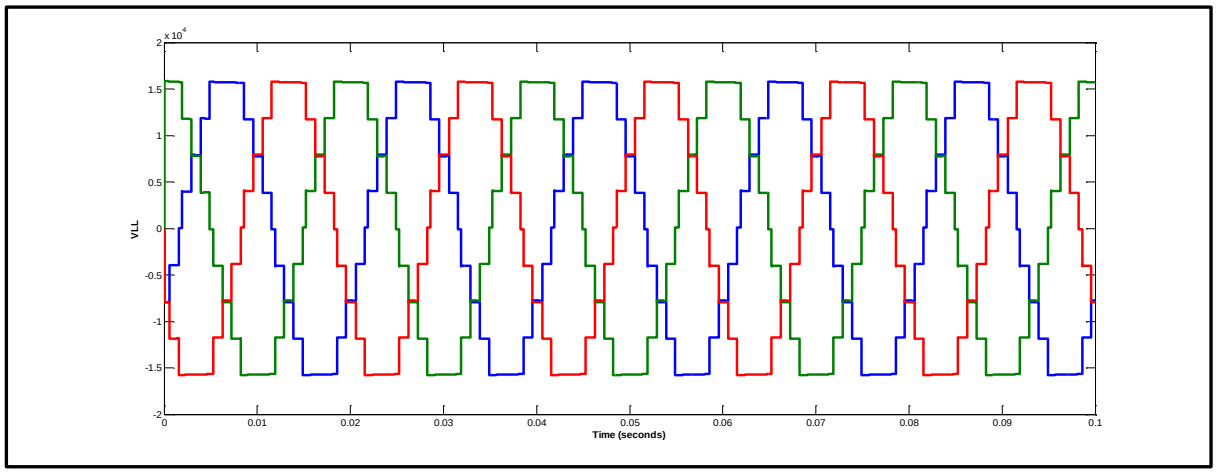


Figure 5.44: Output three-phase voltage for five-level CHB-MLI (11 kV L-L) before filter implementation

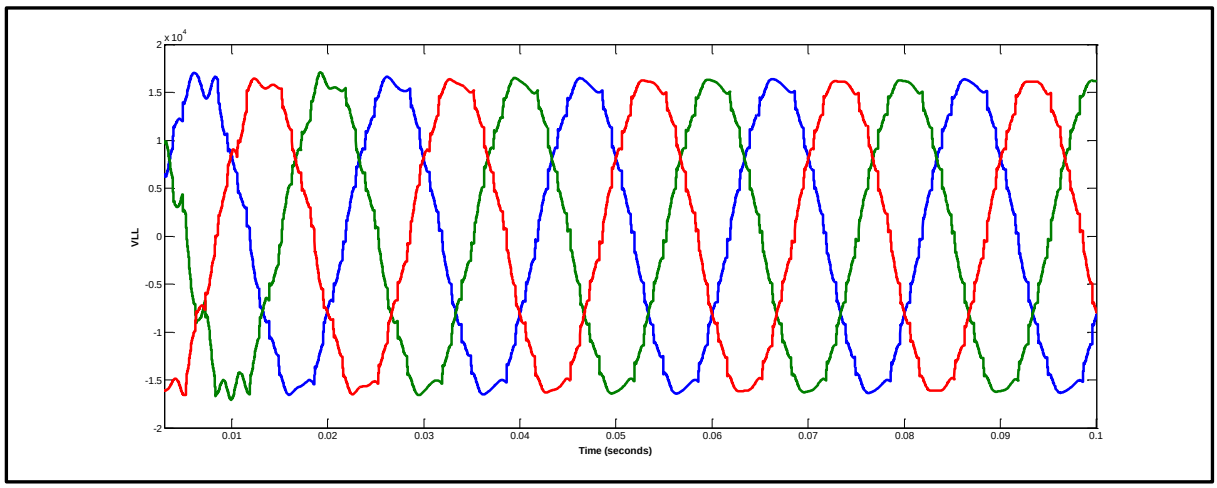


Figure 5.45: Output three-phase voltage for five-level CHB-MLI (11 kV L-L) after filter implementation

Table 5- 20: GA Performance for Optimum Design of Composite PPF for a seven-level CHB-MLI (11 kV L-L)

Proposed Passive Power Filter (PPF)			
Filter Type	ST	ST	HP
Order	11^{th}	13^{th}	$>17^{th}$
Size (kVar)	600	400	2,550
C (µF)	5.3	3.5	22.4
L (mH)	15.9	17.1	1.57
R (Ω)	0.92	1.16	8.3
Quality Factor	60	60	5
Total Filter Size (kVar)		3,550	
THD Before Filter (%)		6.28	
THD After Filter (%)		2.61	

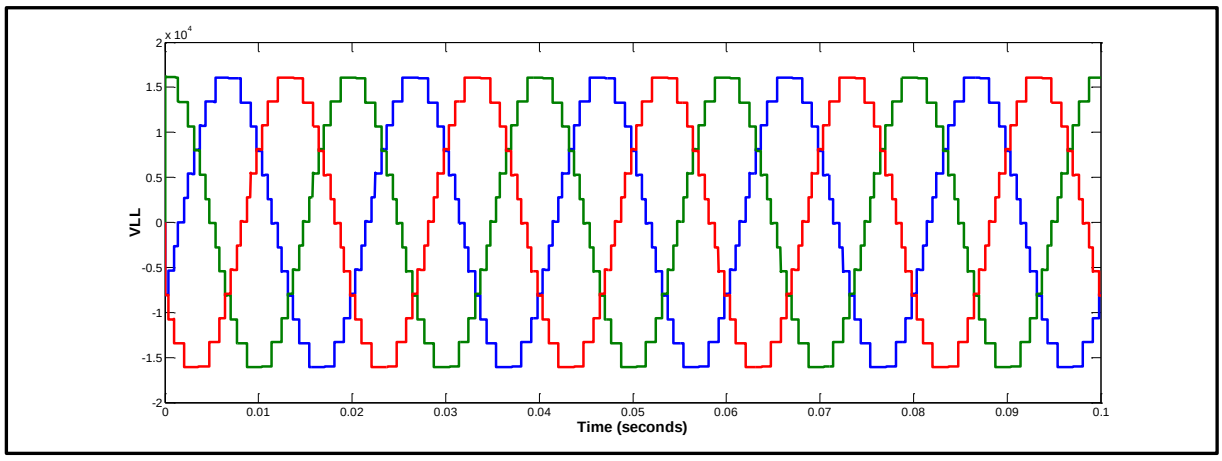


Figure 5.46: Output three-phase voltage for seven-level CHB-MLI (11 kV L-L) before filter implementation

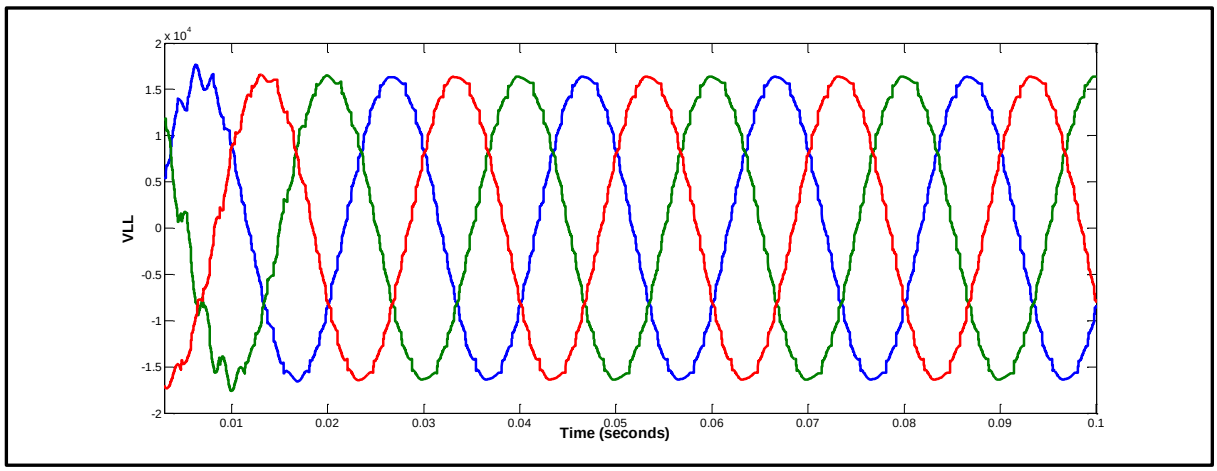


Figure 5.47: Output three-phase voltage for seven-level CHB-MLI (11 kV L-L) after filter implementation

Table 5-21: GA Performance for Optimum Design of Composite PPF for nine-level CHB-MLI (11 kV L-L)

Filter Type	ST	HP
Order	13^{th}	$>17^{th}$
Size (kVar)	350	2,900
C (µF)	3.07	25.43
L (mH)	19.53	1.38
R (Ω)	1.33	7.36
Quality Factor	60	5
Total Filter Size (kVar)	3,250	
THD Before Filter (%)	5.7	
THD After Filter (%)	1.84	

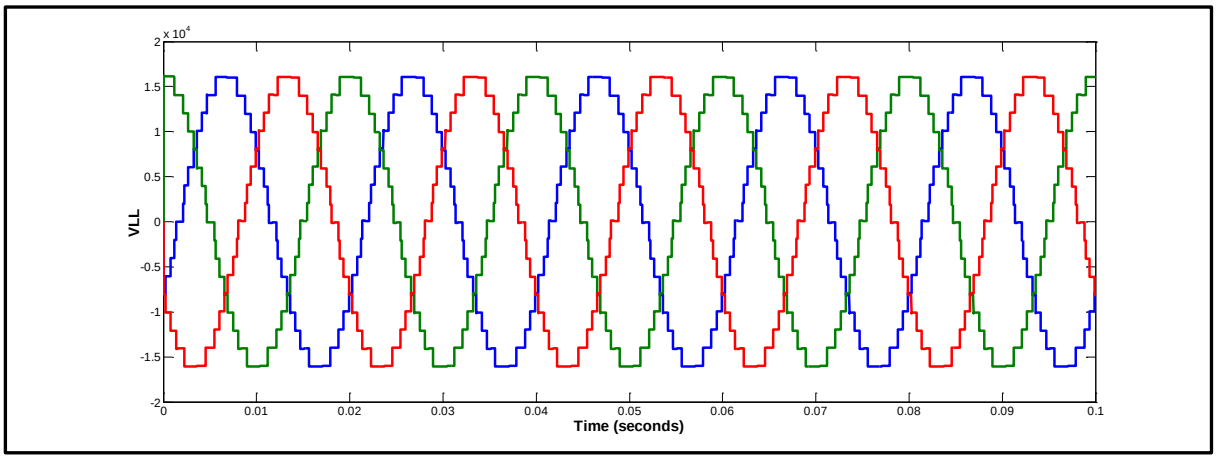


Figure 5.48: Output three-phase voltage for nine-level CHB-MLI (11 kV L-L) before filter implementation

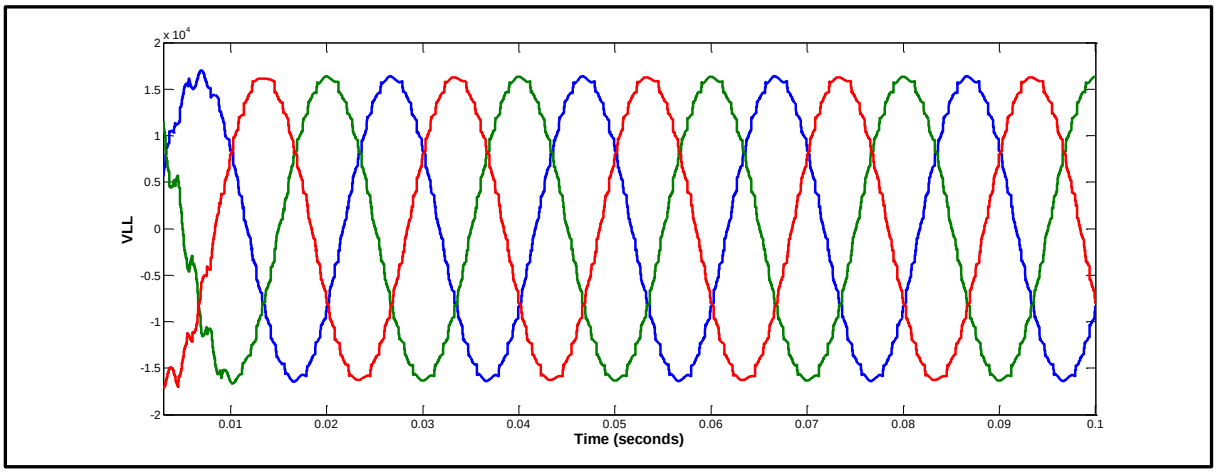


Figure 5.49: Output three-phase voltage for nine-level CHB-MLI (11 kV L-L) after filter implementation

Table 5-22: GA Performance for Optimum Design of Composite PPF for 11-level CHB-MLI (11 kV L-L)

Filter Type	ST	HP
Order	17^{h}	$>19^{th}$
Size (kVar)	550	2,500
C (μF)	4.82	21.92
L (mH)	12.43	1.28
R (Ω)	0.85	7.64
Quality Factor	60	5
Total Filter Size (kVar)	3,050	
THD Before Filter (%)	4.85	
THD After Filter (%)	1.42	

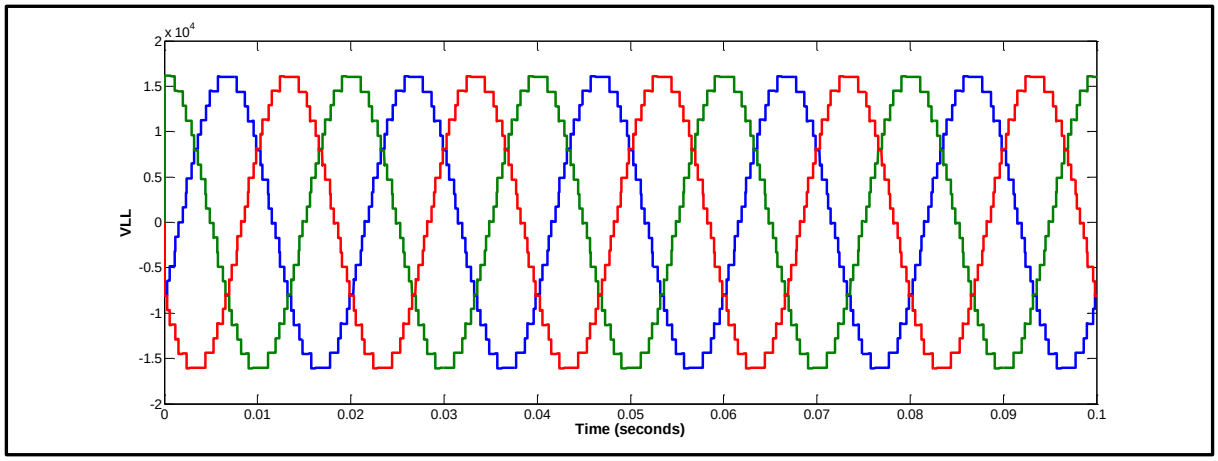


Figure 5.50: Output three-phase voltage for 11-level CHB-MLI (11 kV L-L) before filter implementation

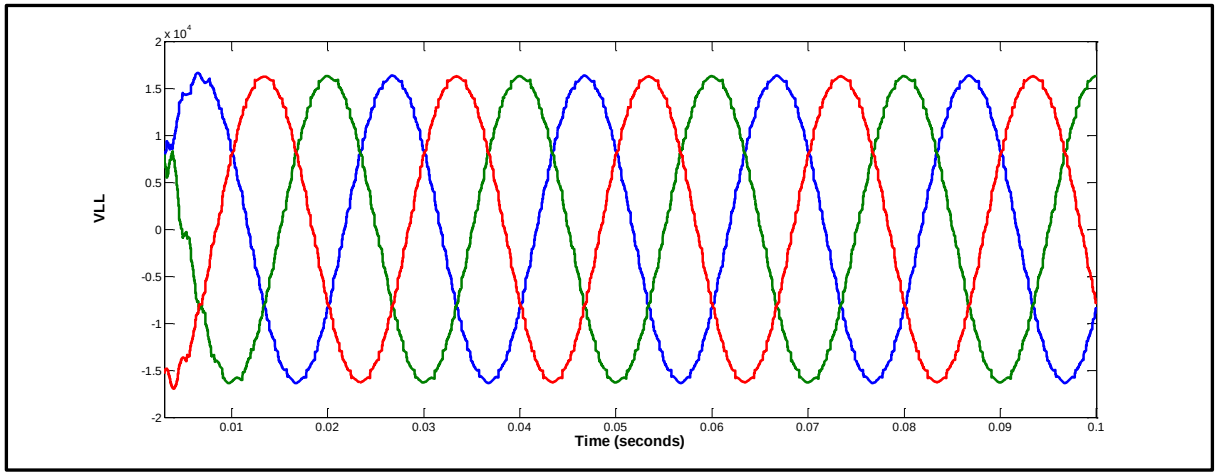


Figure 5.51: Output three-phase voltage for 11-level CHB-MLI (11 kV L-L) after filter implementation

Table 5-23: GA Performance for Optimum Design of Composite PPF for 13-level CHB-MLI (11 kV L-L)

Proposed Passive Power Filter (PPF)	
Filter Type	HP
Order	>19th
Size (kVar)	2,750
C (µF)	24.11
L (mH)	1.16
R (Ω)	6.95
Quality Factor	5
Total Filter Size (kVar)	2,750
THD Before Filter	4.0 %
THD After Filter	1.33 %

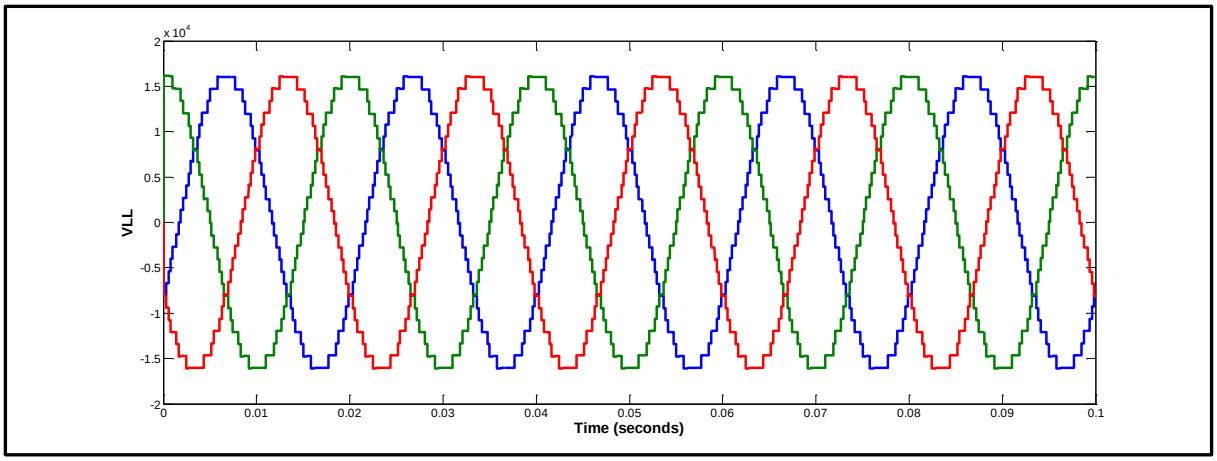


Figure 5.52: Output three-phase voltage for 13-level CHB-MLI (11 kV L-L) before filter implementation

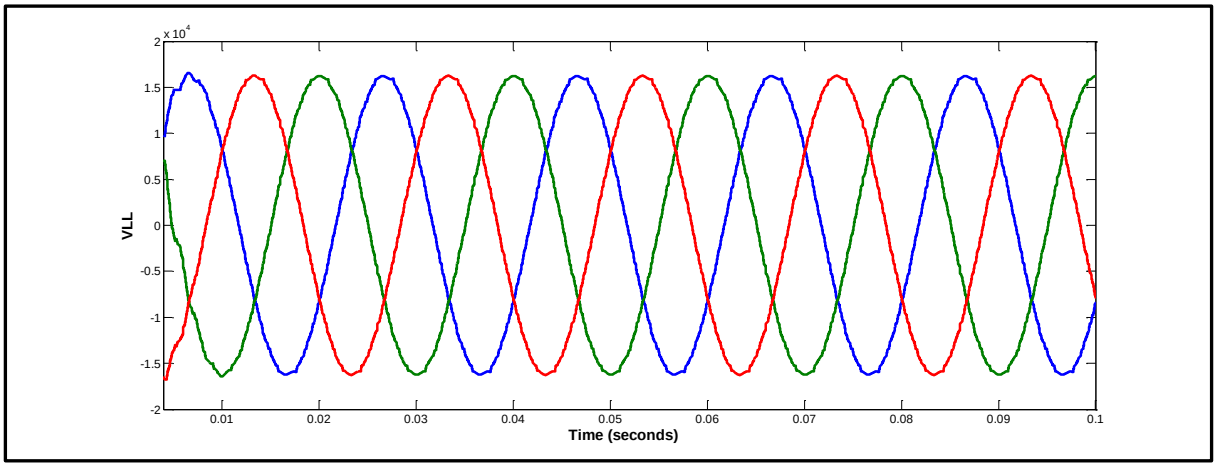


Figure 5.53: Output three-phase voltage for 13-level CHB-MLI (11 kV L-L) after filter implementation

Table 5-24: GA Performance for Optimum Design of Composite PPF for 15-level CHB-MLI (11 kV L-L)

Proposed Passive Power Filter (PPF)	
Filter Type	HP
Order	>19th
Size (kVar)	2,500
C (µF)	21.92
L (mH)	1.28
R (Ω)	7.64
Quality Factor	5
Total Filter Size (kVar)	2,500
THD Before Filter (%)	3.61
THD After Filter (%)	1.34

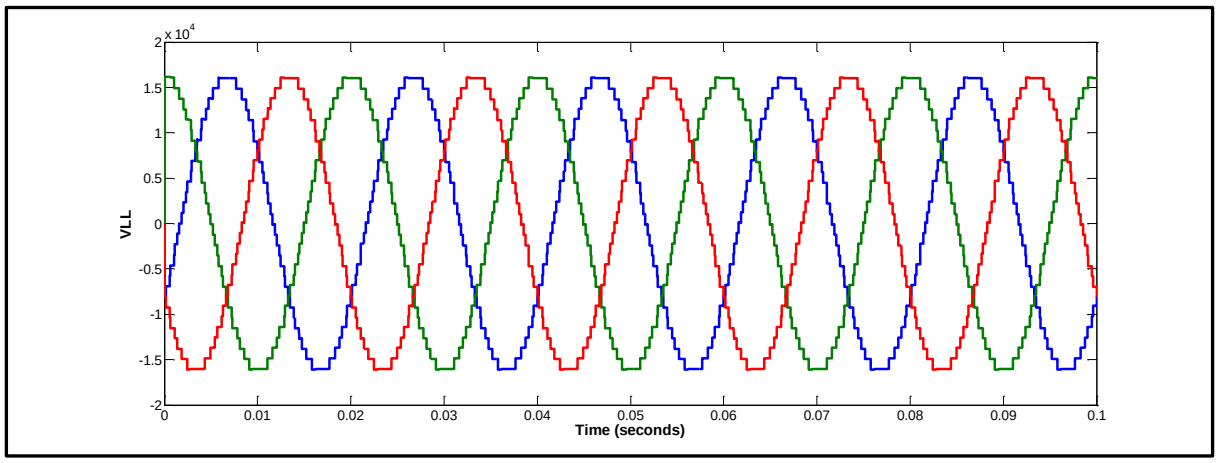


Figure 5.54: Output three-phase voltage for 15-level CHB-MLI (11 kV L-L) before filter implementation

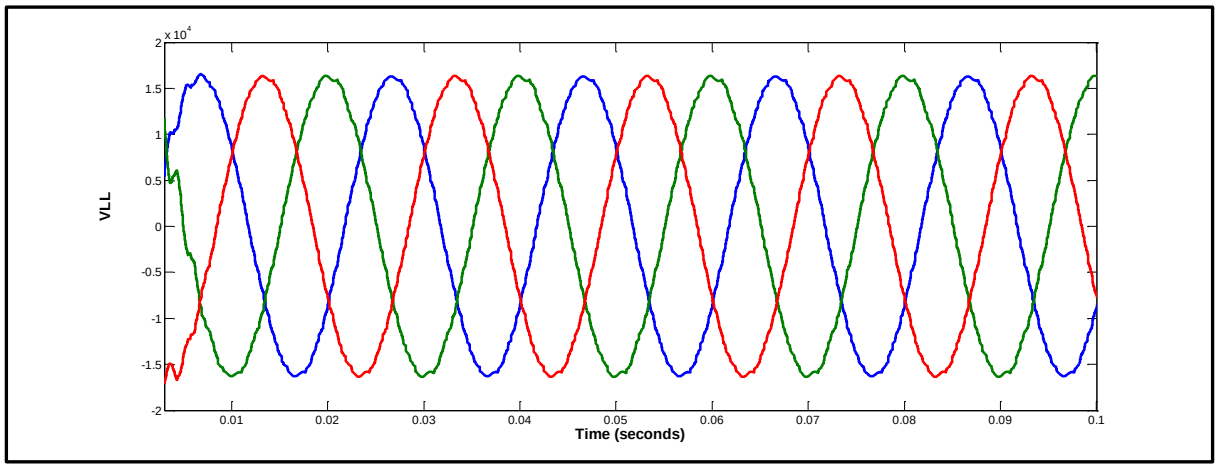


Figure 5.55: Output three-phase voltage for 15-level CHB-MLI (11 kV L-L) after filter implementation

Table 5-25: GA Performance for Optimum Design of Composite PPF for 17-level CHB-MLI (11 kV L-L)

Proposed Passive Power Filter (PPF)	
Filter Type	HP
Order	>19th
Size (kVar)	2,100
C (μF)	18.41
L (mH)	1.52
R (Ω)	9.1
Quality Factor	5
Total Filter Size (kVar)	2,100
THD Before Filter (%)	3.06
THD After Filter (%)	1.31

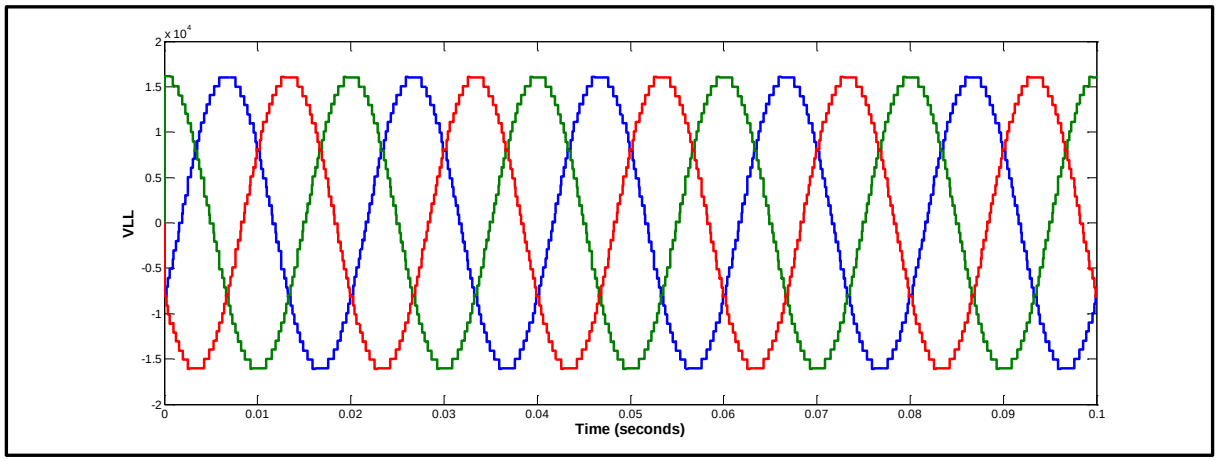


Figure 5.56: Output three-phase voltage for 17-level CHB-MLI (11 kV L-L) before filter implementation

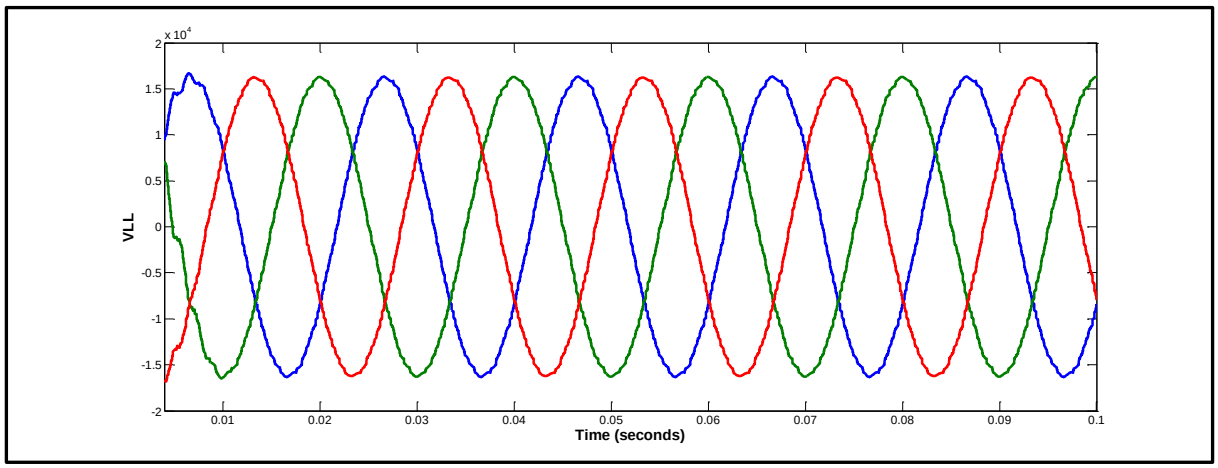


Figure 5.57: Output three-phase voltage for 17-level CHB-MLI (11 kV L-L) after filter implementation

Table 5-26: GA Performance for Optimum Design of Composite PPF for 19-level CHB-MLI (11 kV L-L)

Proposed Passive Power Filter (PPF)	
Filter Type	HP
Order	>19th
Size (kVar)	1,800
C (µF)	15.78
L (mH)	1.78
R (Ω)	10.61
Quality Factor	5
Total Filter Size (kVar)	1,800
THD Before Filter (%)	2.82
THD After Filter (%)	1.25

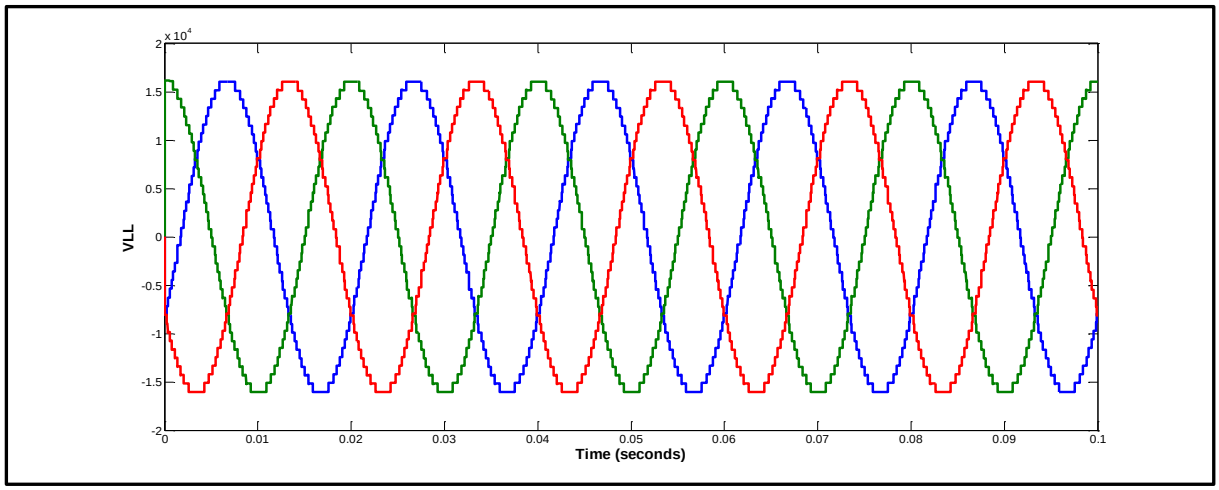


Figure 5.58: Output three-phase voltage for 19-level CHB-MLI (11 kV L-L) before filter implementation

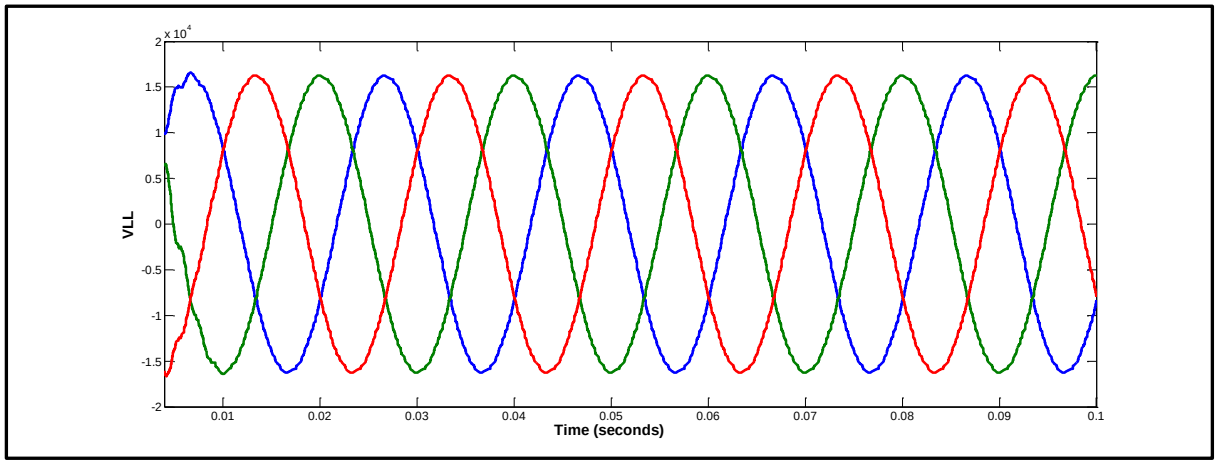


Figure 5.59: Output three-phase voltage for 19-level CHB-MLI (11 kV L-L) after filter implementation

Table 5-27: GA Performance for Optimum Design of Composite PPF for 21-level CHB-MLI (11 kV L-L)

Proposed Passive Power Filter (PPF)	
Filter Type	HP
Order	>19th
Size (kVar)	1,750
C (µF)	1.83
L (mH)	15.34
R (Ω)	10.91
Quality Factor	5
Total Filter Size (kVar)	1,750
THD Before Filter (%)	2.64
THD After Filter (%)	1.29

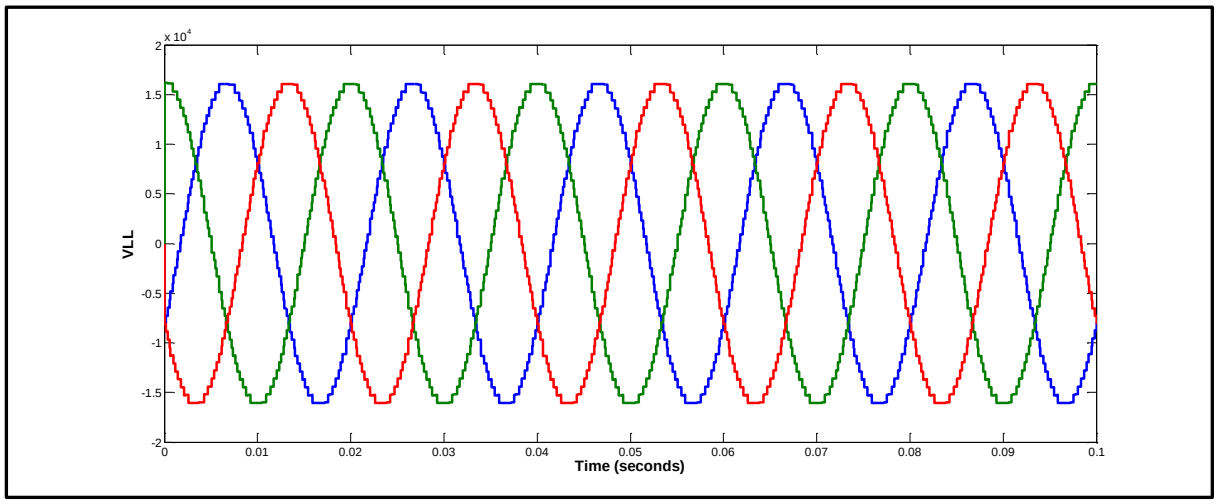


Figure 5.60: Output three-phase voltage for 21-level CHB-MLI (11 kV L-L) before filter implementation

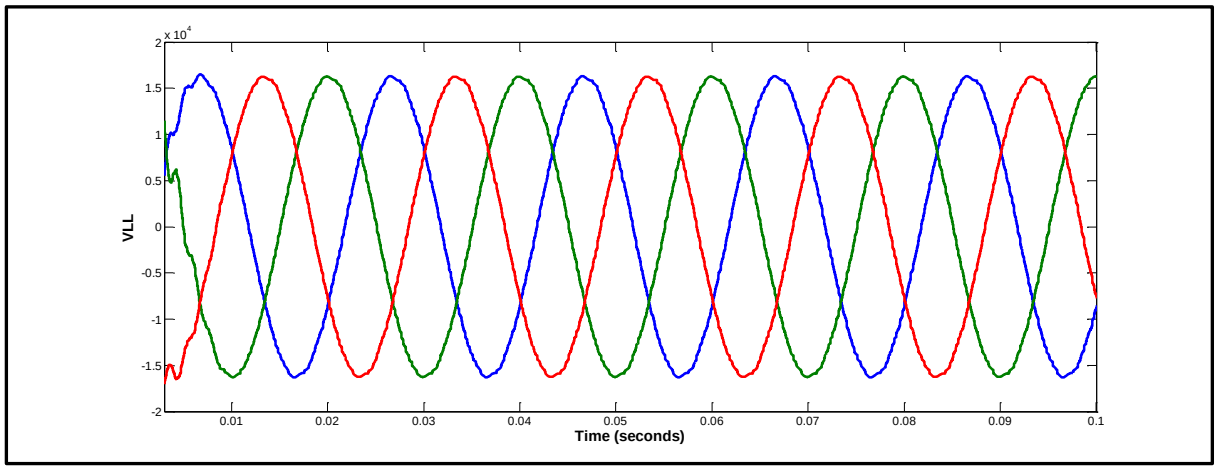


Figure 5.61: Output three-phase voltage for 21-level CHB-MLI (11 kV L-L) after filter implementation

To quantify the trade-off, the key measures for the design of different inverter levels (5 to 21 levels) and their corresponding optimum PPFs are displayed in Table 5-28.

Table 5-28: Key Measures Performance Calculated for the Designed Inverters and optimal PPF at different levels.

No. Levels	5	7	9	11	13	15	17	19	21
Device Counts	48	36	48	60	72	84	96	108	120
% THD	4.99	2.62	1.84	1.42	1.33	1.34	1.31	1.25	1.29
P_{loss} (kW)	22.18	22.93	15.5	19.11	18.59	24.2	23.67	16.71	18.61
P_{loss} Cost (£)	110,925	114,656	77,509	95,593	92,987	120,937	118,377	83,565	93,062
IGBT Cost (£)	54,000	72,000	54,000	51,300	61,560	31,500	36,000	23,004	25,560
Filter Size (KVAR)	3,950	3,550	3,250	3,050	2,750	2,700	2,100	1,800	1,750
Filter Cost (£)	40,000	36,000	32,500	30,500	27,500	27,000	21,000	18,000	17,500
Total Cost (£)	204,925	22,656	164,009	177,393	182,047	177,437	175,377	124,569	136,122

A total measure value of each design that combines all the normalized key measures is applied based on weighted averages as follows:

$$T_{M_V} = 0.4 \times THD + 0.4 \times \left(P_{loss_{cost}} + IGBT_{Cost} + Filter_{cost}\right) + 0.2 \times Device\ Counts \qquad 5.30$$

The total measure values for each design are compared in Figure 5.62. Based on the calculated normalized total measure values, the CHB-MLIs with 19-level was found to be the best design. This result can be justified by the smaller size of PPF required for this topology and the low THD at its output. In addition, the implemented IGBT device at 1.7 kV for 19-level had very low power loss dissipation compared to the high-voltage IGBTs used in the other designs. The nine- and 21-levels were found to be the best following to the 19-level topology. In contrast, topologies with lower numbers of levels (typically 5- and 7-level) were found to have the worst total measure values mainly because of high components cost, high power losses and high THD values. Furthermore, they also required larger size PPFs with two single-tuned branches and one HP branch. The proposed multi-objective function could be modified to meet the objectives of design engineers. In some designs, the minimisation of power loss is very important. In other designs, the THD or power factor is important. The weighted averages of the multi-objectives are chosen according to the aims of the designer engineer.

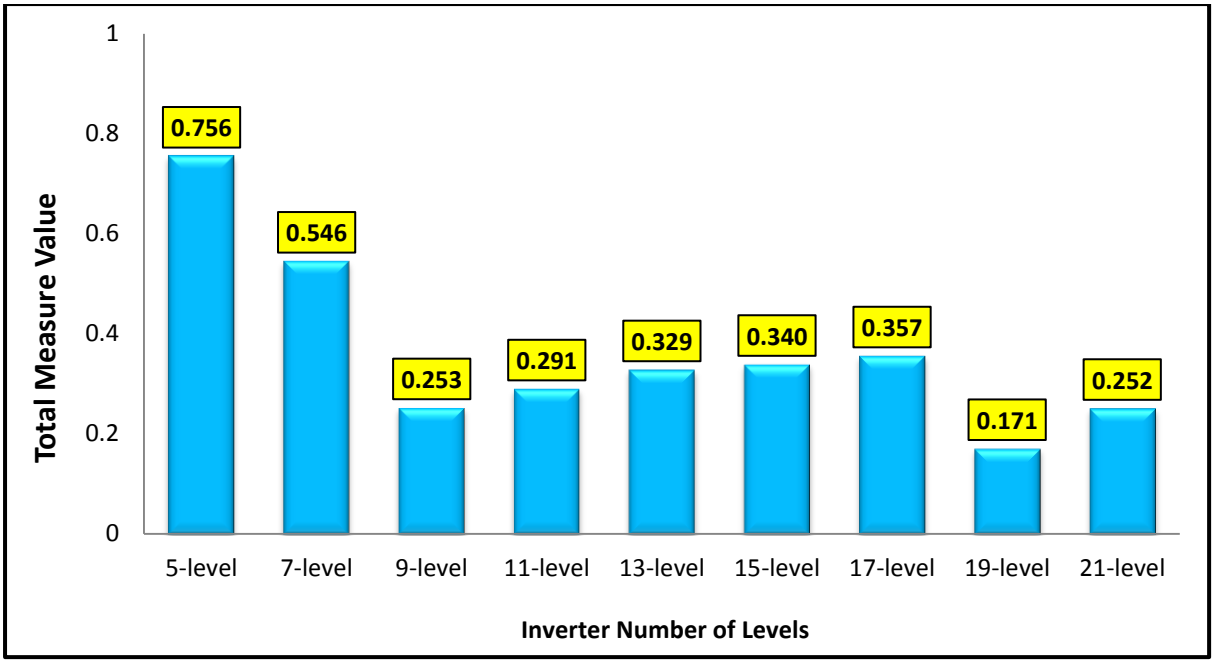


Figure 5.62: Normalized total measure performance value for CHB-MLI designed at different levels with implemented composite PPF

The optimum size of output passive power filters for different inverter's levels are displayed in Figure 5.63. The optimum solution showed that as the inverter level increased, the optimal size of output filter decreases.

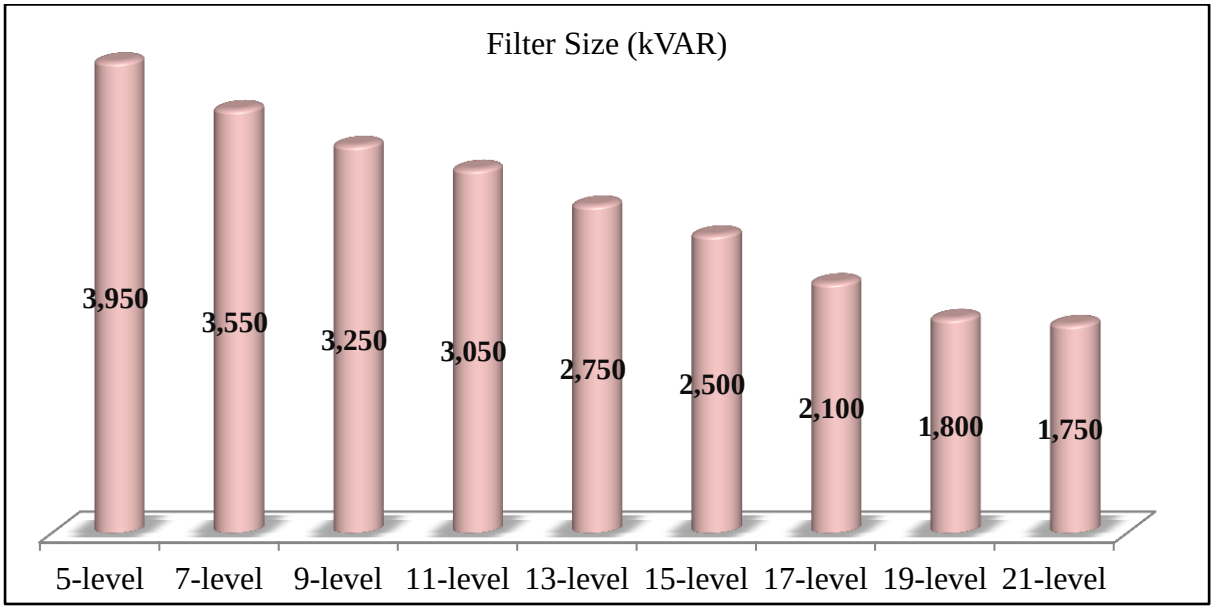


Figure 5.63: Optimum passive power filter (PPF) size in kVARs for different inverter's levels

5.9 Summary

This chapter presented an analysis of the trade-off required to achieve the optimal design of a CHB-MLI in a Matlab/Simulink simulation environment. The analysis was conducted in three main parts.

In the first part, the inverter control was optimised for minimal THD. The optimal switching angles of SHE control were solved for different levels of CHB-MLIs (3 to 31 levels). The GA was found to be efficient and powerful in solving the problem even at higher numbers of inverter levels. In addition to finding the optimal switching angles for each inverter topology, the output THD was minimised. The generated simulation results offered a generic optimal solution of the switching angles in CHB-MLIs of levels 3 to 31. The THD was studied at different inverter levels by applying the SHE control. The outcome was compared with different SPWM control methods, and the SHE control was found to achieve minimal THD values.

In the second part of the analysis, the conduction and switching power losses were evaluated and investigated for different levels of CHB-MLIs by applying the SHE control and different SPWM controls. The inverter losses were much lower in the case of inverters controlled by SHE compared to SPWM. The main reason is the that the SHE control was applied at a fundamental frequency, which minimised the switching losses considerably. Based on the results of part one and part two of the analysis, the SHE control is recommended for the trade-off optimisation because it had minimum THD values and significantly lower losses in inverter power.

In the last part of the analysis, the trade-off optimisation model was applied in the case study of an 11 kV, 5 MW. Key measures, such as THD, power loss, inverter cost and inverter complexity represented by device counts, were applied to the trade-off optimisation. The results showed that the CHB-MLI with a nine-level inverter was the best design. A further trade-off optimisation was carried out using an output composite PPF that was designed by GA. The results showed that inverters with a high number of levels had a minimal objective function compared to those with a low number of levels. The 19-level inverter was the best design in this case study because it implemented switching devices with low power dissipation, and it required a smaller output filter.

The purpose for applying GA optimization in this study, was for planning of the multilevel inverter design in which the running time of the optimizer has no significant importance. But it was important to test most of the possible solution. The GA takes longer time as it evaluates the fitness functions for all individuals. The convergence time might be significantly improved when applying intelligent fitness functions or by applying hybrid optimization techniques which have faster convergence time.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

Currently, grid-connected PV power plants are considered the fastest-growing energy technology, with annual growth of about 33%, according to the British Petroleum Plc report-2016 [4]. The current trend is to integrate PV power plants into power grids via voltage-source multilevel inverters, which have many technical attractions and features compared to conventional two-level inverters. CHB-MLI topology is superior among voltage-source multilevel-inverter topologies for high-power–medium-voltage applications, as explained in Section 2.3. This will lead to further implementation of high-power–medium-voltage CHB-MLIs in current and future power networks. These multilevel inverters generate output AC voltage in a number of steps, based on the inverter's circuit design. In practice, there is a trade-off in deciding how many levels are required for power applications in the CHB-MLI design. The trade-off depends on many factors such as power loss, power quality, system complexity, switching devices, inverter control and output-filter size, and the overall cost of the system as described in Section 4.2. This trade-off problem is a research gap, which requires further investigation of the potential for optimisation.

This thesis aims to provide a generic model to optimize the trade-off problem for the CHB-MLI's number of levels and output-filter size in high-power–medium-voltage applications. The applied methodology is based on minimisation of inverter conduction and switching power loss, optimisation of the inverter control for minimum THD and optimisation of the output-filter size and cost. In this study, the purpose was to find a feasible method to quantify the existing trade-off key measures in order to optimize the design for number of levels in the cascaded H-bridge multilevel-inverter (CHB-MLI) topology and the required size of output filter for medium-voltage–high-power applications. Key measures include: 1) inverter's number of levels, 2) conduction and switching-power losses, 3) output THD, 4) power-switching device counts and ratings, 5) size of output filter and 6) system cost per device. There is an optimum number of inverter levels and size of output filter where the integration system achieves its lowest cost, based on optimisation dimensions and applied system constraints. This has been accomplished by introducing a new trade-off model, based on multi-objective optimisation to minimize these key measures. GA was implemented to optimize the inverter control for minimum THD. A precise model for conduction and switching-power loss is proposed as estimation tool of a key measure value of the trade-off model. The filter-output design was optimized using GA. The following tasks were

accomplished and are considered to be contributions to current knowledge in the field of efficient integration of renewable energy sources into power systems:

1. A comprehensive critical literature review of high-power inverters, starting with general classification and a detailed discussion on state-of-the-art CSIs and VSIs, highlighting the operating principle, key features and historical background of each topology, followed by a technical point-by-point comparison. Then, a further critical review of VSIs covered the three basic topologies, which also provided a technical comparison in a separate table. This literature review ended by illustrating the most widely applied control techniques for voltage-source multilevel inverters. The outcome achieved from this critical review shows that for medium-voltage–high-power applications, the CHB-MLI is superior compared to other high-power inverters, due to its many advantages and features. Hence, this topology was considered for the trade-off optimisation model.

2. The problem of power system harmonics was addressed by providing a description of the phenomenon, classifying its main sources, discussing the adverse effects of harmonics on power systems and reviewing the existing solutions applied for harmonics mitigation. Subsequently, a greater focus on power filters was provided by conducting a critical review of filter configurations. This task concluded by providing important and helpful selection tables for passive, active and hybrid power filters.

3. Based on completion of the reviewing of high-power inverters, multilevel inverters and multilevel control, a decision was made to implement the CHB-MLI for efficient integration of medium-voltage– high-power application. SHE was selected as the applied control as it has a low switching frequency, which significantly minimized inverter-switching losses. For the output-filter topology, a composite passive power filter was chosen to connect to the CHB-MLI output. This filter consisted of single-tuned shunt filters to eliminate predominant low-order harmonics, and a high-pass filter was chosen for the higher-order harmonics. The reason for selecting this topology was its simple structure, low cost and minimal losses. The decision to select the type of integration-circuit configuration comprising the CHB-MLI and the output filter is the first step towards an efficient integration system.

4. A mathematical model for the problem of SHE control in CHB-MLI was demonstrated. Different existing solution approaches for the SHE problem were discussed, addressing the key features, merits and drawbacks of each approach. Based on the literature, the SHE problem can be solved using a) iterative methods, b) resultant theory, or c) heuristic methods. A preliminary study was conducted by the author to compare three techniques for solving the SHE problem for seven-level CHB-MLI [72]. In this study, NR, PSO and GA performance were compared for solving the SHE problem. Based on the review and the outcome of the preliminary study, it was found that heuristic techniques efficiently solve the SHE problem. This is mainly because heuristic techniques are capable of solving the problem over the entire range of the modulation index. They can also find a solution for inverters with a high number of levels, without additional complications and computational burdens. However, more care should be taken when defining the objective function as it has a significant effect on the solution. A generic GA-based optimisation model has been introduced for solving the switching angles of the SHE problem for CHB-MLI at any number of levels.

5. The problem of power-loss evaluation in multilevel inverters was investigated. Calculating the conduction and switching-power losses in multilevel inverters is a complicated task compared to conventional two-level inverters. This is mainly due to the fact that the current in each power switch is different, and it is affected by the applied switching-function-control method. In the literature, most of the applied methods are based on estimation and not on accurate calculations. It is critical to evaluate inverter power losses in the planning stage. A proposal was made for a generic detailed model to precisely calculate conduction and switching-power losses in multilevel inverters, based on actual power-switch datasheets. The model can be applied for any multilevel-inverter topology with any number of levels.

6. The optimum design of PPF at the output of the multilevel inverter was considered. First, a comprehensive review was carried out to implement conventional and heuristic approaches in PPF design. This review showed that the conventional approach for PPF design suffers from many limitations. Conversely, heuristic techniques are capable of efficiently finding the optimum PPF design while also taking account of cost in the analysis. A GA-based optimum-design model for PPF, based on both economic and technical considerations, is proposed for the trade-off problem.

7. The proposed optimum trade-off model was implemented in Matlab/Simulink. The simulation results were presented and discussed in detail for all considered cases, which led to the following achievements:

- Solution of the SHE problem was obtained for CHB-MLI with different levels (3 to 31). The proposed GA-based optimisation determined the unknown switching angles, eliminated the low-order predominate harmonics and minimized the %THD for each level of inverter topology. The analysis showed that, beyond 31-levels, minimisation of %THD is limited. It was found that it is not technically and economically feasible to increase the inverter number of levels beyond 31. The obtained solution tables for switching angles can be used directly by researchers, which is considered to be a contribution to knowledge in this field.

- The proposed model for conduction and switching-losses calculations in multilevel inverters was applied to a case study in which different inverter levels with different power-switching devices were investigated. The considered high-voltage IGBTs were chosen according to market availability, with blocking voltage 1.7, 2.5, 3.3, 4.5 and 6.5 kV. A curve-fitting tool was applied, based on the considered devices' datasheets, to assure accuracy throughout the analysis. In the case study, inverter losses were investigated by applying different control techniques, which are low-frequency SHE and high-frequency SPWM, namely PD-SPWM, POD-SPWM and APOD-SPWM. The outcome of this study showed that CHB-MLI controlled by SHE for medium-voltage–high-power applications experienced lower power losses compared to CHB-MLI controlled by a different SPWM control. This is because the SHE control applied low-switching frequency, which minimized the switching-power loss. Generally, the conduction loss was found to increase as the inverter's number of levels increased. Conversely, the switching loss declined sharply as the number of inverter levels increased. However, this also depends on the IGBT blocking voltage and power-loss dissipation. Devices with low blocking voltage (namely 1.7 kV) have a power-dissipation value of almost 50% compared to devices with higher blocking voltage as per their datasheets.

- For the conducted case study of designing 11 kV CHB-MLI, applying SHE control, it was found that the inverters designed with nine levels or higher generate good-quality AC waveforms at their output, which is within the IEEE-519 recommended limits. Other topologies (namely 5-level and 7-level) have THD output above the recommended standards. In the investigation for the case without an output filter, the nine-level CHB-MLI was considered best, based on applied key measures.

- Considering the output composite PPF for different level CHB-MLIs, the GA optimisation design for the filter showed that, as the inverter's number of levels increases, the optimum size of the output filter becomes smaller. This can be justified as the quality of the voltage waveforms is better for higher inverter levels.

- The analysis showed that power-loss dissipation of the implemented IGBT device and the required size of output filter are the main factors for the trade-off optimisation. Accordingly, inverters with a higher number of levels have a minimal objective function compared to those with a lower number of levels. The inverter design for 19-levels was found to be best for the considered case study. This is mainly because the 19-level design implements switching devices that have low power loss dissipation and cost less compared to devices with higher blocking voltage. Furthermore, the 19-level inverters requires small filter size at its outputs which making the design at low cost.

- Finally, the applied trade-off optimisation is generic and can be applied for any multilevel-inverter topology. The multi-objective function applied in the trade-off can be adjusted and modified to suit the main objectives of any considered case study. Some designers may be interested in minimizing power losses as a main objective. Others may aim to maximize the power factor as a priority. Yet others may seek minimal THD at the output. Based on the designer's objectives, the weighting average values of each single objective can be adopted.

6.2 Future Work

Proposed future work may consider the following:

- A further study could be undertaken as a continuation of this work, by applying the proposed optimisation trade-off model with different control techniques for the multilevel inverter. In such a study, the switching frequency might be considered a

variable parameter and included in the optimisation model, which can be solved using heuristic techniques.

- Wind and PV solar power plants are considered intermittent renewable energy sources, which have a highly variable output. Most of the time, these sources are not load-following, which limits the contribution of wind and PV solar in power generation. It is often stated that this problem can be solved by integration with energy storage. Further investigation is needed in this area, for example, by including energy storage in the trade-off optimisation for better integration of PV solar power plants. An in-depth technical and economic analysis of different energy-storage technologies may also be undertaken.
- Further interesting future research topics include applying different artificial intelligence techniques such as PSO, ANN, Neuro-Fuzzy, Expert Systems, Tabu Search, Simulated Annealing, Fuzzy Logic and so forth to optimize the problem of this trade-off. This is considered an improvement to the applied optimisation algorithms.

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APPENDIX A

MATLAB SCRIBTS AND SIMULINK MODELS

```
**************************************************************************
% This MATLAB code is for solving the problem of SHE using Newton-Raphson
% method in Cascaded H-Bridge MLI (7-LEVEL given as example)
% THE SWITCHING ANGLES SHOULD BE Θ1 < θ2 < θ3< 90°
**************************************************************************

clear all
% STEP (1): INITIAL GUESS OF SWITCHING ANGLES IN DEGREES (θ1, θ2 and θ3)

x=[20;30;50];

% The Value of Modulation index is (0.8)
mi= 0.8;
% The Newton-Raphson iterations starts here
del=1;
indx=0;

while del>1e-6 && indx<100

% STEP (2): FIND THE VALUE OF F (θ1, θ2, θ3)
F=[cosd(x(1))+cosd(x(2))+cosd(x(3))-3*mi;
   cosd(5*x(1))+cosd(5*x(2))+cosd(5*x(3));
   cosd(7*x(1))+cosd(7*x(2))+cosd(7*x(3));
   cosd(11*x(1))+cosd(11*x(2))+cosd(11*x(3))];

% STEP (2): FIND THE VALUE OF JACOBIAN JF (θ1, θ2, θ3, θ4)
JF=[-sind(x(1)) -sind(x(2)) -sind(x(3));
    -5*sind(5*x(1)) -5*sind(5*x(2)) -5*sind(5*x(3));
    -7*sind(7*x(1)) -7*sind(7*x(2)) -7*sind(7*x(3))];


% STEP (4): SOLVE FOR d(θ1, θ2, θ3)
delx = -inv(JF)*(F);

% NOTE THAT STEP(5) IS ALREADY DONE BY THE While Loop

% STEP (6): UPDATE THE VALUES OF (θ1, θ2, θ3 and θ4)
x=x+delx;
del=max(abs(F));
indx=indx+1;

end

% Print the Solution

 alpha=x;

'NEWTON-RAPHSON SOLUTION CONVERGES IN ITERATIONS',indx
'FINAL VALUES OF x in degrees ARE',alpha
```

```
**************************************************************************
% This MATLAB code is for solving the problem of SHE using Genetic Algorithm
% (GA) method in Cascaded H-Bridge MLI (7-LEVEL given as example)
% THE SWITCHING ANGLES SHOULD BE Θ1 < θ2 < θ3< 90°
**************************************************************************
clc
clear all
opts = gaoptimset(@gamultiobj);
opts.Generations=30;
opts.StallGenLimit=50;
opts.PlotFcns={@gaplotbestf,@gaplotdistance };
lb=[0,0, 0];
ub=[90,90,90];
[Q,Fval,exitFlag,Output] = ga(@THD_Mingab7,3,[],[],[], ...
  [],lb,ub,[],opts);
fprintf('\Switching_Angle_1 = ' ,X(1))
fprintf('\Switching_Angle_2 = ',X(2))
fprintf('\Switching_Angle_3 = ',X(3))
fprintf('Total Harmonic Distortion %THD =',THD)
```

```
function y = THD_Mingab7( x )

m=0.9;
H1 = cosd(x(1))+cosd(x(2))+cosd(x(3));

H= [1/5*(cosd(5*x(1))+cosd(5*x(2))+cosd(5*x(3)));
  1/7*(cosd(7*x(1))+cosd(7*x(2))+cosd(7*x(3)));
  1/11*(cosd(11*x(1))+cosd(11*x(2))+cosd(11*x(3)));
  1/13*(cosd(13*x(1))+cosd(13*x(2))+cosd(13*x(3)));
  1/17*(cosd(17*x(1))+cosd(17*x(2))+cosd(17*x(3)));
  1/19*(cosd(19*x(1))+cosd(19*x(2))+cosd(19*x(3)));
  1/23*(cosd(23*x(1))+cosd(23*x(2))+cosd(23*x(3)));
  1/25*(cosd(25*x(1))+cosd(25*x(2))+cosd(25*x(3)));
  1/29*(cosd(29*x(1))+cosd(29*x(2))+cosd(29*x(3)));
  1/31*(cosd(31*x(1))+cosd(31*x(2))+cosd(31*x(3)));
  1/35*(cosd(35*x(1))+cosd(35*x(2))+cosd(35*x(3)));
  1/37*(cosd(37*x(1))+cosd(37*x(2))+cosd(37*x(3)));
  1/41*(cosd(41*x(1))+cosd(41*x(2))+cosd(41*x(3)));
  1/43*(cosd(43*x(1))+cosd(43*x(2))+cosd(43*x(3)));
  1/47*(cosd(47*x(1))+cosd(47*x(2))+cosd(47*x(3)));
  1/49*(cosd(49*x(1))+cosd(49*x(2))+cosd(49*x(3)))];

HH = H.^2;
HN = sum(HH);
THD = sqrt(HN)/H1*100;
'Total Harmonic Distortion %THD =', THD
'Fundamental', H1-3*m
'5th harmonic =', H(1,1)/H1*100
'7th harmonic =', H(2,1)/H1*100

y = 50*((H1-3*m)^4)+50*(H(1,1)^2+ H(2,1)^2)+THD/100 ;

end
```

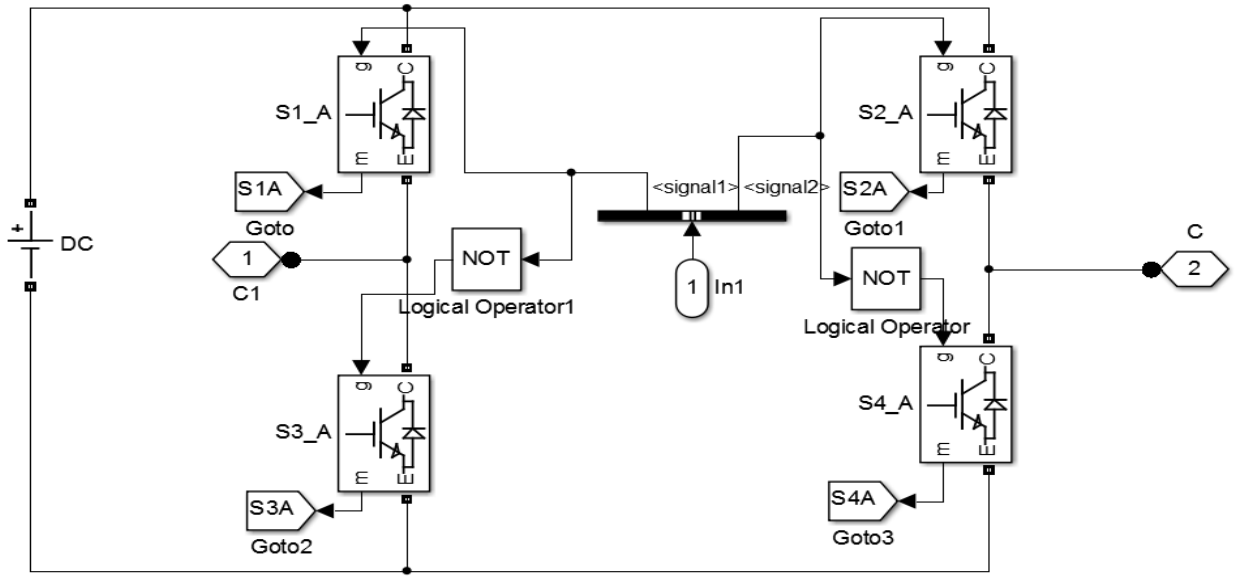

Figure A.1: Simulink block model for single H-Bridge circuit

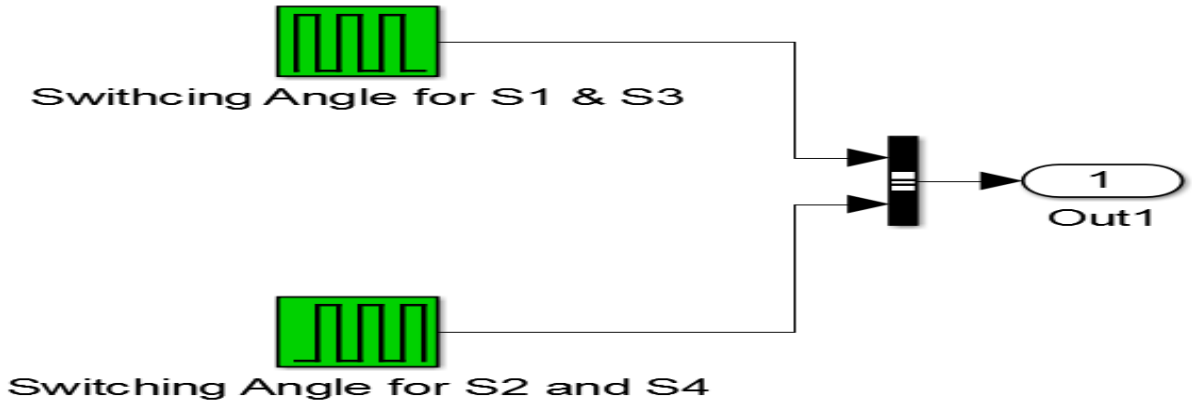

Figure A.2: Repeating sequence block applied to generates switching angles

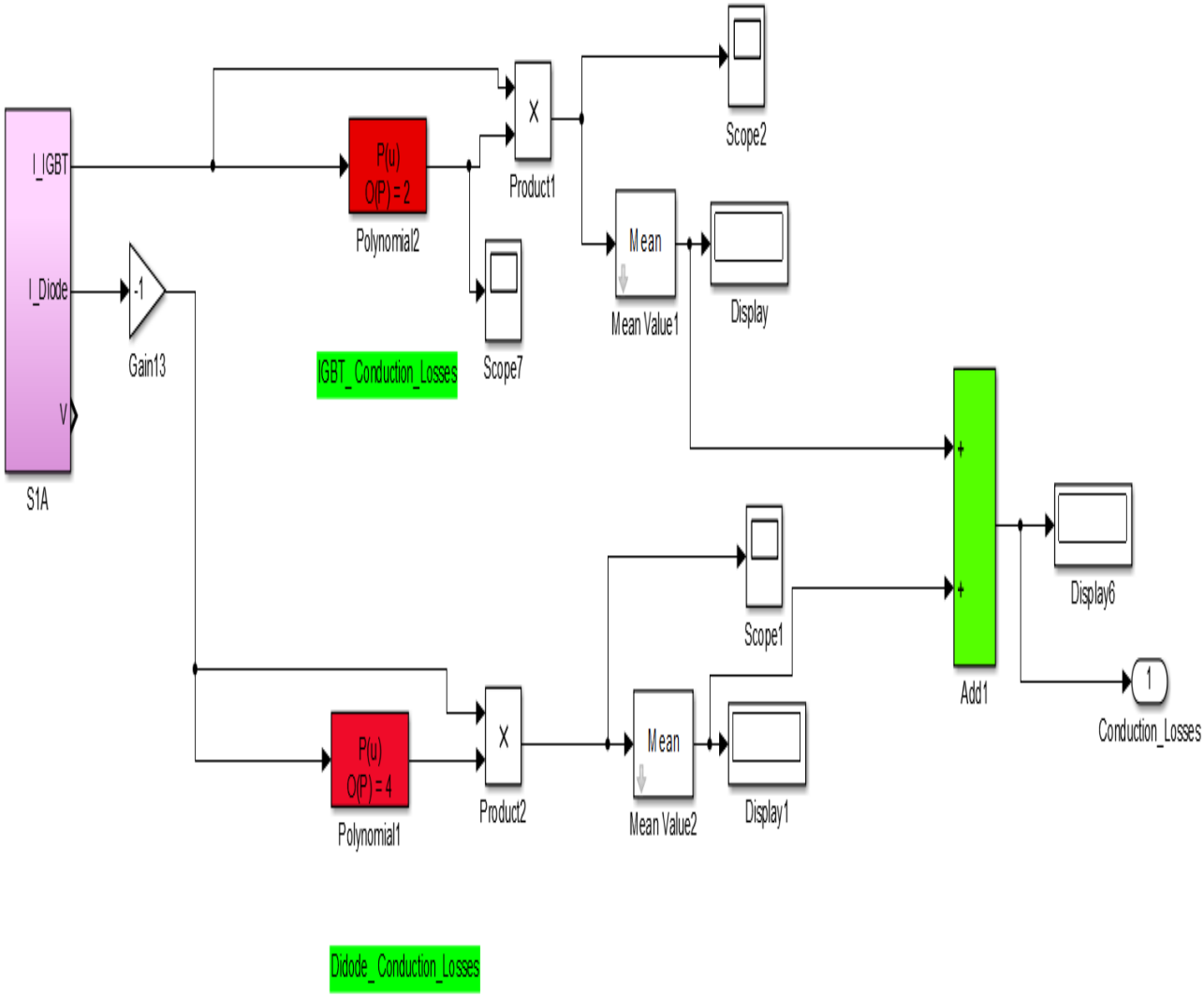

Figure A.3: Simulink block for conduction losses calculation for a single switch

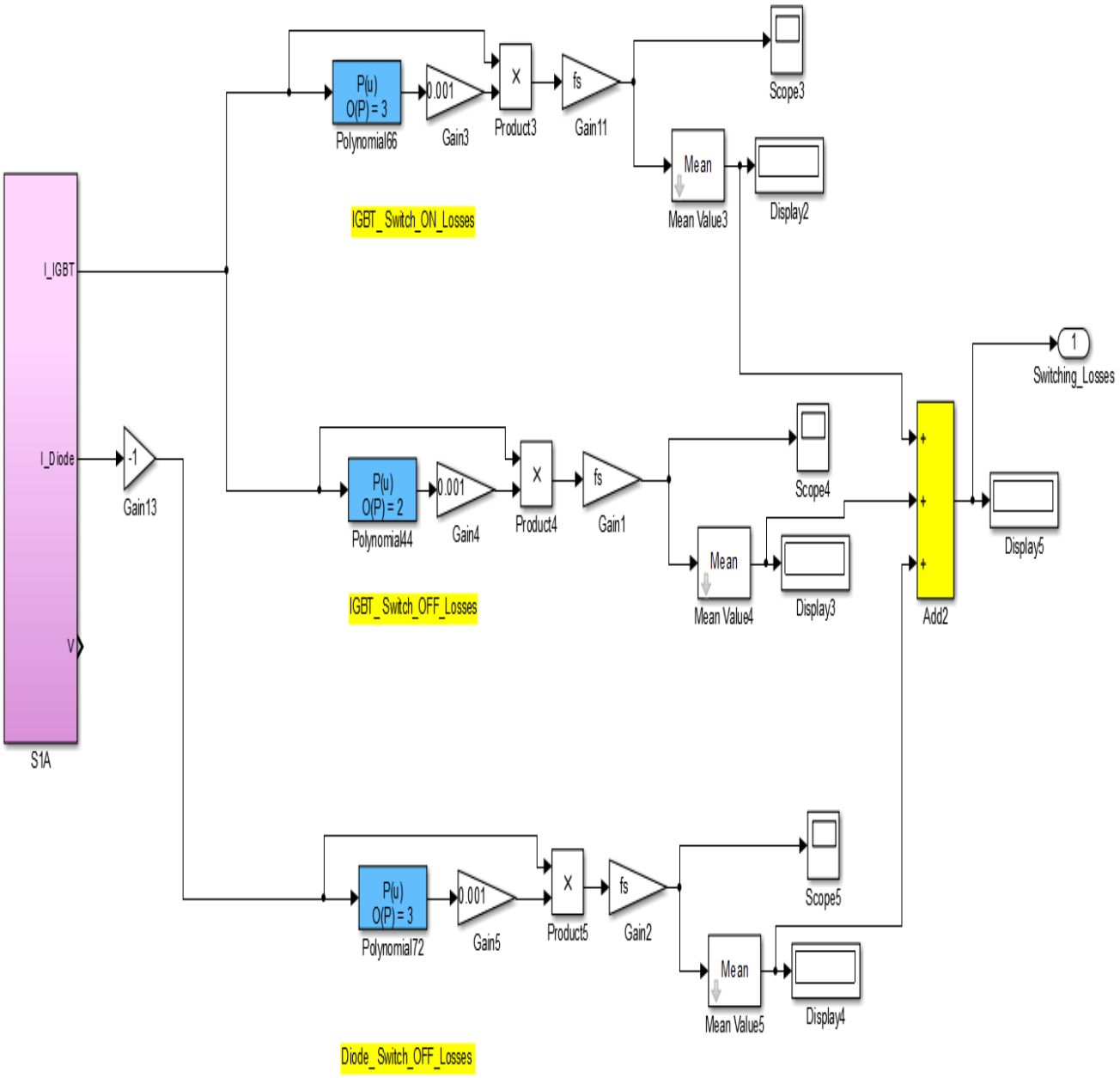

Figure A.4: Simulink block for switching losses calculation for a single switch

```
**************************************************************************
% This MATLAB code is for the optimum design of passive power filter (PPF)
% using Genetic Algorithm (GA) method in Cascaded H-Bridge MLI (7-LEVEL)
% Two single tuned filter and one high pass filter
**************************************************************************

clc
clear all
opts = gaoptimset(@gamultiobj);
opts.Generations=10;
opts.StallGenLimit=50;
opts.PlotFcns={@gaplotbestf,@gaplotdistance };
lb=[300000,300000, 1000000];
ub=[1500000,1500000, 3000000];
 [Q,Fval,exitFlag,Output] = ga(@Q_7_level_inverter,3,[],[],[], ...
  [],lb,ub,[],opts);

fprintf('\nDesigned Parameter Q1= %f',Q(1))
fprintf('\nDesigned Parameter Q1= %f',Q(2))
fprintf('\nDesigned Parameter Q1= %f',Q(3))
fprintf('\nSum of designed parameters Q= %f',Q(1)+Q(2)+Q(3))
fprintf('     1.6<%f<3.75',Q(1)+Q(2)+Q(3))
fprintf('\nTHD= %f \n',THD.THD)
```

```
function [Q ] = Q_7_level_inverter(Q)

assignin('base', 'Q1', Q(1));
assignin('base', 'Q2',Q(2));
assignin('base', 'Q3', Q(3));
sim('Seven_Level_CHB__Inverter_07')
pause(0.5);
assignin('base', 'Ploss', ploss);
f1=[(Q(1)+Q(2)+Q(3))*(1/100)]+[[(max(ploss.Data)/1000)*4380*0.11]*[(((1.05)^1
5)-1)/(0.05*((1.05)^15))]];
assignin('base', 'VLL', VLL);
THD=power_fftscope(VLL);
THD.fundamental=50;
THD.maxFrequency=2500;
THD.startTime=0.01;
THD=power_fftscope(THD);
f2=THD.THD;
f3= 100-[(Q(1)+Q(2)+Q(3))/1000000];
assignin('base', 'THD', THD);
end
```

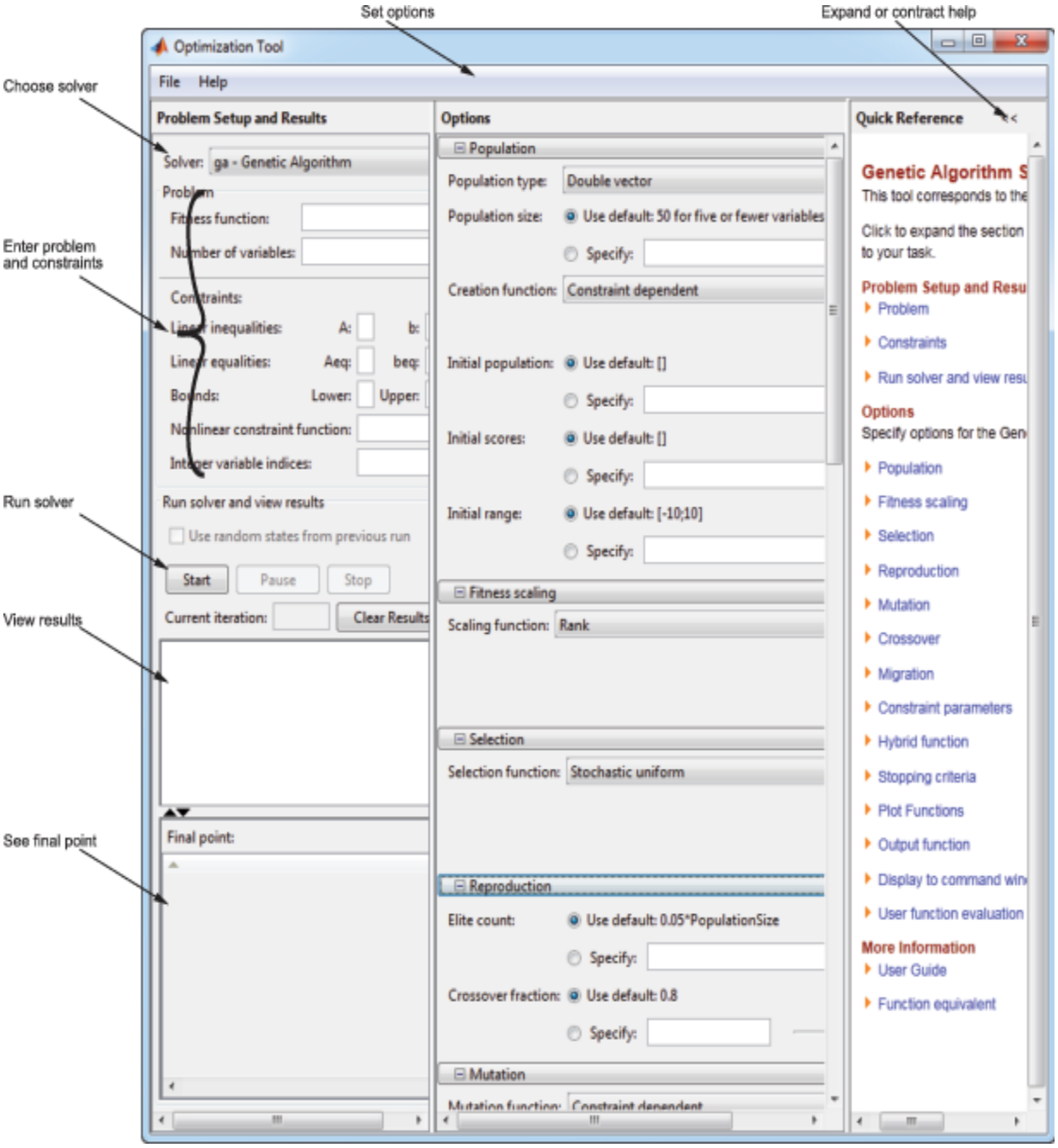

Figure A.5: MATLAB genetic algorithm tool

APPENDIX B

HIGH VOLTAGE IGBT DEVICES DATA SHEETS

Technische Information / Technical Information

IGBT-Module
IGBT-modules

FZ400R17KE3

62mm C-Serien Modul mit Trench/Feldstop IGBT³ und Emitter Controlled³ Diode
62mm C-series module with trench/fieldstop IGBT³ and Emitter Controlled³ diode

Vorläufige Daten
Preliminary Data

IGBT,Wechselrichter / IGBT,Inverter

Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 25°C	V_{CES}	1700	V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 80°C, $T_{vj\,max}$ = 150°C T_C = 25°C, $T_{vj\,max}$ = 150°C	$I_{C\,nom}$ I_C	400 620	A A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	800	A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, $T_{vj\,max}$ = 150	P_{tot}	2250	W
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage		V_{GES}	+/-20	V

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	I_C = 400 A, V_{GE} = 15 V I_C = 400 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C	$V_{CE\,sat}$		2,00 2,40	2,45	V V
Gate-Schwellenspannung Gate threshold voltage	I_C = 16,0 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	5,2	5,8	6,4	V
Gateladung Gate charge	V_{GE} = -15 V ... +15 V		Q_G		4,60		µC
Interner Gatewiderstand Internal gate resistor	T_{vj} = 25°C		R_{Gint}		1,9		Ω
Eingangskapazität Input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		36,0		nF
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		1,20		nF
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V_{CE} = 1700 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			3,0	mA
Gate-Emitter-Reststrom Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	I_C = 400 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Gon} = 3,6 Ω	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,on}$		0,28 0,30		µs µs
Anstiegszeit, induktive Last Rise time, inductive load	I_C = 400 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Gon} = 3,6 Ω	T_{vj} = 25°C T_{vj} = 125°C	t_r		0,08 0,10		µs µs
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	I_C = 400 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Goff} = 3,6 Ω	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,off}$		0,80 1,00		µs µs
Fallzeit, induktive Last Fall time, inductive load	I_C = 400 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Goff} = 3,6 Ω	T_{vj} = 25°C T_{vj} = 125°C	t_f		0,12 0,20		µs µs
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 400 A, V_{CE} = 900 V, L_S = 60 nH V_{GE} = ±15 V R_{Gon} = 3,6 Ω	T_{vj} = 25°C T_{vj} = 125°C	E_{on}		105 135		mJ mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 400 A, V_{CE} = 900 V, L_S = 60 nH V_{GE} = ±15 V R_{Goff} = 3,6 Ω	T_{vj} = 25°C T_{vj} = 125°C	E_{off}		85,0 125		mJ mJ
Kurzschlußverhalten SC data	V_{GE} ≤ 15 V, V_{CC} = 1000 V V_{CEmax} = V_{CES} -L_{sCE} ·di/dt	t_P ≤ 10 µs, T_{vj} = 125°C	I_{SC}		1600		A
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}			0,055	K/W
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,017		K/W
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		125	°C

prepared by: HS	date of publication: 2013-10-03
approved by: WR	revision: 2.2

Technische Information / Technical Information

IGBT-Module
IGBT-modules

FZ400R17KE3

Vorläufige Daten
Preliminary Data

Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	1700	V
Dauergleichstrom Continuous DC forward current		I_F	400	A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	800	A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I²t	25500	A²s

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Durchlassspannung Forward voltage	I_F = 400 A, V_{GE} = 0 V I_F = 400 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C	V_F		1,80 1,90	2,20	V V
Rückstromspitze Peak reverse recovery current	I_F = 400 A, - di_F/dt = 4250 A/µs (T_{vj}=125°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	I_{RM}		440 480		A A
Sperrverzögerungsladung Recovered charge	I_F = 400 A, - di_F/dt = 4250 A/µs (T_{vj}=125°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	Q_r		100 170		µC µC
Abschaltenergie pro Puls Reverse recovery energy	I_F = 400 A, - di_F/dt = 4250 A/µs (T_{vj}=125°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	E_{rec}		54,0 96,0		mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			0,08	K/W
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		0,025		K/W
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		125	°C

prepared by: HS	date of publication: 2013-10-03
approved by: WR	revision: 2.2

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IGBT-Module
IGBT-modules

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Vorläufige Daten
Preliminary Data

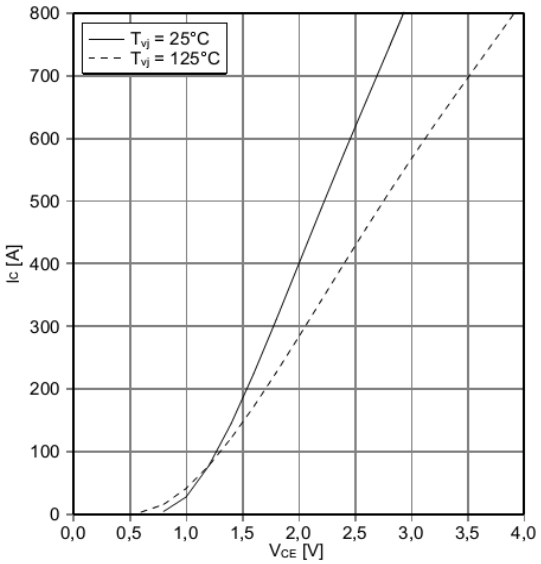
Modul / Module

Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		3,4		kV
Material Modulgrundplatte Material of module baseplate				Cu		
Innere Isolation Internal isolation	Basisisolierung (Schutzklasse 1, EN61140) basic insulation (class 1, IEC 61140)			Al_2O_3		
Kriechstrecke Creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			25,0 19,0		mm
Luftstrecke Clearance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			25,0 10,0		mm
Vergleichszahl der Kriechwegbildung Comperative tracking index		CTI		> 400		
			min.	typ.	max.	
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Modul / per module λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,01		K/W
Modulstreuinduktivität Stray inductance module		L_{sCE}		16		nH
Modulleitungswiderstand, Anschlüsse - Chip Module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		0,50		mΩ
Lagertemperatur Storage temperature		T_{stg}	-40		125	°C
Anzugsdrehmoment f. Modulmontage Mounting torque for modul mounting	Schraube M6 - Montage gem. gültiger Applikationsschrift Screw M6 - Mounting according to valid application note	M	3,00	-	6,00	Nm
Anzugsdrehmoment f. elektr. Anschlüsse Terminal connection torque	Schraube M4 - Montage gem. gültiger Applikationsschrift Screw M4 - Mounting according to valid application note Schraube M6 - Montage gem. gültiger Applikationsschrift Screw M6 - Mounting according to valid application note	M	1,1 2,5	- -	2,0 5,0	Nm Nm
Gewicht Weight		G		340		g

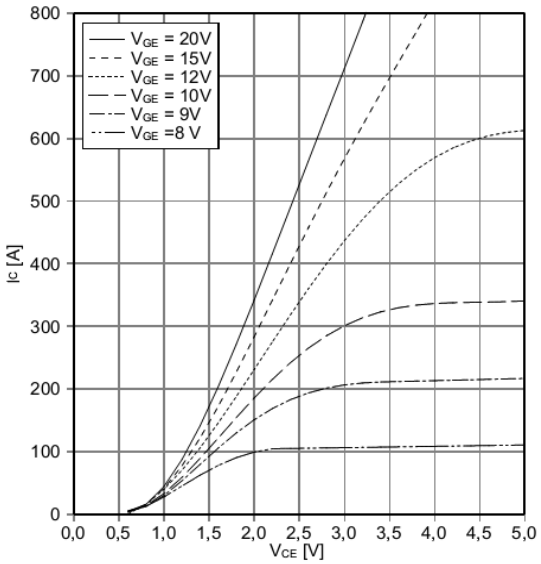
prepared by: HS	date of publication: 2013-10-03
approved by: WR	revision: 2.2

Vorläufige Daten
Preliminary Data

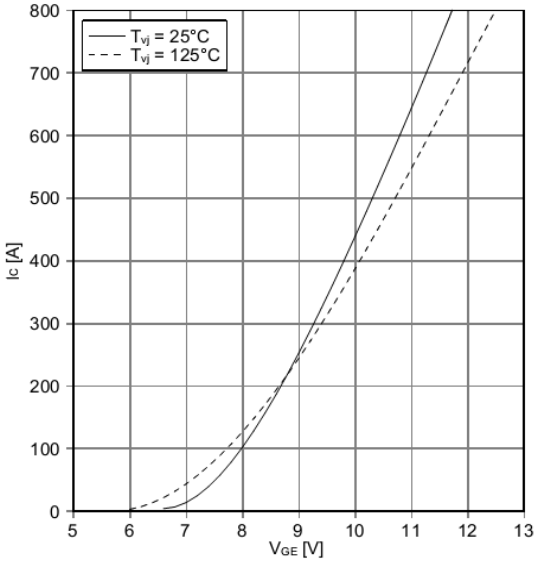
Ausgangskennlinie IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
V_{GE} = 15 V



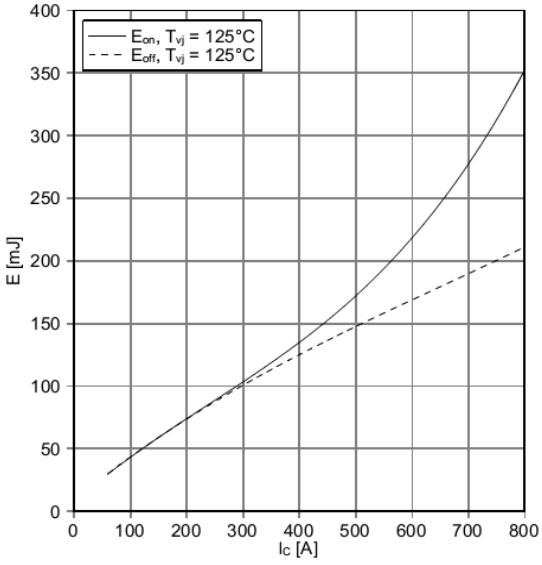
Ausgangskennlinienfeld IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
T_{vj} = 125°C



Übertragungscharakteristik IGBT,Wechselrichter (typisch)
transfer characteristic IGBT,Inverter(typical)
$I_C = f(V_{GE})$
V_{CE} = 20 V



SchaltverlustelGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
V_{GE} = ±15 V, R_{Gon} = 3.6 Ω, R_{Goff} = 3.6 Ω, V_{CE} = 900 V



prepared by: HS	date of publication: 2013-10-03
approved by: WR	revision: 2.2

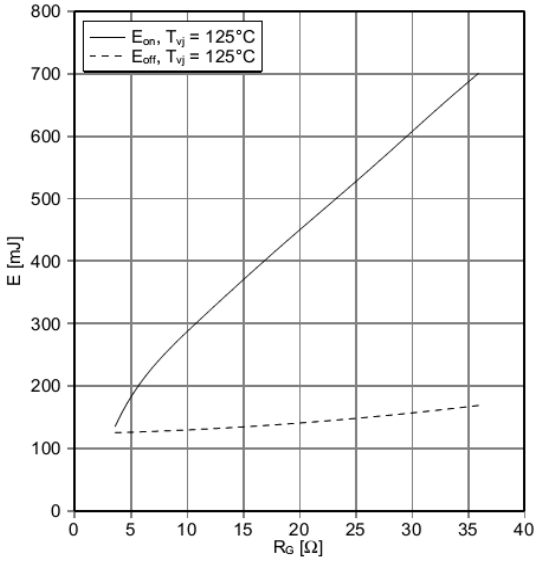
Technische Information / Technical Information

IGBT-Module
IGBT-modules

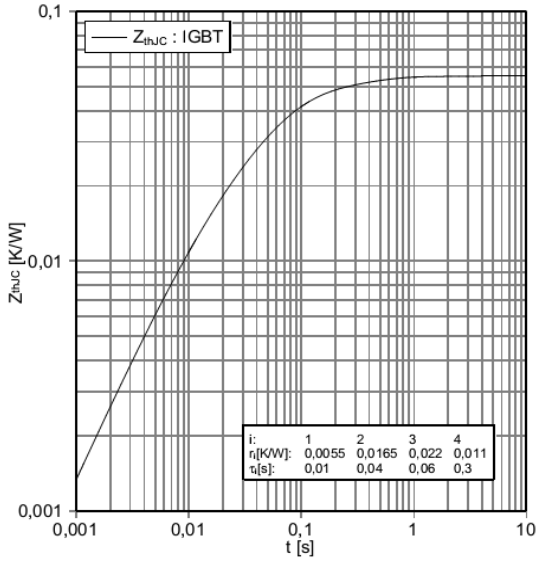
FZ400R17KE3

Vorläufige Daten
Preliminary Data

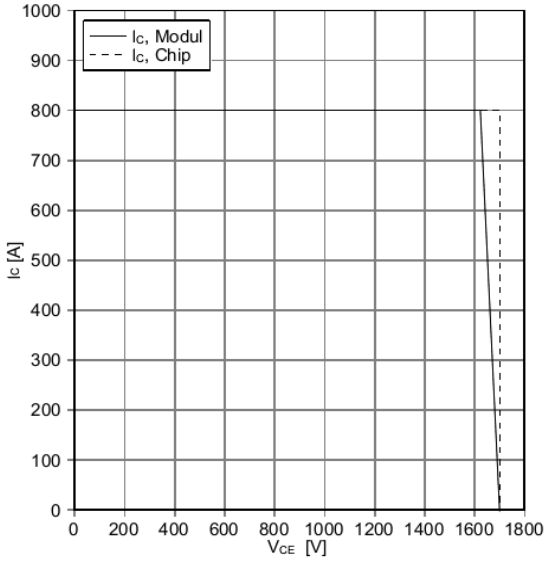
SchaltverlustelGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
V_{GE} = ±15 V, I_C = 400 A, V_{CE} = 900 V



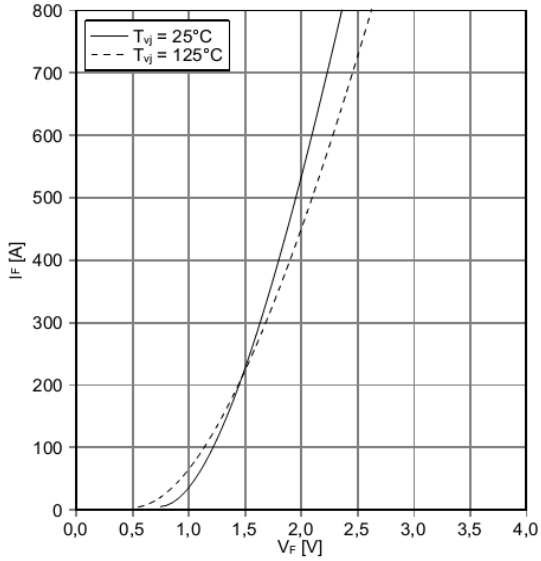
Transienter Wärmewiderstand IGBT,Wechselrichter
transient thermal impedance IGBT,Inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT,Wechselrichter (RBSOA)
reverse bias safe operating area IGBT,Inverter (RBSOA)
$I_C = f(V_{CE})$
V_{GE} = ±15 V, R_{Goff} = 3.6 Ω, T_{vj} = 125°C



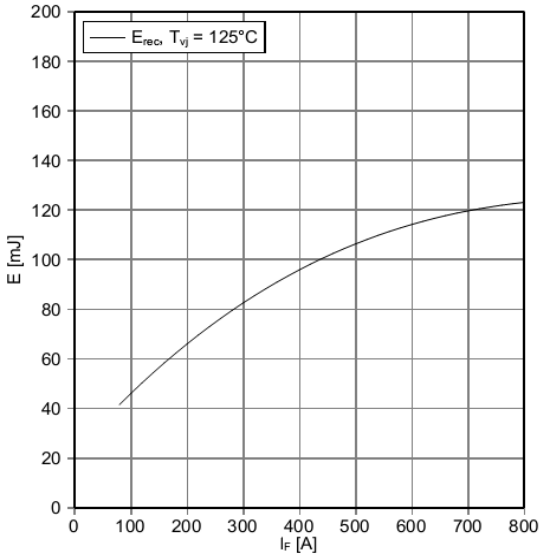
Durchlasskennlinie der Diode, Wechselrichter (typisch)
forward characteristic of Diode, Inverter (typical)
$I_F = f(V_F)$



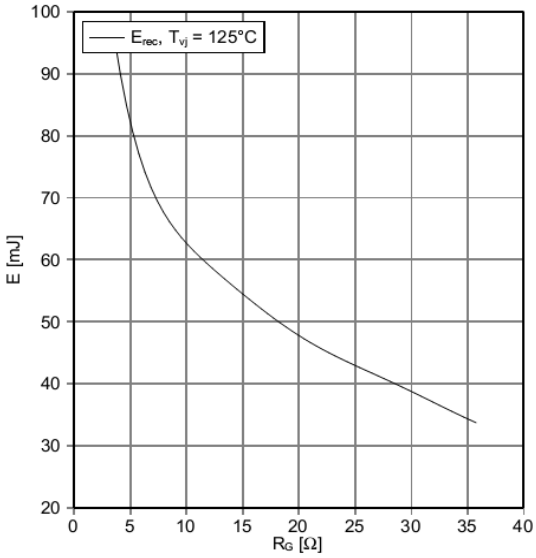
prepared by: HS	date of publication: 2013-10-03
approved by: WR	revision: 2.2

Vorläufige Daten
Preliminary Data

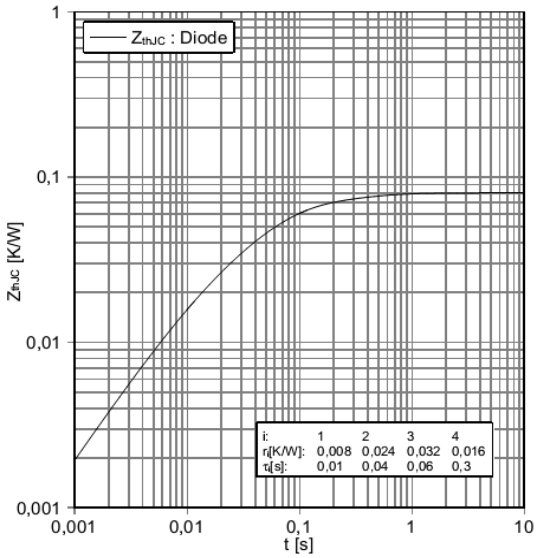
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 3.6\ \Omega$, $V_{CE} = 900$ V



Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 400$ A, $V_{CE} = 900$ V



Transienter Wärmewiderstand Diode, Wechselrichter
transient thermal impedance Diode, Inverter
$Z_{thJC} = f(t)$



prepared by: HS	date of publication: 2013-10-03
approved by: WR	revision: 2.2

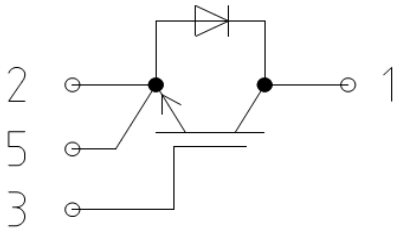
Technische Information / Technical Information

IGBT-Module
IGBT-modules

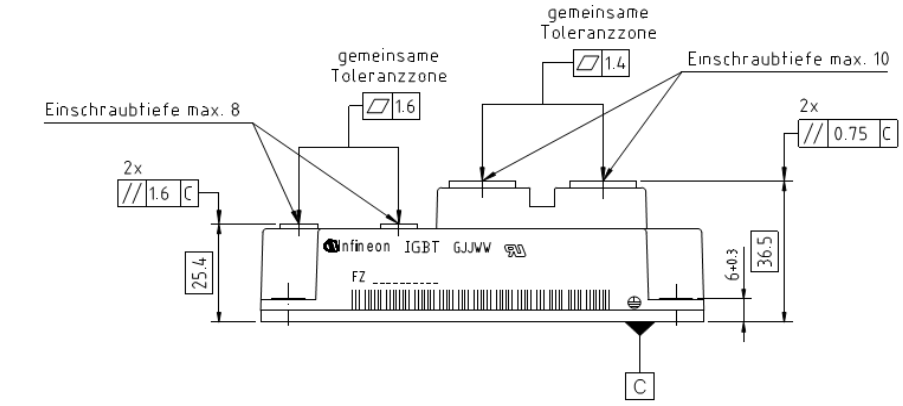
FZ400R17KE3

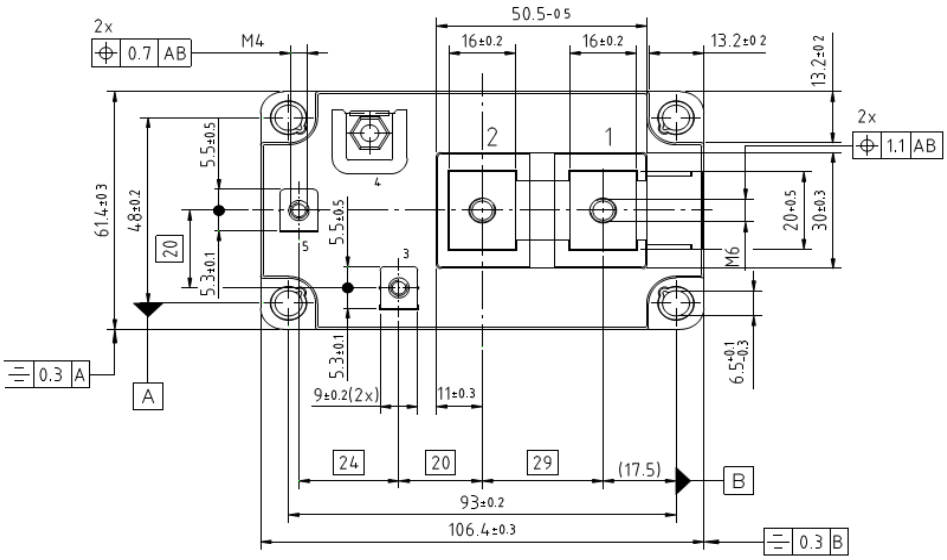
Vorläufige Daten
Preliminary Data

Schaltplan / circuit_diagram_headline



Gehäuseabmessungen / package outlines





prepared by: HS	date of publication: 2013-10-03
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Technische Information / Technical Information

IGBT-Module
IGBT-modules

FZ400R17KE3

Vorläufige Daten
Preliminary Data

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- the conclusion of Quality Agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery depended on the realization of any such measures.

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prepared by: HS	date of publication: 2013-10-03
approved by: WR	revision: 2.2

MITSUBISHI HVIGBT MODULES

CM400DY-50H

HIGH POWER SWITCHING USE
INSULATED TYPE

HVIGBT (High Voltage Insulated Gate Bipolar Transistor) Modules

CM400DY-50H

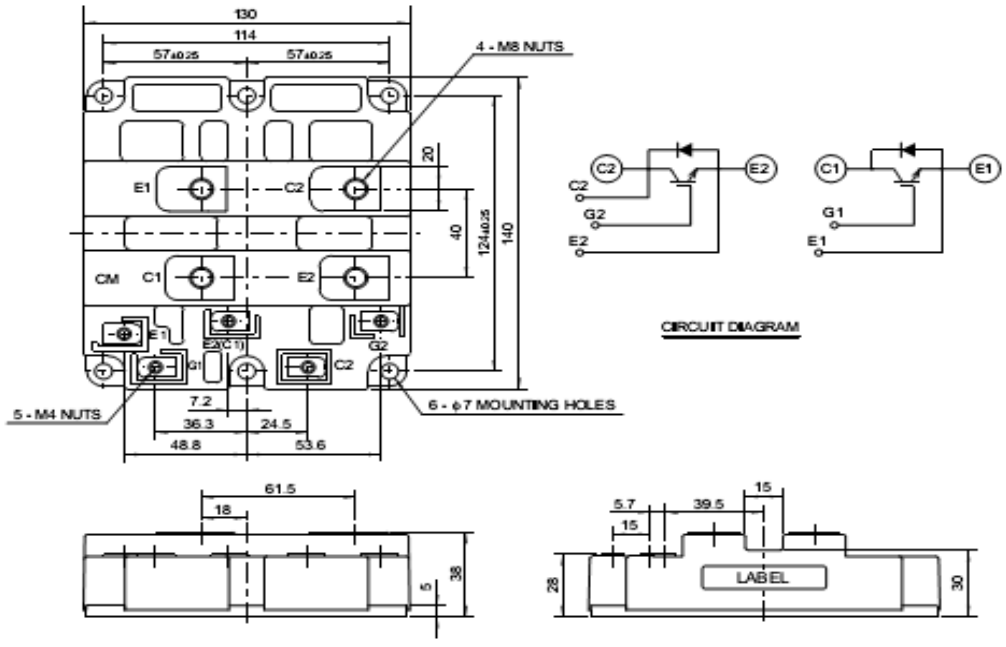
- IC 400A
- VCES 2500V
- Insulated Type
- 2-elements in a pack

APPLICATION

Inverters, Converters, DC choppers, Induction heating, DC to DC converters.

OUTLINE DRAWING & CIRCUIT DIAGRAM

Dimensions in mm



Mar. 2003

MITSUBISHI ELECTRIC

MITSUBISHI HVIGBT MODULES

CM400DY-50H

HIGH POWER SWITCHING USE
INSULATED TYPE

HVIGBT (High Voltage Insulated Gate Bipolar Transistor) Modules

MAXIMUM RATINGS (T_j = 25°C)

Symbol	Item	Conditions	Ratings	Unit
V_{CES}	Collector-emitter voltage	V_{GE} = 0V	2500	V
V_{GES}	Gate-emitter voltage	V_{CE} = 0V	±20	V
I_C	Collector current	DC, T_C = 80°C	400	A
I_{CM}		Pulse (Note 1)	800	A
I_E (Note 2)	Emitter current		400	A
I_{EM} (Note 2)		Pulse (Note 1)	800	A
P_C (Note 3)	Maximum collector dissipation	T_C = 25°C, IGBT part	3400	W
T_j	Junction temperature	—	−40 ~ +150	°C
T_{stg}	Storage temperature	—	−40 ~ +125	°C
V_{iso}	Isolation voltage	Charged part to base plate, rms, sinusoidal, AC 60Hz 1min.	6000	V
—	Mounting torque	Main terminals screw M8	6.67 ~ 13.00	N·m
		Mounting screw M6	2.84 ~ 6.00	N·m
		Auxiliary terminals screw M4	0.88 ~ 2.00	N·m
—	Mass	Typical value	1.5	kg

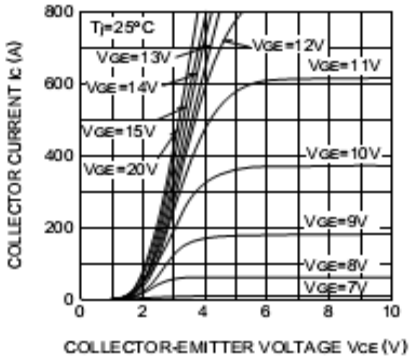
ELECTRICAL CHARACTERISTICS (T_j = 25°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I_{CES}	Collector cutoff current	V_{CE} = V_{CES}, V_{GE} = 0V	—	—	5	mA
$V_{GE(th)}$	Gate-emitter threshold voltage	I_C = 40mA, V_{CE} = 10V	4.5	6.0	7.5	V
I_{GES}	Gate-leakage current	V_{GE} = V_{GES}, V_{CE} = 0V	—	—	0.5	µA
$V_{CE(sat)}$	Collector-emitter saturation voltage	T_j = 25°C; I_C = 400A, V_{GE} = 15V (Note 4)	—	3.20	4.16	V
		T_j = 125°C; I_C = 400A, V_{GE} = 15V (Note 4)	—	3.60	—	V
C_{ies}	Input capacitance	V_{CE} = 10V, V_{GE} = 0V	—	40	—	nF
C_{oes}	Output capacitance		—	4.4	—	nF
C_{res}	Reverse transfer capacitance		—	1.3	—	nF
Q_G	Total gate charge	V_{CC} = 1250V, I_C = 400A, V_{GE} = 15V	—	1.8	—	µC
$t_{d(on)}$	Turn-on delay time	V_{CC} = 1250V, I_C = 400A	—	—	1.00	µs
t_r	Turn-on rise time	V_{GE1} = V_{GE2} = 15V	—	—	2.00	µs
$t_{d(off)}$	Turn-off delay time	R_G = 7.5Ω	—	—	2.00	µs
t_f	Turn-off fall time	Resistive load switching operation	—	—	1.00	µs
V_{EC} (Note 2)	Emitter-collector voltage	I_E = 400A, V_{GE} = 0V	—	2.90	3.77	V
t_{rr} (Note 2)	Reverse recovery time	I_E = 400A	—	—	1.20	µs
Q_{rr} (Note 2)	Reverse recovery charge	die / dt = −800A / µs	—	85	—	µC
$R_{th(j-c)Q}$	Thermal resistance	Junction to case, IGBT part (Per 1/2 module)	—	—	0.036	K/W
$R_{th(j-c)R}$		Junction to case, FWDi part (Per 1/2 module)	—	—	0.072	K/W
$R_{th(c-f)}$	Contact thermal resistance	Case to fin, conductive grease applied (Per 1/2 module)	—	0.016	—	K/W

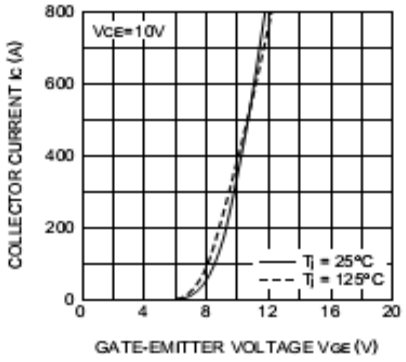
Note 1. Pulse width and repetition rate should be such that the device junction temp. (T_j) does not exceed T_{jmax} rating.
2. I_E, V_{EC}, t_{rr}, Q_{rr} & die/dt represent characteristics of the anti-parallel, emitter to collector free-wheel diode.
3. Junction temperature (T_j) should not increase beyond 150°C.
4. Pulse width and repetition rate should be such as to cause negligible temperature rise.

PERFORMANCE CURVES

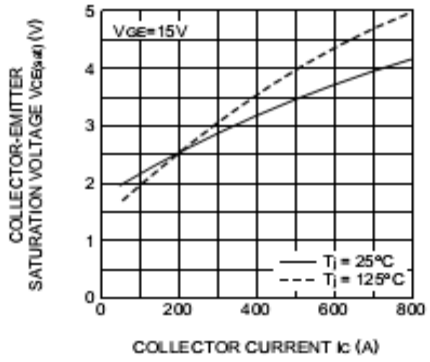
OUTPUT CHARACTERISTICS (TYPICAL)



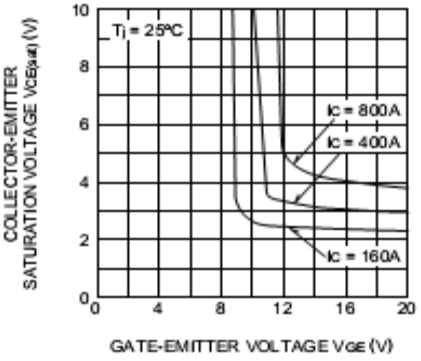
TRANSFER CHARACTERISTICS (TYPICAL)



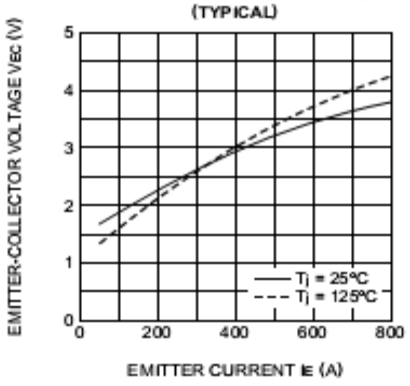
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



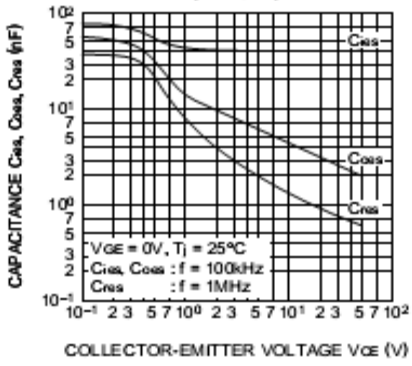
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



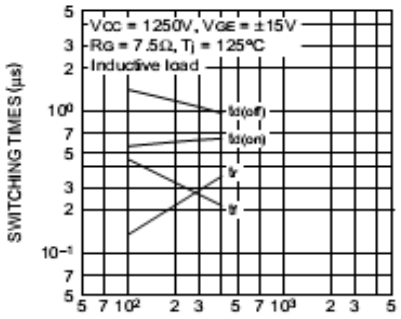
FREE-WHEEL DIODE FORWARD CHARACTERISTICS (TYPICAL)



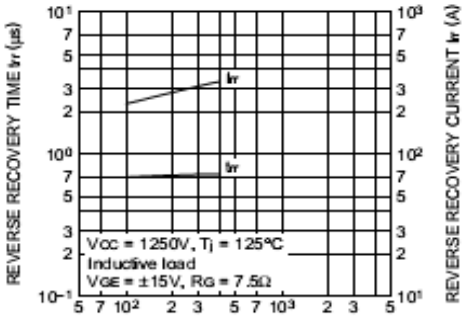
CAPACITANCE CHARACTERISTICS (TYPICAL)



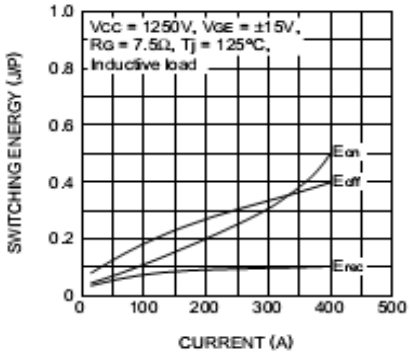
HALF-BRIDGE
SWITCHING TIME CHARACTERISTICS
(TYPICAL)



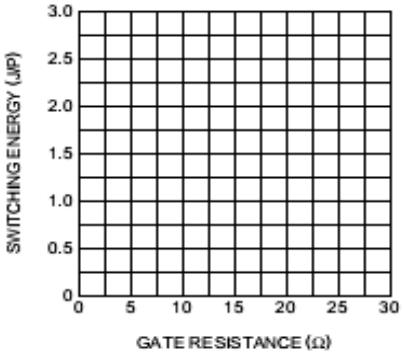
REVERSE RECOVERY CHARACTERISTICS
OF FREE-WHEEL DIODE
(TYPICAL)



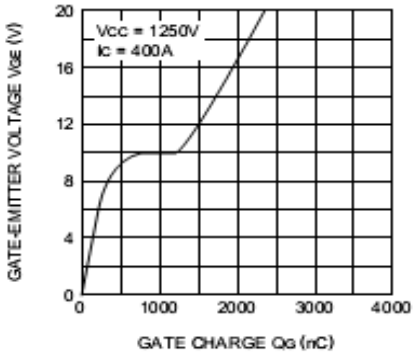
HALF-BRIDGE
SWITCHING ENERGY CHARACTERISTICS
(TYPICAL)



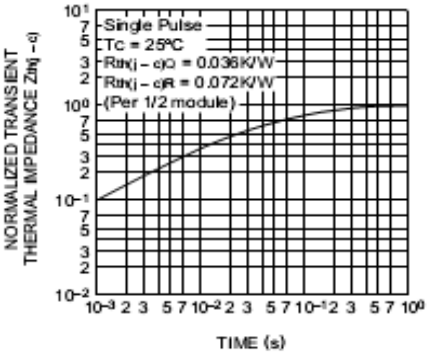
HALF-BRIDGE
SWITCHING ENERGY CHARACTERISTICS
(TYPICAL)



GATE CHARGE CHARACTERISTICS
(TYPICAL)



TRANSIENT THERMAL
IMPEDANCE CHARACTERISTICS



Technische Information / Technical Information

IGBT-Module
IGBT-modules

FZ400R33KL2C_B5

Vorläufige Daten
Preliminary Data

IGBT,Wechselrichter / IGBT,Inverter

Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 25°C T_{vj} = -25°C	V_{CES}	3300 3300	V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 80°C, $T_{vj\,max}$ = 150°C T_C = 25°C, $T_{vj\,max}$ = 150°C	$I_{C\,nom}$ I_C	400 750	A A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	800	A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, $T_{vj\,max}$ = 150	P_{tot}	4,90	kW
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage		V_{GES}	+/-20	V

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	I_C = 400 A, V_{GE} = 15 V I_C = 400 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C	$V_{CE\,sat}$		3,00 3,70	3,65 4,45	V V
Gate-Schwellenspannung Gate threshold voltage	I_C = 40,0 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	4,2	5,1	6,0	V
Gateladung Gate charge	V_{GE} = -15 V ... +15 V, V_{CE} = 1800V		Q_G		7,50		µC
Interner Gatewiderstand Internal gate resistor	T_{vj} = 25°C		R_{Gint}		1,3		Ω
Eingangskapazität Input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		48,0		nF
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		2,70		nF
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V_{CE} = 3300 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			5,0	mA
Gate-Emitter-Reststrom Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	I_C = 400 A, V_{CE} = 1800 V V_{GE} = ±15 V R_{Gon} = 13 Ω, C_{GE} = 100 nF	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,on}$		1,00 1,00		µs µs
Anstiegszeit, induktive Last Rise time, inductive load	I_C = 400 A, V_{CE} = 1800 V V_{GE} = ±15 V R_{Gon} = 13 Ω, C_{GE} = 100 nF	T_{vj} = 25°C T_{vj} = 125°C	t_r		0,40 0,40		µs µs
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	I_C = 400 A, V_{CE} = 1800 V V_{GE} = ±15 V R_{Goff} = 13 Ω, C_{GE} = 100 nF	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,off}$		3,70 3,90		µs µs
Fallzeit, induktive Last Fall time, inductive load	I_C = 400 A, V_{CE} = 1800 V V_{GE} = ±15 V R_{Goff} = 13 Ω, C_{GE} = 100 nF	T_{vj} = 25°C T_{vj} = 125°C	t_f		0,25 0,35		µs µs
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 400 A, V_{CE} = 1800 V, L_S = 60 nH V_{GE} = ±15 V, di/dt = 3000 A/µs R_{Gon} = 6,2 Ω, C_{GE} = 100 nF	T_{vj} = 25°C T_{vj} = 125°C	E_{on}		900 1200		mJ mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 400 A, V_{CE} = 1800 V, L_S = 60 nH V_{GE} = ±15 V R_{Goff} = 13 Ω, C_{GE} = 100 nF	T_{vj} = 25°C T_{vj} = 125°C	E_{off}		440 600		mJ mJ
Kurzschlußverhalten SC data	V_{GE} ≤ 15 V, V_{CC} = 2500 V V_{CEmax} = V_{CES} -L_{sCE} ·di/dt	t_P ≤ 10 µs, T_{vj} = 125°C	I_{SC}		1800		A
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}			25,5	K/kW
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		24,0		K/kW
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		125	°C

prepared by: KHH	date of publication: 2013-10-03
approved by: TS	revision: 2.0

Technische Information / Technical Information

IGBT-Module
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Vorläufige Daten
Preliminary Data

Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 25°C T_{vj} = -25°C	V_{RRM}	3300 3300	V
Dauergleichstrom Continuous DC forward current		I_F	400	A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	800	A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I²t	72,0	kA²s
Spitzenverlustleistung Maximum power dissipation	T_{vj} = 125°C	P_{RQM}	600	kW
Mindesteinschaltdauer Minimum turn-on time		$t_{on\ min}$	10,0	µs

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Durchlassspannung Forward voltage	I_F = 400 A, V_{GE} = 0 V I_F = 400 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C	V_F		2,60 2,55	t.b.d.	V V
Rückstromspitze Peak reverse recovery current	I_F = 400 A, - di_F/dt = 3000 A/µs (T_{vj}=125°C) V_R = 1800 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	I_{RM}		600 670		A A
Sperrverzögerungsladung Recovered charge	I_F = 400 A, - di_F/dt = 3000 A/µs (T_{vj}=125°C) V_R = 1800 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	Q_r		270 480		µC µC
Abschaltenergie pro Puls Reverse recovery energy	I_F = 400 A, - di_F/dt = 3000 A/µs (T_{vj}=125°C) V_R = 1800 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	E_{rec}		250 500		mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			51,0	K/kW
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		48,0		K/kW
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\ op}$	-40		125	°C

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Vorläufige Daten
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Modul / Module

Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		10,2		kV
Teilentladungs-Aussetzspannung Partial discharge extinction voltage	RMS, f = 50 Hz, Q_{PD} typ 10 pC (acc. to IEC 1287)	V_{ISOL}		5,1		kV
Kollektor-Emitter-Gleichsperrspannung DC stability	T_{vj} = 25°C, 100 fit	$V_{CE\,D}$		2150		V
Material Modulgrundplatte Material of module baseplate				AlSiC		
Innere Isolation Internal isolation	Basisisolierung (Schutzklasse 1, EN61140) basic insulation (class 1, IEC 61140)			AlN		
Kriechstrecke Creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			64,0 56,0		mm
Luftstrecke Clearance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			40,0 26,0		mm
Vergleichszahl der Kriechwegbildung Comperative tracking index		CTI		> 600		
			min.	typ.	max.	
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Modul / per module λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		16,0		K/kW
Modulstreuinduktivität Stray inductance module		L_{sCE}		25		nH
Modulleitungswiderstand, Anschlüsse - Chip Module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		0,37		mΩ
Lagertemperatur Storage temperature		T_{stg}	-40		125	°C
Anzugsdrehmoment f. Modulmontage Mounting torque for modul mounting	Schraube M6 - Montage gem. gültiger Applikationsschrift Screw M6 - Mounting according to valid application note	M	4,25	-	5,75	Nm
Anzugsdrehmoment f. elektr. Anschlüsse Terminal connection torque	Schraube M8 - Montage gem. gültiger Applikationsschrift Screw M8 - Mounting according to valid application note	M	8,0	-	10	Nm
Gewicht Weight		G		500		g

prepared by: KHH	date of publication: 2013-10-03
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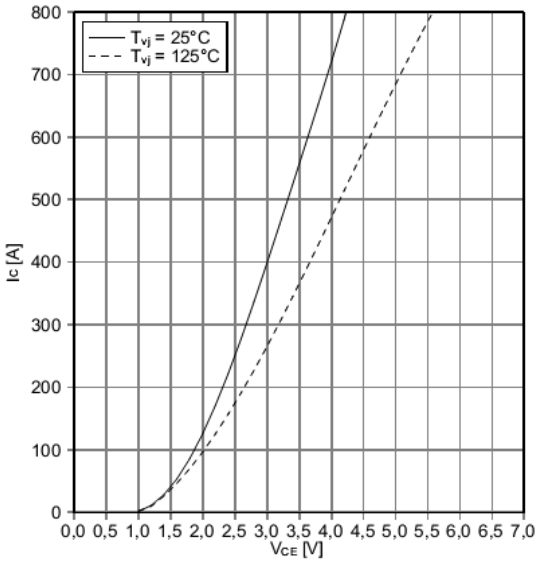
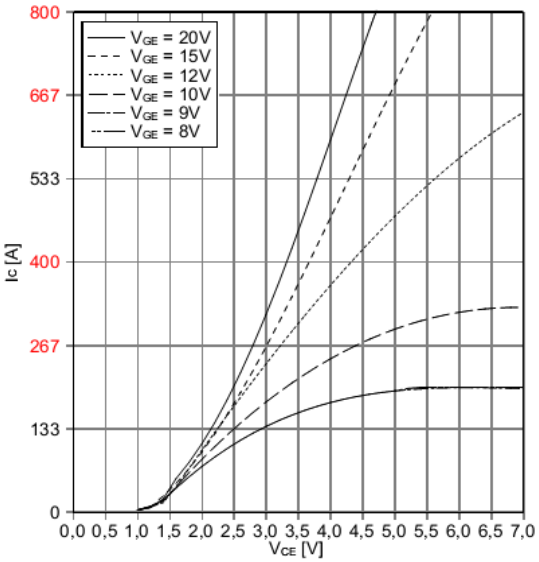
Vorläufige Daten
Preliminary Data

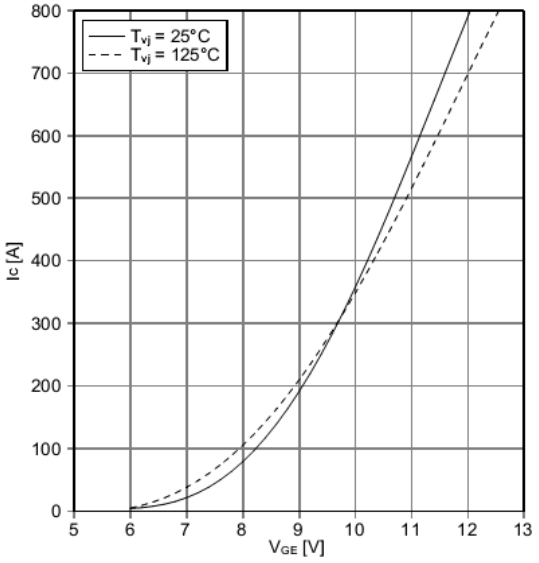
Ausgangskennlinie IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
V_{GE} = 15 V



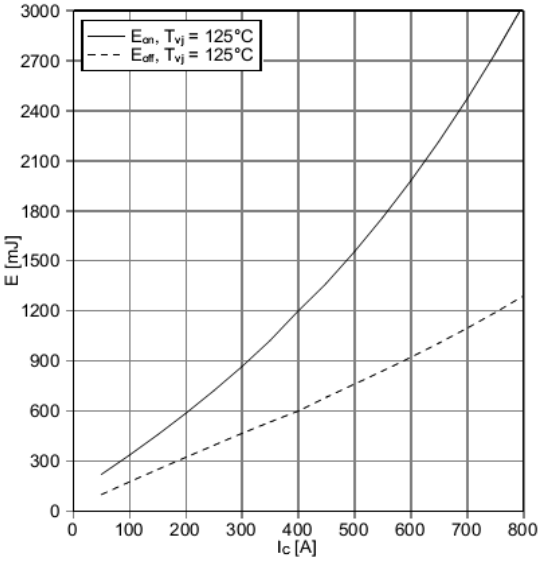
Ausgangskennlinienfeld IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
T_{vj} = 125°C



Übertragungscharakteristik IGBT,Wechselrichter (typisch)
transfer characteristic IGBT,Inverter(typical)
$I_C = f(V_{GE})$
V_{CE} = 20 V



SchaltverlustelGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
V_{GE} = ±15 V, R_{Gon} = 6.2 Ω, R_{Goff} = 13 Ω, V_{CE} = 1800 V, C_{GE} = 100 nF



prepared by: KHH	date of publication: 2013-10-03
approved by: TS	revision: 2.0

Technische Information / Technical Information

IGBT-Module
IGBT-modules

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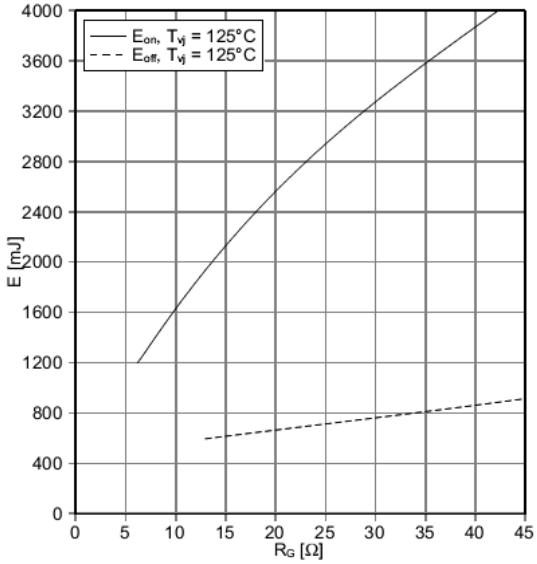
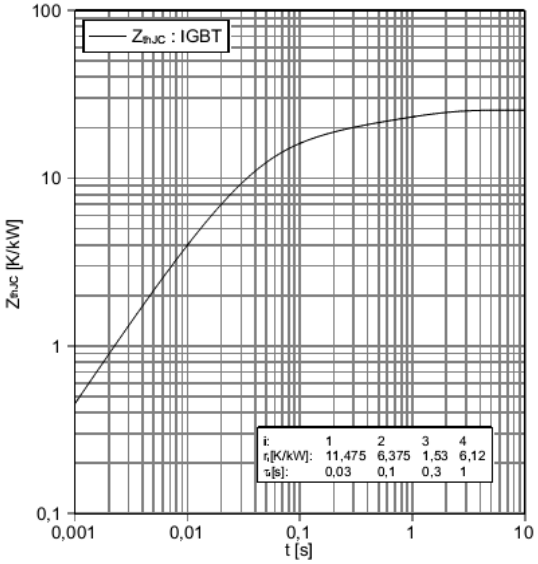
Vorläufige Daten
Preliminary Data

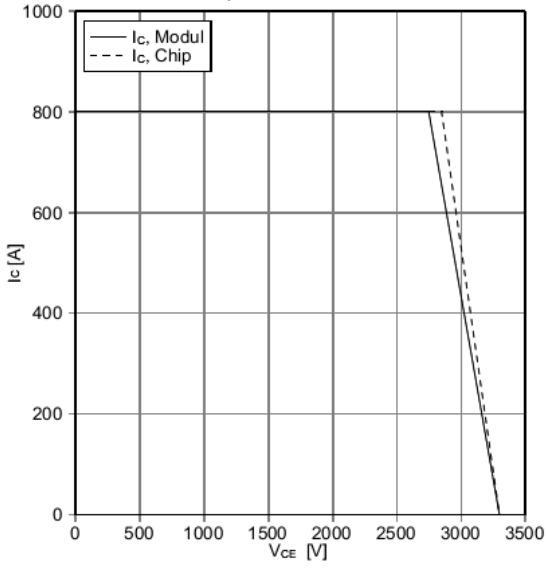
SchaltverlustelGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
V_{GE} = ±15 V, I_C = 400 A, V_{CE} = 1800 V, C_{GE} = 100 nF



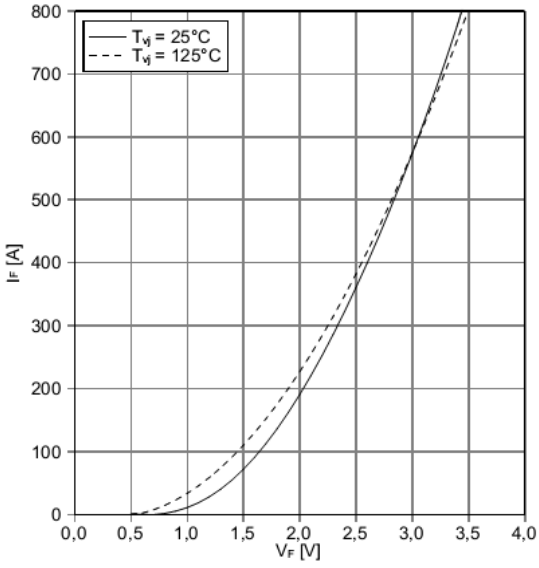
Transienter Wärmewiderstand IGBT,Wechselrichter
transient thermal impedance IGBT,Inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT,Wechselrichter (RBSOA)
reverse bias safe operating area IGBT,Inverter (RBSOA)
$I_C = f(V_{CE})$
V_{GE} = ±15 V, R_{Goff} = 13 Ω, T_{vj} = 125°C, C_{GE} = 100 nF



Durchlasskennlinie der Diode, Wechselrichter (typisch)
forward characteristic of Diode, Inverter (typical)
$I_F = f(V_F)$



prepared by: KHH	date of publication: 2013-10-03
approved by: TS	revision: 2.0

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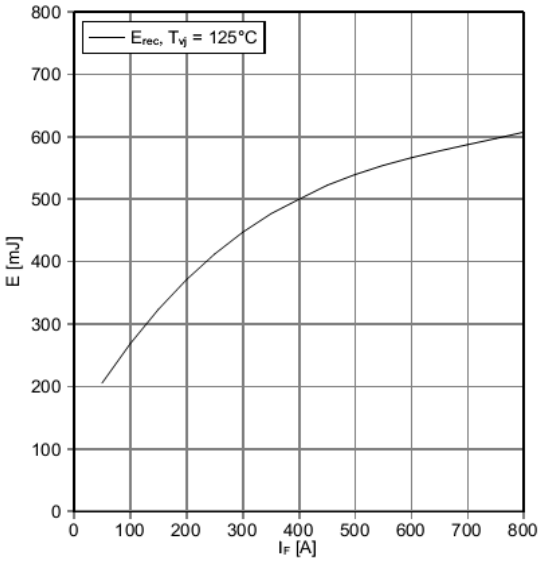
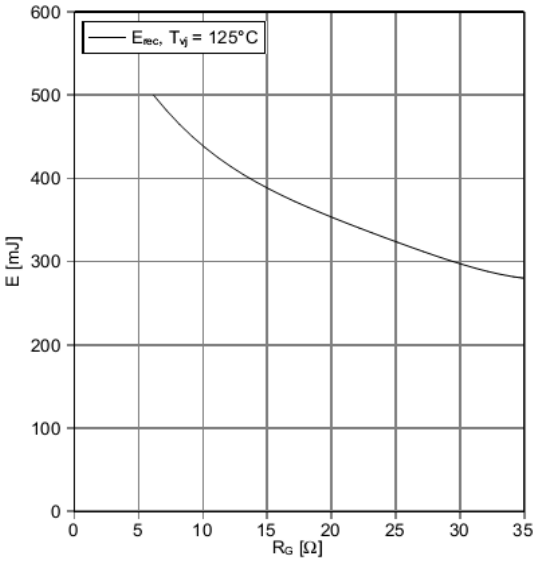
Vorläufige Daten
Preliminary Data

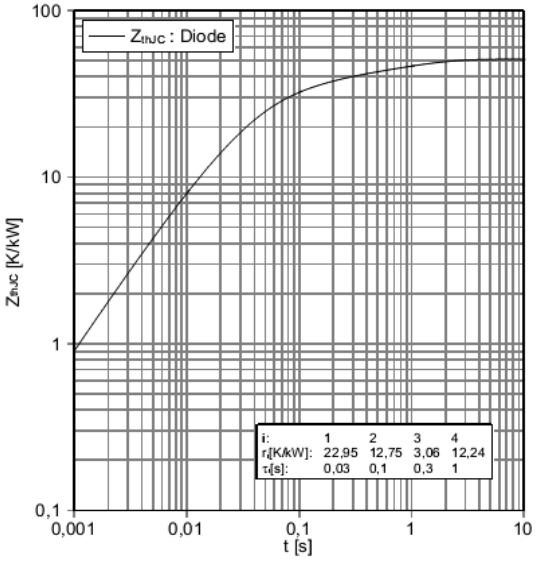
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 6.2\ \Omega$, $V_{CE} = 1800$ V



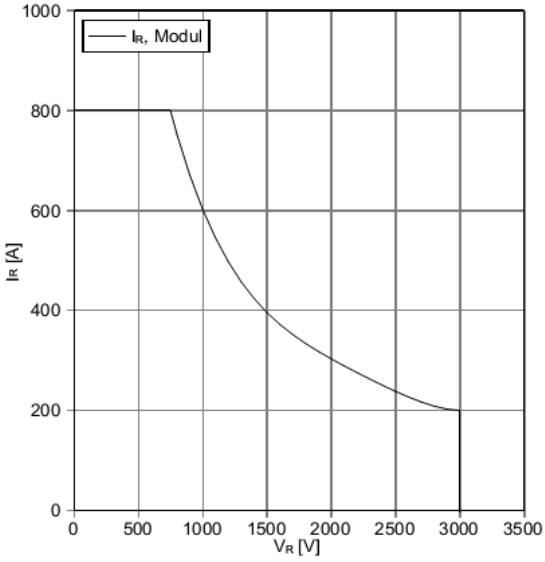
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 400$ A, $V_{CE} = 1800$ V



Transienter Wärmewiderstand Diode, Wechselrichter
transient thermal impedance Diode, Inverter
$Z_{thJC} = f(t)$



Sicherer Arbeitsbereich Diode, Wechselrichter (SOA)
safe operation area Diode, Inverter (SOA)
$I_R = f(V_R)$
$T_{vj} = 125$°C



prepared by: KHH	date of publication: 2013-10-03
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Technische Information / Technical Information

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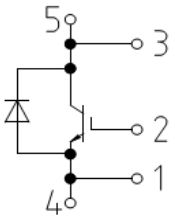
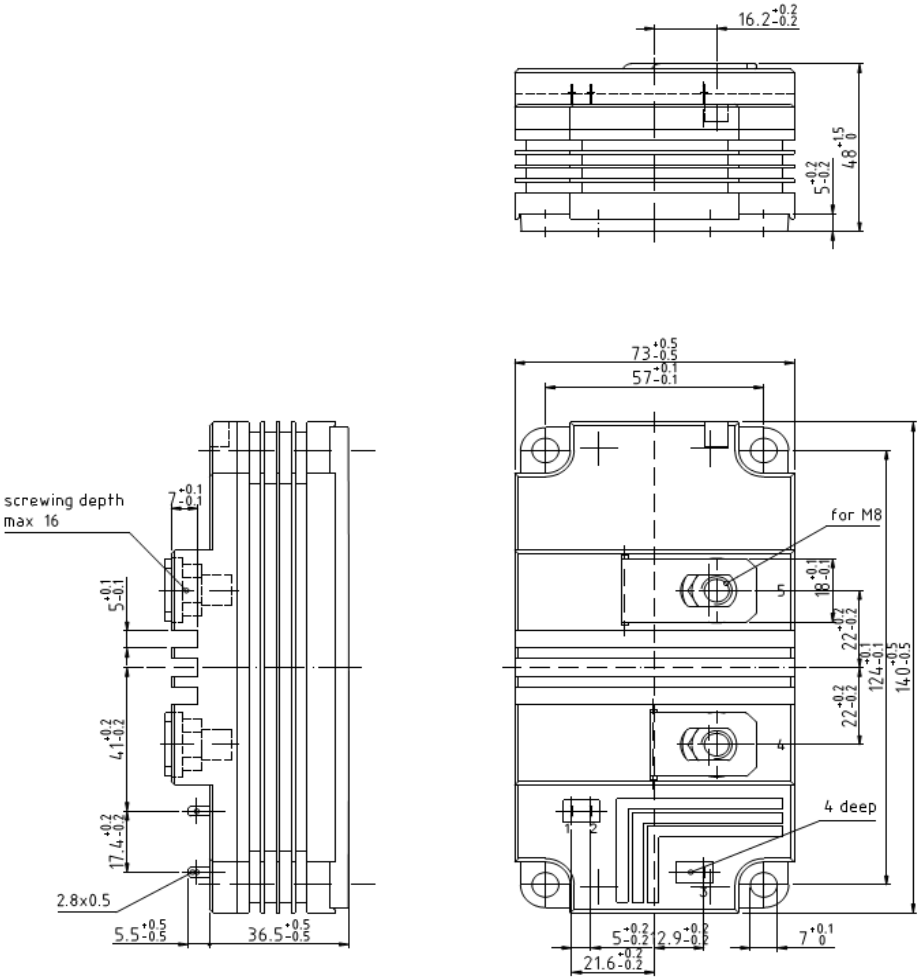
Vorläufige Daten
Preliminary Data

Schaltplan / circuit_diagram_headline



Gehäuseabmessungen / package outlines



prepared by: KHH	date of publication: 2013-10-03
approved by: TS	revision: 2.0

Technische Information / Technical Information

IGBT-Module
IGBT-modules

FZ400R33KL2C_B5

Vorläufige Daten
Preliminary Data

Nutzungsbedingungen

Die in diesem Produktdatenblatt enthaltenen Daten sind ausschließlich für technisch geschultes Fachpersonal bestimmt. Die Beurteilung der Eignung dieses Produktes für Ihre Anwendung sowie die Beurteilung der Vollständigkeit der bereitgestellten Produktdaten für diese Anwendung obliegt Ihnen bzw. Ihren technischen Abteilungen.

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- die gemeinsame Durchführung eines Risiko- und Qualitätsassessments;
- den Abschluss von speziellen Qualitätssicherungsvereinbarungen;
- die gemeinsame Einführung von Maßnahmen zu einer laufenden Produktbeobachtung dringend empfehlen und gegebenenfalls die Belieferung von der Umsetzung solcher Maßnahmen abhängig machen.

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Terms & Conditions of usage

The data contained in this product data sheet is exclusively intended for technically trained staff. You and your technical departments will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to such application.

This product data sheet is describing the characteristics of this product for which a warranty is granted. Any such warranty is granted exclusively pursuant the terms and conditions of the supply agreement. There will be no guarantee of any kind for the product and its characteristics. The information in the valid application- and assembly notes of the module must be considered.

Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of our product, please contact the sales office, which is responsible for you (see www.infineon.com). For those that are specifically interested we may provide application notes.

Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact the sales office, which is responsible for you.

Should you intend to use the Product in aviation applications, in health or live endangering or life support applications, please notify. Please note, that for any such applications we urgently recommend
- to perform joint Risk and Quality Assessments;
- the conclusion of Quality Agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery depended on the realization of any such measures.

If and to the extent necessary, please forward equivalent notices to your customers.

Changes of this product data sheet are reserved.

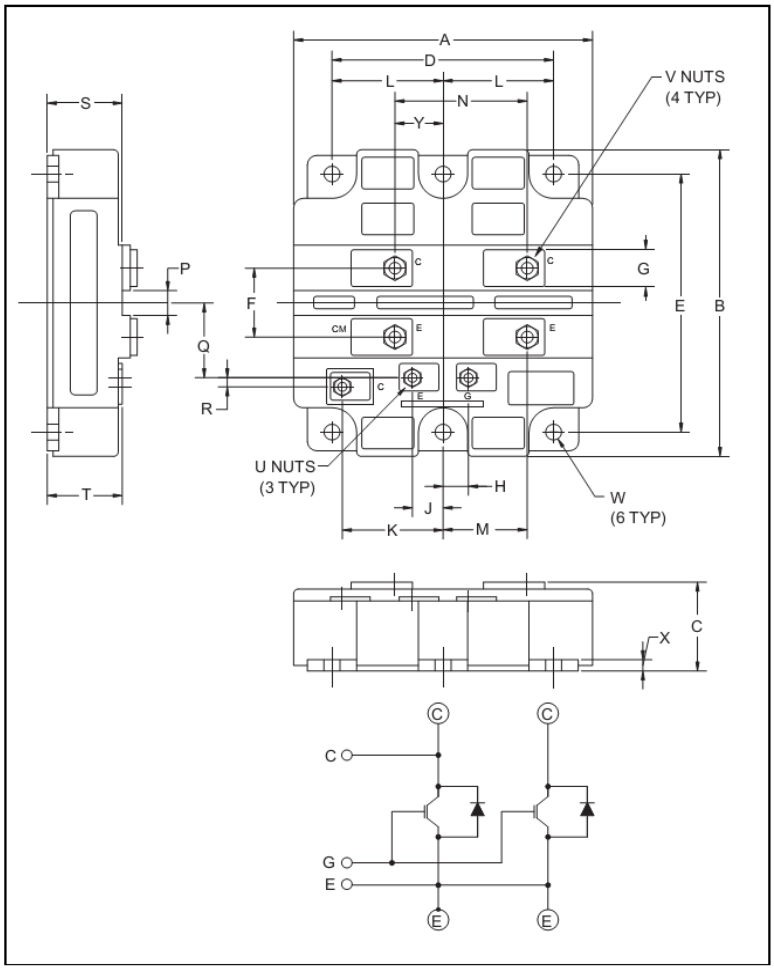
prepared by: KHH	date of publication: 2013-10-03
approved by: TS	revision: 2.0

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

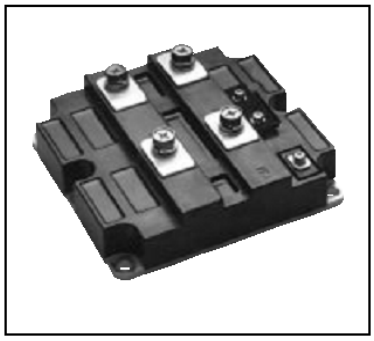
CM400HB-90H

Single IGBTMOD™ HVIGBT

400 Amperes/4500 Volts



Outline Drawing and Circuit Diagram



Description:
Powerex IGBTMOD™ Modules are designed for use in switching applications. Each module consists of one IGBT Transistor with a reverse-connected super-fast recovery free-wheel diode. All components and interconnects are isolated from the heat sinking baseplate, offering simplified system assembly and thermal management.

Features:
- ☐ Low Drive Power
- ☐ Low $V_{CE(sat)}$
- ☐ Super-Fast Recovery Free-Wheel Diode
- ☐ Isolated Baseplate for Easy Heat Sinking

Applications:
- ☐ Traction
- ☐ Medium Voltage Drive
- ☐ High Voltage Power Supplies

Ordering Information:
Example: Select the complete part module number you desire from the table below -i.e. CM400HB-90H is a 4500V (V_{CES}), 400 Ampere Single IGBTMOD™ Power Module.

Type	Current Rating Amperes	V_{CES} Volts (x 50)
CM	400	90

Dimensions	Inches	Millimeters
A	5.12	130.0
B	5.51	140.0
C	1.50	38.0
D	4.48	114.0
E	4.88±0.01	124.0±0.25
F	1.57	40.0
G	0.79	20.0
H	0.41	10.35
J	0.42	10.65
K	1.92	48.8
L	2.24±0.01	57.0±0.25
M	1.71	43.5

Dimensions	Inches	Millimeters
N	2.42	61.5
P	0.59	15.0
Q	1.57	40.0
R	0.20	5.2
S	1.16	29.5
T	1.10	28.0
U	M4 Metric	M4
V	M8 Metric	M8
W	0.28 Dia.	Dia.7.0
X	0.20	5.0
Y	0.71	18.0

Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (724) 925-7272

CM400HB-90H
Single IGBTMOD™ HVIGBT
400 Amperes/4500 Volts

Absolute Maximum Ratings, T_j = 25 °C unless otherwise specified

Ratings	Symbol	CM400HB-90H	Units
Junction Temperature	T_j	-40 to 150	°C
Storage Temperature	T_{stg}	-40 to 125	°C
Collector-Emitter Voltage (V_{GE} = 0V)	V_{CES}	4500	Volts
Gate-Emitter Voltage (V_{CE} = 0V)	V_{GES}	±20	Volts
Collector Current (T_C = 25°C)	I_C	400	Amperes
Peak Collector Current (Pulse)	I_{CM}	800*	Amperes
Diode Forward Current** (T_C = 25°C)	I_E	400	Amperes
Diode Forward Surge Current** (Pulse)	I_{EM}	800*	Amperes
Maximum Collector Dissipation (T_C = 25°C, IGBT Part, $T_j \leq$ 125°C)	P_C	4300	Watts
Max. Mounting Torque M8 Terminal Screws	–	115	in-lb
Max. Mounting Torque M6 Mounting Screws	–	53	in-lb
Max. Mounting Torque M4 Auxiliary Terminal Screws	–	17	in-lb
Module Weight (Typical)	–	1.5	kg
Isolation Voltage (Charged Part to Baseplate, AC 60Hz 1 min.)	V_{iso}	6000	Volts

* Pulse width and repetition rate should be such that device junction temperature (T_j) does not exceed $T_{j(max)}$ rating.
**Represents characteristics of the anti-parallel, emitter-to-collector free-wheel diode (FWDi).

Static Electrical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Collector-Cutoff Current	I_{CES}	$V_{CE} = V_{CES}$, V_{GE} = 0V	–	–	8.0	mA
Gate Leakage Current	I_{GES}	$V_{GE} = V_{GES}$, V_{CE} = 0V	–	–	0.5	μA
Gate-Emitter Threshold Voltage	$V_{GE(th)}$	I_C = 40mA, V_{CE} = 10V	4.5	6.0	7.5	Volts
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 400A, V_{GE} = 15V, T_j = 25°C	–	3.0	3.9*	Volts
		I_C = 400A, V_{GE} = 15V, T_j = 125°C	–	3.3	–	Volts
Total Gate Charge	Q_G	V_{CC} = 2250V, I_C = 400A, V_{GE} = 15V	–	3.6	–	μC
Emitter-Collector Voltage**	V_{EC}	I_E = 400A, V_{GE} = 0V	–	4.0	5.2	Volts

* Pulse width and repetition rate should be such that device junction temperature rise is negligible.
**Represents characteristics of the anti-parallel, emitter-to-collector free-wheel diode (FWDi).

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CM400HB-90H
Single IGBTMOD™ HVIGBT
400 Amperes/4500 Volts

Dynamic Electrical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input Capacitance		C_{ies}	V_{GE} = 0V, V_{CE} = 10V	–	72	–	nF
Output Capacitance		C_{oes}		–	5.3	–	nF
Reverse Transfer Capacitance		C_{res}		–	1.6	–	nF
Resistive	Turn-on Delay Time	$t_{d(on)}$	V_{CC} = 2250V, I_C = 400A,	–	–	2.4	μs
Load	Rise Time	t_r	V_{GE1} = V_{GE2} = 15V,	–	–	2.4	μs
Switching	Turn-off Delay Time	$t_{d(off)}$	R_G = 22.5Ω	–	–	6.0	μs
Times	Fall Time	t_f	Resistive Load Switching Operation	–	–	1.2	μs
Diode Reverse Recovery Time**		t_{rr}	I_E = 400A, di_E/dt = -800A/μs	–	–	1.8	μs
Diode Reverse Recovery Charge**		Q_{rr}	I_E = 400A, di_E/dt = -800A/μs	–	160*	–	μC

* Pulse width and repetition rate should be such that device junction temperature rise is negligible.
**Represents characteristics of the anti-parallel, emitter-to-collector free-wheel diode (FWDi).

Thermal and Mechanical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Thermal Resistance, Junction to Case	$R_{th(j-c)}$ Q	Per IGBT	–	–	0.023	K/W
Thermal Resistance, Junction to Case	$R_{th(j-c)}$ D	Per FWDi	–	–	0.045	K/W
Contact Thermal Resistance, Case to Fin	$R_{th(c-f)}$	Per Module, Thermal Grease Applied	–	0.015	–	K/W

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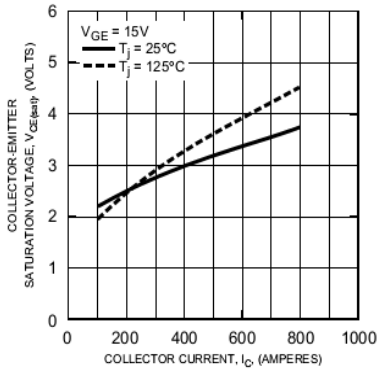
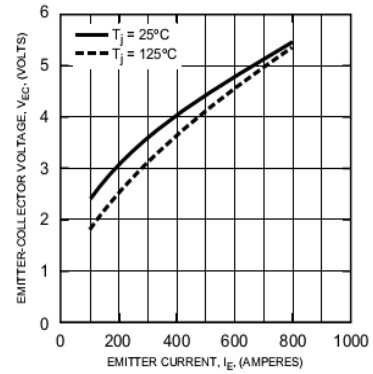
CM400HB-90H
Single IGBTMOD™ HVIGBT
400 Amperes/4500 Volts

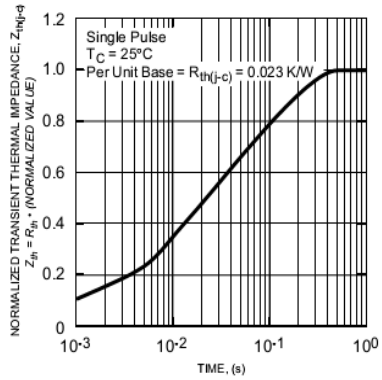
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



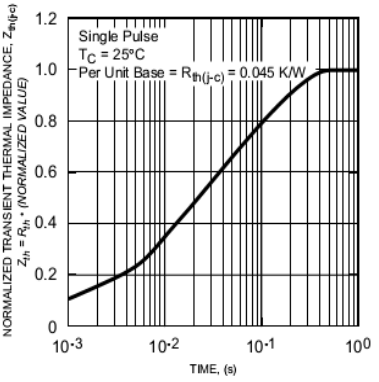
FREE-WHEEL DIODE FORWARD CHARACTERISTICS (TYPICAL)



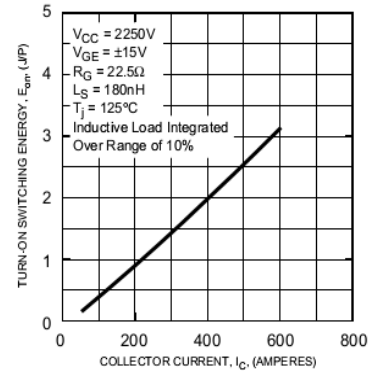
TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (IGBT)



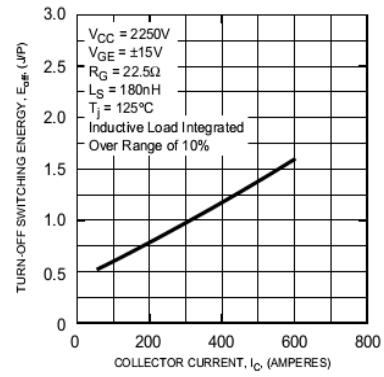
TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (FWDi)



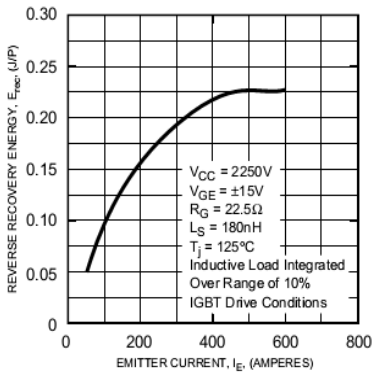
HALF-BRIDGE TURN-ON SWITCHING ENERGY CHARACTERISTICS (TYPICAL)



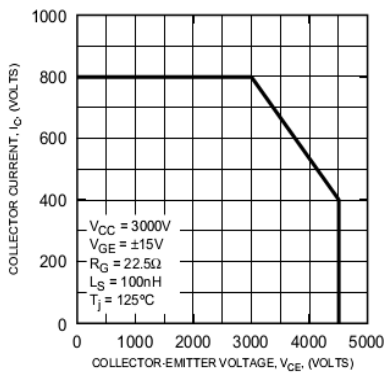
HALF-BRIDGE TURN-OFF SWITCHING ENERGY CHARACTERISTICS (TYPICAL)



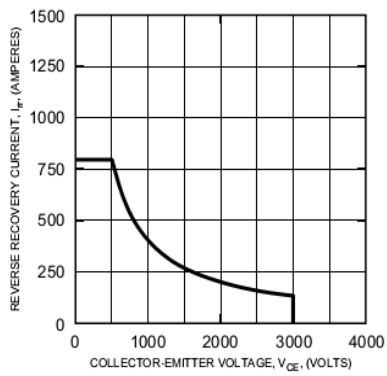
FREE-WHEEL DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)



TURN-ON SWITCHING SAFE OPERATING AREA (RBSOA) (TYPICAL)



DIODE REVERSE RECOVERY SAFE OPERATING AREA (TYPICAL)



Technische Information / Technical Information

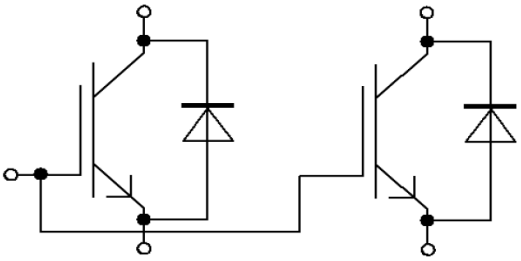
IGBT-Module
IGBT-modules

FZ400R65KE3

hochisolierendes Modul
high insulated module

Vorläufige Daten / Preliminary Data

Typical Appearance



V_{CES} = 6500V
$I_{C\ nom}$ = 400A / I_{CRM} = 800A

Typische Anwendungen
- Mittelspannungsantriebe
- Traktionsumrichter

Typical Applications
- Medium Voltage Converters
- Traction Drives

Elektrische Eigenschaften
- Niedriges V_{CEsat}

Electrical Features
- Low V_{CEsat}

Mechanische Eigenschaften
- AlSiC Bodenplatte für erhöhte thermische Lastwechselfestigkeit
- Erweiterter Lagertemperaturbereich bis zu T_{stg} = -55°C
- Gehäuse mit CTI > 600
- Gehäuse mit erweiterten Isolationseigenschaften von 10,2kV AC 1min
- Große Luft- und Kriechstrecken

Mechanical Features
- AlSiC Base Plate for increased Thermal Cycling Capability
- Extended Storage Temperature down to T_{stg} = -55°C
- Package with CTI > 600
- Package with enhanced Insulation of 10.2kV AC 1min
- High Creepage and Clearance Distances

Module Label Code

Barcode Code 128

Sample
00000123456000000000000

DMX - Code

Content of the Code	Digit
Module Serial Number	1 - 5
Module Material Number	6 - 11
Production Order Number	12 - 19
Datecode (Production Year)	20 - 21
Datecode (Production Week)	22 - 23

prepared by: DTH	date of publication: 2013-03-14	
approved by: DTS	revision: 2.1	UL approved (E83335)

Technische Information / Technical Information

IGBT-Module
IGBT-modules

FZ400R65KE3

Vorläufige Daten
Preliminary Data

IGBT,Wechselrichter / IGBT,Inverter

Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 125°C T_{vj} = 25°C T_{vj} = -50°C	V_{CES}	6500 6500 5900	V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 80°C, T_{vj} = 150°C	$I_{C\,nom}$	400	A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	800	A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, T_{vj} = 150°C	P_{tot}	8,35	kW
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage		V_{GES}	+/-20	V

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	I_C = 400 A, V_{GE} = 15 V I_C = 400 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C	$V_{CE\,sat}$	3,00 3,70	3,40	V V
Gate-Schwellenspannung Gate threshold voltage	I_C = 70,0 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	5,4	6,0	6,6	V
Gateladung Gate charge	V_{GE} = -15 V ... +15 V, V_{CE} = 3600V		Q_G		17,0		µC
Interner Gatewiderstand Internal gate resistor	T_{vj} = 25°C		R_{Gint}		1,1		Ω
Eingangskapazität Input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		110		nF
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		1,70		nF
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V_{CE} = 6500 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			5,0	mA
Gate-Emitter-Reststrom Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	I_C = 400 A, V_{CE} = 3600 V V_{GE} = ±15 V R_{Gon} = 1,9 Ω	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,on}$		0,70 0,80		µs µs
Anstiegszeit, induktive Last Rise time, inductive load	I_C = 400 A, V_{CE} = 3600 V V_{GE} = ±15 V R_{Gon} = 1,9 Ω	T_{vj} = 25°C T_{vj} = 125°C	t_r		0,33 0,40		µs µs
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	I_C = 400 A, V_{CE} = 3600 V V_{GE} = ±15 V R_{Goff} = 13 Ω	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,off}$		7,30 7,60		µs µs
Fallzeit, induktive Last Fall time, inductive load	I_C = 400 A, V_{CE} = 3600 V V_{GE} = ±15 V R_{Goff} = 13 Ω	T_{vj} = 25°C T_{vj} = 125°C	t_f		0,40 0,50		µs µs
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 400 A, V_{CE} = 3600 V, L_S = 280 nH V_{GE} = ±15 V, di/dt = 1600 A/µs (T_{vj}=125°C) R_{Gon} = 1,9 Ω	T_{vj} = 25°C T_{vj} = 125°C	E_{on}		2250 3450		mJ mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 400 A, V_{CE} = 3600 V, L_S = 280 nH V_{GE} = ±15 V R_{Goff} = 13 Ω	T_{vj} = 25°C T_{vj} = 125°C	E_{off}		2000 2250		mJ mJ
Kurzschlußverhalten SC data	V_{GE} ≤ 15 V, V_{CC} = 4500 V V_{CEmax} = V_{CES} -L_{sCE} ·di/dt	t_P ≤ 10 µs, T_{vj} = 125°C	I_{SC}		2400		A
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}			15,0	K/kW
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		14,0		K/kW

prepared by: DTH	date of publication: 2013-03-14
approved by: DTS	revision: 2.1

Technische Information / Technical Information

IGBT-Module
IGBT-modules

FZ400R65KE3

Vorläufige Daten
Preliminary Data

Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 125°C T_{vj} = 25°C T_{vj} = -50°C	V_{RRM}	6500 6500 5900	V
Dauergleichstrom Continuous DC forward current		I_F	400	A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	800	A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I²t	130	kA²s
Spitzenverlustleistung Maximum power dissipation	T_{vj} = 125°C	P_{RQM}	1600	kW
Mindesteinschaltdauer Minimum turn-on time		$t_{on\ min}$	10,0	µs

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Durchlassspannung Forward voltage	I_F = 400 A, V_{GE} = 0 V I_F = 400 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C	V_F		3,00 2,95	3,50	V V
Rückstromspitze Peak reverse recovery current	I_F = 400 A, - di_F/dt = 1600 A/µs (T_{vj}=125°C) V_R = 3600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	I_{RM}		600 670		A A
Sperrverzögerungsladung Recovered charge	I_F = 400 A, - di_F/dt = 1600 A/µs (T_{vj}=125°C) V_R = 3600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	Q_r		470 870		µC µC
Abschaltenergie pro Puls Reverse recovery energy	I_F = 400 A, - di_F/dt = 1600 A/µs (T_{vj}=125°C) V_R = 3600 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	E_{rec}		740 1600		mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			33,0	K/kW
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		21,5		K/kW

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Modul / Module

Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		10,2		kV
Teilentladungs-Aussetzspannung Partial discharge extinction voltage	RMS, f = 50 Hz, Q_{PD} typ 10 pC (acc. to IEC 1287)	V_{ISOL}		5,1		kV
Kollektor-Emitter-Gleichsperrspannung DC stability	T_{vj} = 25°C, 100 fit	$V_{CE\,D}$		3800		V
Material Modulgrundplatte Material of module baseplate				AlSiC		
Innere Isolation Internal isolation	Basisisolierung (Schutzklasse 1, EN61140) basic insulation (class 1, IEC 61140)			AlN		
Kriechstreck Creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			56,0 56,0		mm
Luftstrecke Clearance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			26,0 26,0		mm
Vergleichszahl der Kriechwegbildung Comperative tracking index		CTI		> 600		
			min.	typ.	max.	
Modulstreuinduktivität Stray inductance module		L_{sCE}		20		nH
Modulleitungswiderstand, Anschlüsse - Chip Module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$ $R_{AA'+CC'}$		0,18 0,18		mΩ
Höchstzulässige Sperrschichttemperatur Maximum junction temperature	Wechselrichter, Brems-Chopper / inverter, brake-chopper	$T_{vj\,max}$			150	°C
Temperatur im Schaltbetrieb Temperature under switching conditions	Wechselrichter, Brems-Chopper / inverter, brake-chopper	$T_{vj\,op}$	-50		125	°C
Lagertemperatur Storage temperature		T_{stg}	-55		125	°C
Anzugsdrehmoment f. Modulmontage Mounting torque for modul mounting	Schraube M6 - Montage gem. gültiger Applikationsschrift Screw M6 - Mounting according to valid application note	M	4,25	-	5,75	Nm
Anzugsdrehmoment f. elektr. Anschlüsse Terminal connection torque	Schraube M8 - Montage gem. gültiger Applikationsschrift Screw M8 - Mounting according to valid application note	M	1,8 8,0	- -	2,1 10	Nm Nm
Gewicht Weight		G		1000		g

prepared by: DTH	date of publication: 2013-03-14
approved by: DTS	revision: 2.1

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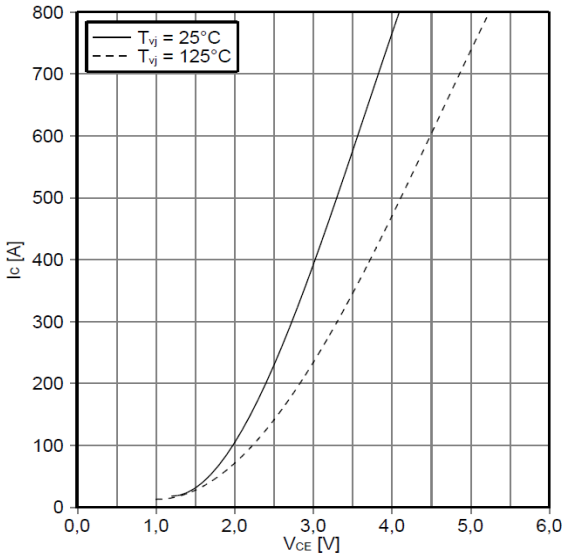
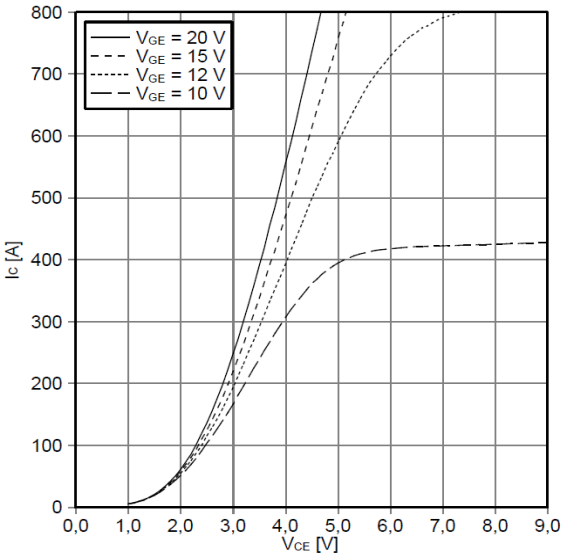
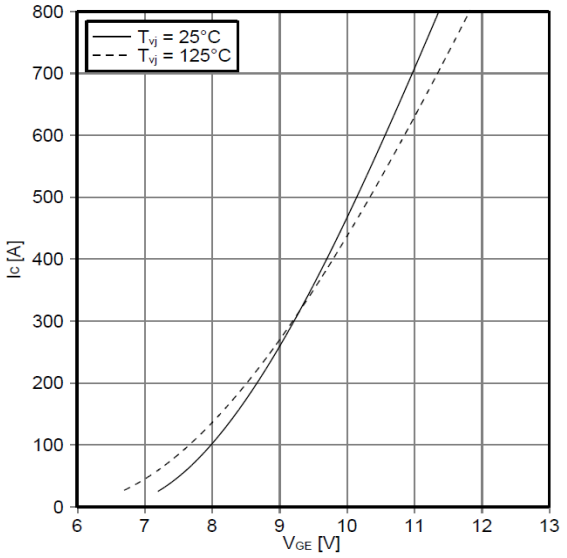
Ausgangskennlinie IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
V_{GE} = 15 V



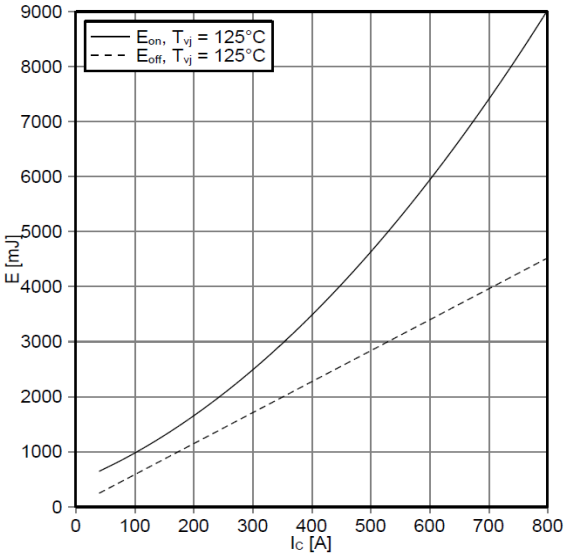
Ausgangskennlinienfeld IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
T_{vj} = 125°C



Übertragungscharakteristik IGBT,Wechselrichter (typisch)
transfer characteristic IGBT,Inverter(typical)
$I_C = f(V_{GE})$
V_{CE} = 20 V



SchaltverlustelGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
V_{GE} = ±15 V, R_{Gon} = 1.9 Ω, R_{Goff} = 12.8 Ω, V_{CE} = 3600 V



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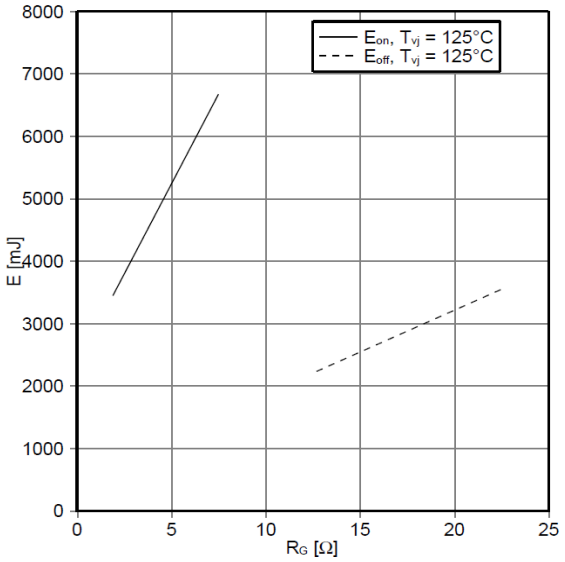
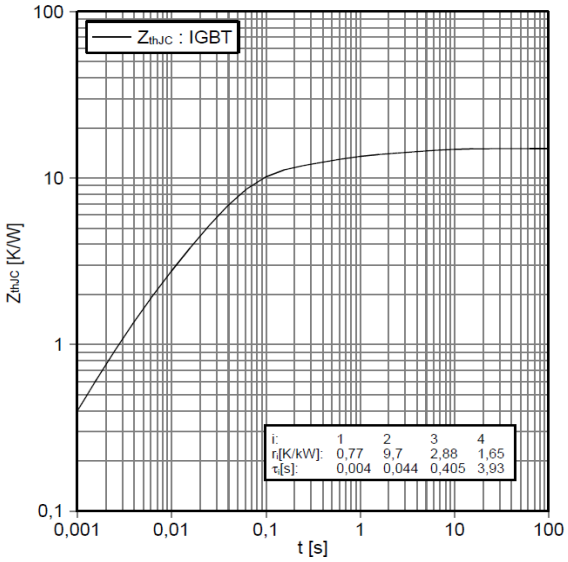
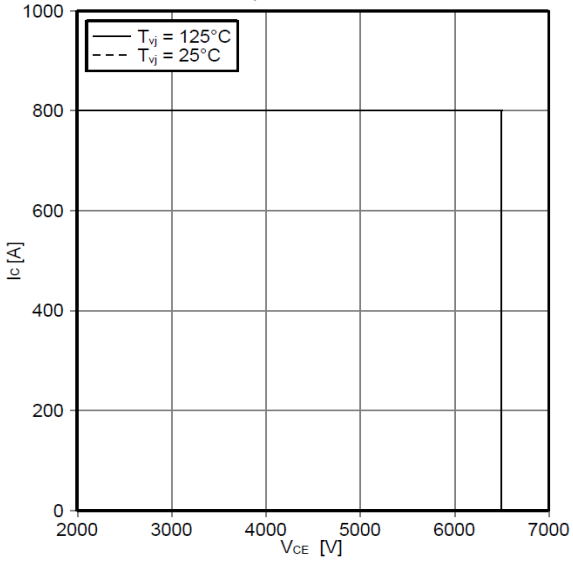
SchaltverlusteIGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
V_{GE} = ±15 V, I_C = 400 A, V_{CE} = 3600 V



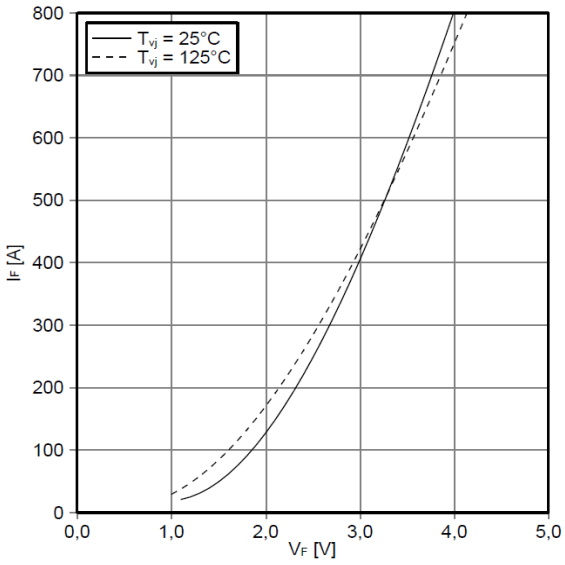
Transienter Wärmewiderstand IGBT,Wechselrichter
transient thermal impedance IGBT,Inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT,Wechselrichter (RBSOA)
reverse bias safe operating area IGBT,Inverter (RBSOA)
$I_C = f(V_{CE})$
V_{GE} = ±15 V, R_{Goff} = 12.8 Ω, T_{vj} = 125°C



Durchlasskennlinie der Diode, Wechselrichter (typisch)
forward characteristic of Diode, Inverter (typical)
$I_F = f(V_F)$



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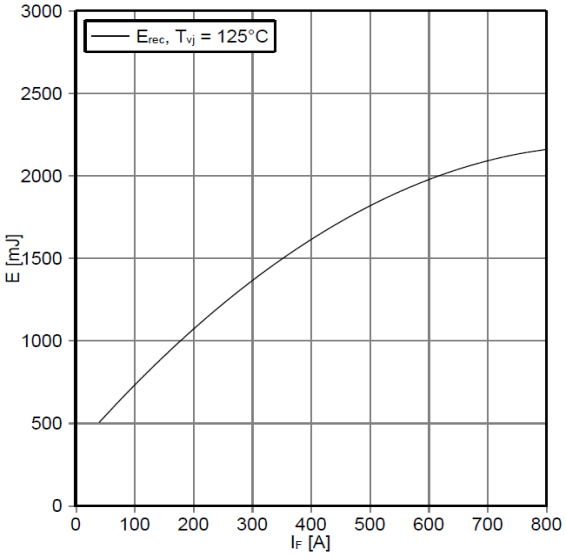
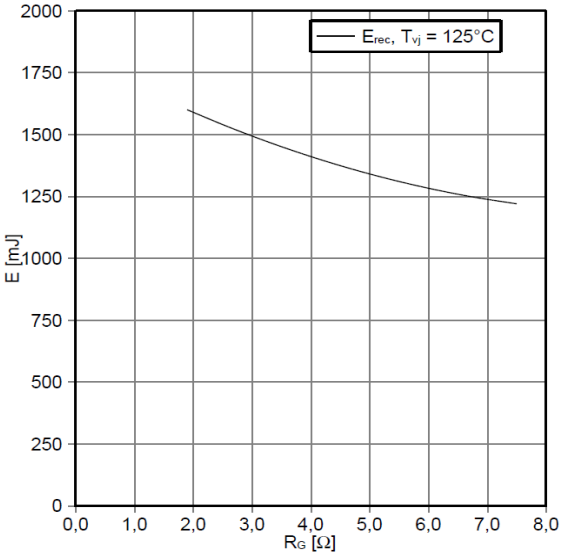
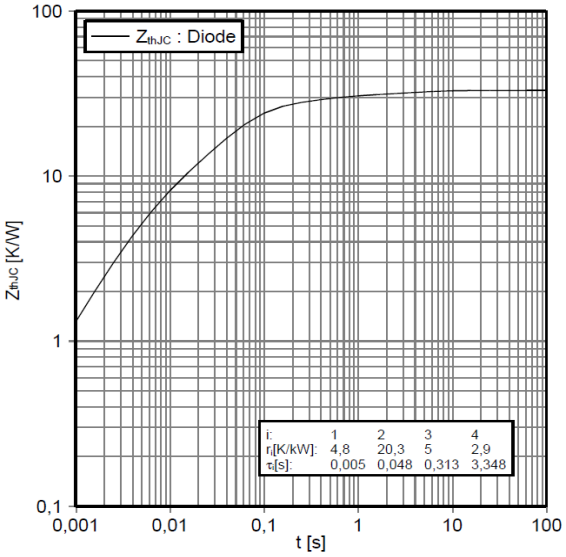
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 1.9\ \Omega$, $V_{CE} = 3600$ V



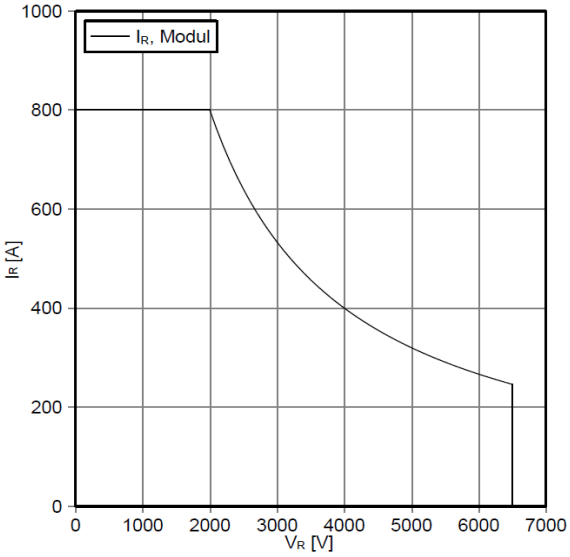
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 400$ A, $V_{CE} = 3600$ V



Transienter Wärmewiderstand Diode, Wechselrichter
transient thermal impedance Diode, Inverter
$Z_{thJC} = f(t)$



Sicherer Arbeitsbereich Diode, Wechselrichter (SOA)
safe operation area Diode, Inverter (SOA)
$I_R = f(V_R)$
$T_{vj} = 125$°C



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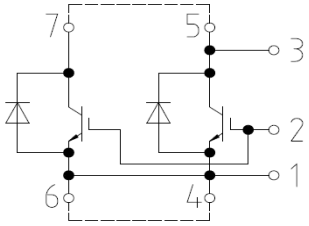
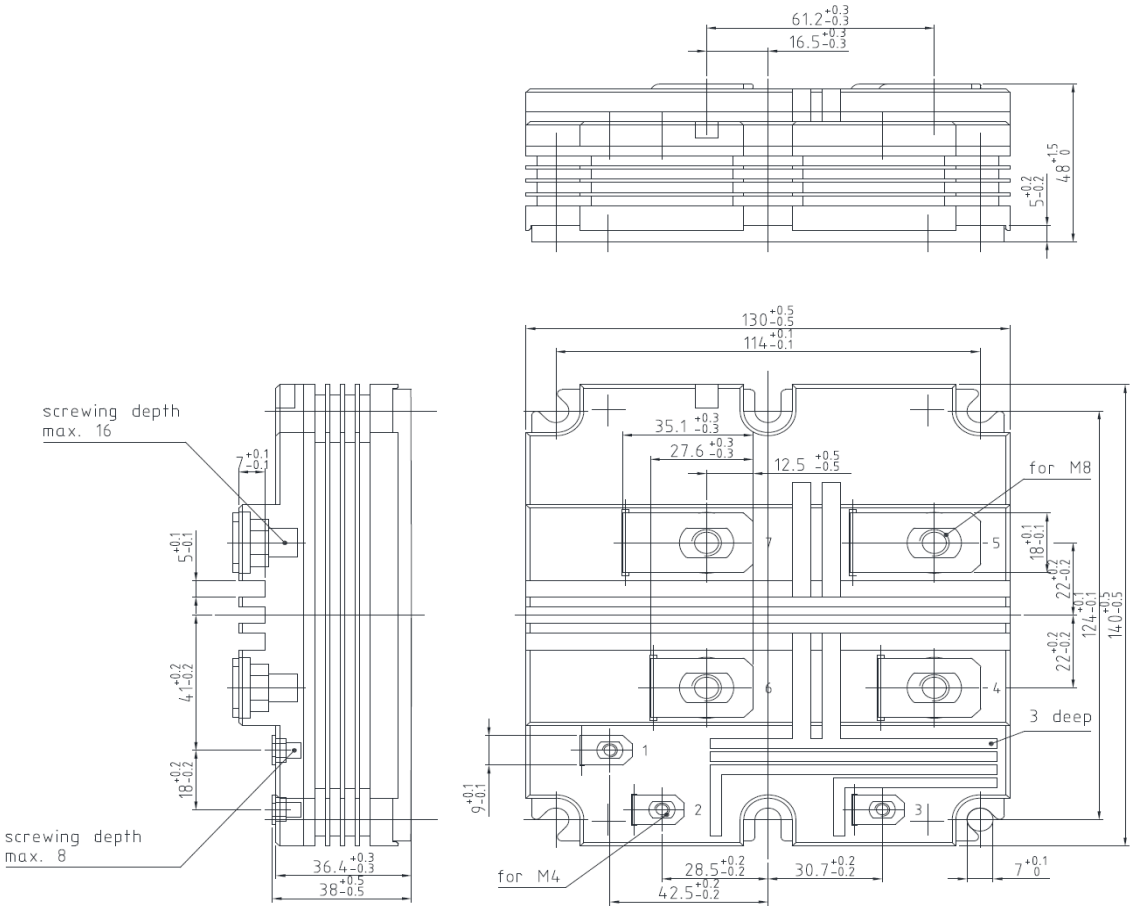
Schaltplan / circuit_diagram_headline



Gehäuseabmessungen / package outlines



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approved by: DTS	revision: 2.1