Organic thin film transistors using a liquid crystalline palladium phthalocyanine as active layer

Juan A. Jiménez Tejada,[1, a)] Pilar Lopez-Varo,[1, b)] Nandu B. Chaure,[2, 3, c)] Isabelle Chambrier,[4, d)] Andrew N. Cammidge,[4, e)] Michael J. Cook,[4, f)] Ali Jafari-Fini,[4, g)] and Asim K. Ray[2, 5, h)]

[1)] *Departamento de Electrónica y Tecnología de Computadores. CITIC-UGR. Universidad de Granada. 18071 Granada. SPAIN*

[2)] *Materials Research Centre, Queen Mary, University of London, Mile End Road London, E1 4NS, UK*

[3)] *Department of Physics, Savitribai Phule Pune University, Pune 411007, INDIA*

[4)] *School of Chemistry, University of East Anglia, Norwich Research Park, Norwich, NR4 7TJ, UK*

[5)] *Department of Electronic and Computer Engineering, Brunel University London, Uxbridge, UB8 3PH, UK*

(Dated: 22 February 2018)

70nm thick solution-processed films of a palladium phthalocyanine ($PdPc_6$) derivative bearing eight hexyl ($-C_6H_{13}$) chains at non-peripheral positions have been employed as active layers in the fabrication of bottom-gate bottom-contact organic thin film transistors (OTFTs) deposited on **highly doped p-type Si (110) substrates with SiO_2 gate dielectric**. The dependence of the transistor electrical performance upon the mesophase behavior of the $PdPc_6$ films has been investigated by measuring the output and transfer characteristics of the OTFT having its active layer ex-situ vacuum annealed at temperatures between 500 °C and 200 °C. A clear correlation between the annealing temperature and the threshold voltage and carrier mobility of the transistors, and the transition temperatures extracted from the differential scanning calorimetric (DSC) curves for bulk materials has been established. This direct relation has been obtained by means of a compact electrical model in which the contact effects are taken into account. The precise determination of the contact-voltage drain-current curves allows for obtaining such a relation.

PACS numbers: 85.30.Tv; 85.30.De; 73.40.Cg; 73.61.Ph
Keywords: Phthalocyanine, field effect, contact effects, device parameters, differential scanning electrical calorimetry

I. INTRODUCTION

In recent years, considerable research interest has grown in the area of organic thin film transistors (OTFTs) for a variety of potential applications in large-area, flexible electronics, such as smart cards, radio frequency identification (RFID) tags and sensors[1–3]. Initial work has been primarily concentrated on physical vapor deposition of p-type conducting polymers such as poly (3-hexylthiophene) (P3HT), poly (3-octylthiophene) (P3OT) and small molecule organic semiconductors such as metallated phthalocyanines. This high temperature method produces polycrystalline structures of active layers, limiting the device performance in terms of carrier mobility, on-off ratios and threshold voltage[4]. In order to meet the challenges for industrial exploitation, intense efforts have been spent on the design and synthesis of a broad range of chemically tunable organic semiconductors for low processing temperature deposition on mechanically flat plastic substrates with a view to producing greatly improved device performance[5].

Phthalocyanines (Pcs), referred to above, are organic macrocyclic compounds that contain a conjugated cyclic 18 π-electron system. They are non-toxic chromophores that are used in a range of applications from industrial pigments to photodynamic agents in cancer therapy, photosensitizers in photocopiers and as a component in compact discs. They were amongst the earliest organic compounds known to possess semiconducting properties (p-type) and are now recognised to offer tremendous scope for developing field effect transistors with charge carrier mobility up to 1 $cm^2V^{-1}s^{-1}$[6], solar cells of power conversion efficiencies larger than 5%[7], and smart sensors for environmental pollution monitoring and biodetection at the ppb level[8].

Fabrication of phthalocyanines as thin films has largely exploited vapor deposition techniques. Post-deposition thermal annealing is often required to achieve highly ordered film morphology. **Thus, photoresponsive OTFTs have been fabricated using vacuum deposited palladium phthalocyanine (PdPc) films on Si/SiO_2 substrates for highly sensitive optical transducers and image sensors. PdPc is reported**

[a)] Electronic mail: tejada@ugr.es
[b)] Electronic mail: pilarlopez@ugr.es
[c)] Electronic mail: n.chaure@physics.unipune.ac.in
[d)] Electronic mail: i.fernandes@uea.ac.uk
[e)] Electronic mail: a.cammidge@uea.ac.uk
[f)] Electronic mail: m.cook@uea.ac.uk
[g)] Electronic mail: ali@haj.co.uk
[h)] Electronic mail: Asim.Ray@brunel.ac.uk

to have a more efficient exciton diffusion than copper phthalocyanine (CuPc) and zinc phthalocyanine (ZnPc)[9]. Apart from their interest in optoelectronics, PdPc thin films offer good chemical sensing properties, with fast response times, high base line stability and enhanced sensitivity[10].

The film deposition techniques referred to above are not readily compatible with the requirements for the development of large area, low cost, printable plastic electronics. However, solvent soluble phthalocyanines have been developed through incorporation of various substituents on the fundamental ring system, examples of which include alkyl, alkoxy, or alkoxymethyl chains at some or all of the sixteen sites on the benzenoid rings. Suitable substituted Pc molecules are readily soluble in common organic solvents including tetrahydrofuran, hydrocarbons such as petrol and toluene, and chlorohydrocarbons such as dichloromethane and chloroform. This type of solubility makes them ideal for deposition as well-ordered thin films by using spin coating methods. Particular sets of substituents on the phthalocyanine nucleus can promote the formation of the rare discotic nematic mesophase and/or liquid crystalline columnar mesophase behaviour[11].

In this work, we report the performance of bottom gate OTFTs using the spin coated films of a novel palladium phthalocyanine derivative bearing eight hexyl chains at the so-called non-peripheral (1,4,8,11,15,18,22,25) sites and referred to hereafter as PdPc$_6$. The chemical structure of the molecule and device configuration are shown in Figure 1. The compound demonstrates a columnar mesophase 239-153 °C. Carrier mobility values of 0.02 $cm^2V^{-1}s^{-1}$ and 0.70 $cm^2V^{-1}s^{-1}$ were reported for as-deposited and annealed films, respectively, of similarly substituted CuPc active layer. The high mobility value was partly attributed to the edge-on orientation of the CuPc molecules in the thin film and the relatively large average grain size of 62 nm[12]. Our objectives are to study the role of thermal annealing on the optimization of a PdPc$_6$ OTFT and to determine relations, if they exist, between the molecular reorganization in the semiconductor, that arises from the annealing, and the electrical characteristics of the transistor. In order to establish this link, two different methods are combined: differential scanning calorimetry (DSC) is applied to the material and electrical characterization methods are applied to the transistor.

In order to study the optimization of OTFTs with annealing or other physical or chemical treatments, electrical characterization is frequently employed[13–18]. However, the contact effects of the transistors have not received satisfactory attention. The morphological changes that take place during the annealing process affect all the semiconducting regions of the device, including both the active conducting layer and the contact regions of the transistor. The contact regions of an OTFT deteriorate its electrical performance, but at the same time are a very sensitive part of the device[19–27]. In this regard, the

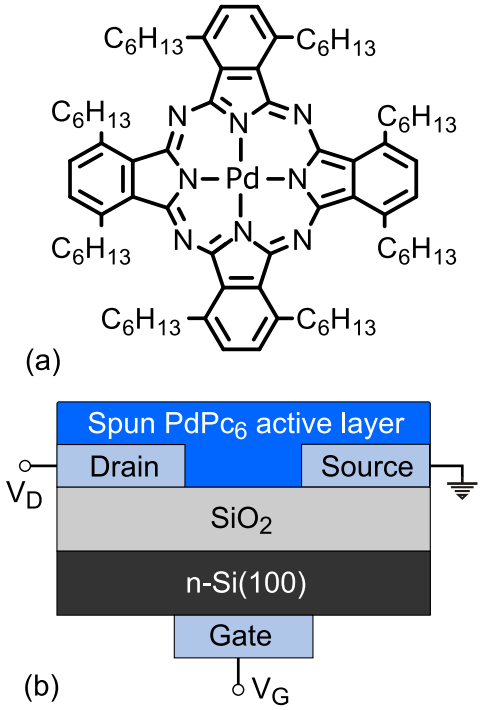

FIG. 1. (a) Palladium phthalocyanine (PdPc$_6$), bearing eight hexyl chains ($-C_6H_{13}$) on non-peripheral sites. (b) bottom-gate bottom-contact (inverted) structure.

characterization of the contact regions can provide useful information about the semiconductor itself. In the case under study, this information provides the way to link the effect of the annealing process on the electrical performance of the OTFT and the mesophase behavior of the organic material. In this work, we describe the evolution of the drain-current vs. contact-voltage ($I_D - V_C$) curves with the annealing temperature. The contact $I_D - V_C$ curves are extracted from output characteristics of the transistor by means of a compact model that considers the effect of the contacts and a gate-voltage dependent mobility[28,29].

II. EXPERIMENTAL METHODS

1,4,8,11,15,18,22,25-Octakis(hexyl)palladium phthalocyanine (PdPc$_6$) (Figure 1a) is a novel phthalocyanine derivative and was prepared by metal insertion into the metal free derivative according to literature procedures using other metal salts[30]. In the typical experiment, palladium(II) acetate was added to a stirred solution of metal-free 1,4,8,11,15,18,22,25-octakis(hexyl)phthalocyanine in 1-pentanol heated to reflux. The colour of the solution changed from green to blue. After 90 minutes, the solution was cooled, the solvent evaporated and the residue, PdPc$_6$, purified by column chromatography.

A Perkin-Elmer differential scanning calorimeter was

used to measure the mesophase behaviour as bulk material of the $PdPc_6$ sample. The precise change in thermal properties of the spun coated sample was optimized by collecting the powder from a dried spun sample. The calorimetry operated with a nitrogen flow of 10 cm^3min^{-1}. Prior to measurements, the temperature of the calorimeter was calibrated. The sample was packed into a specially designed aluminium crucible that was hermetically sealed at 10 MPa pressure. An empty aluminium pan was used for reference. Measurement conditions were set with heating and cooling rate of 10 °C/min.

As shown in Figure 1b, a bottom gate bottom contact (inverted) OTFT with the ratio of channel width (W) to channel length (L) of 200 was fabricated using a 70 nm thick spin coated film of $PdPc_6$ and 250 nm thick silicon dioxide (SiO_2) as the active layer and the gate dielectric layer respectively on the highly doped Si (110) gate electrode. Titanium/gold thin films were used for the source/drain electrodes. The gate SiO_2 dielectric was passivated with an octadecyltrichlorosilane (OTS) self-assembled monolayer. The complete protocols of the substrate cleaning, electrode deposition and surface passivation were given in a previous publication[31].

Twenty OTFT devices were prepared at the same time and these devices were annealed at four different temperatures over the range between 50 °C and 200 °C in a tubular furnace under vacuum of $\sim 2 \times 10^{-7}$ torr and then gradually cooled down to room temperature at the rate of 1 °C/min. **Measurements are repeated on similarly prepared structures with a view to examining the reproducibility of the characteristics.** The surface topographical information of the spin coated $PdPc_6$ thin film was examined in the tapping mode using the Digital Nanoscope III, Atomic Force Microscope (AFM). A cantilever tip (Silicon, NSC15/AIBS, Mikromasch, force constant $k = 46$ N/m) with cantilever resonance frequency at 390 kHz was used as the measuring probe. High resolution images of 512×512 pixels with a scan size of 5×5 μm^2 were obtained.

III. RESULTS AND DISCUSSION

Experimental results are presented along with their interpretation in order to identify the mechanisms responsible for the charge transport mechanism in bottom gated OTFTs employing a 70nm thick liquid crystalline $PdPc_6$ film. New information has been elucidated from careful comparison of values of physical parameters estimated in this investigation with published data.

A. Morphology and liquid crystalline behavior of $PdPc_6$

The DSC scans of as-prepared $PdPc_6$ powder are shown in Figure 2 for both endothermic (heating) and exothermic (cooling) cycles. In the heating cycle, two thermally induced melts exhibited about 192 °C and 239 °C suggesting that different polymorphs were present. The initial broad endothermic transition at 192 °C during the heating cycle is the crystal to columnar mesophase transition. The second transition at about 239 °C is associated with transition from mesophase to isotropic liquid phase. Two transitions exhibited during the cooling cycle $\sim$ 235 °C and 153 °C are related to the mesophase formation and re-crystallization of $PdPc_6$ respectively. The peak at 153 °C is comparatively intense indicating the complete re-crystallization of $PdPc_6$. **Transition temperatures are in broad agreement with those of other similarly substituted metallated phthalocyanines in the literature[32,33].**

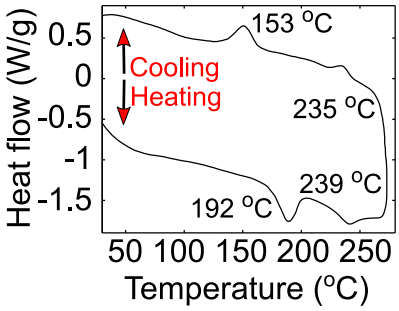

FIG. 2. Differential scanning calorimetry of $PdPc_6$ powder for both heating (endothermic) and cooling (exothermic). The powder is collected from a spin coated sample.

The effect of the post-deposition annealing on the surface morphology of the $PdPc_6$ active layer is **clearly visible from the atomic force images shown in Figure 3**. A void free, compact and small flexible fiber like morphology can be clearly seen from of the as-deposited films (Figure 3a). Thermal treatment at 50 °C caused agglomeration of small fibers to form small flexible clusters (Figure 3b). The cluster size has been found to be increased upon annealing of the film at 100 °C (Figure 3c). The annealing at the higher temperatures of 150 °C and 200 °C gave rise to morphologies containing large sheets Figures 3d and e. All films were found to have adhered well to the substrate. **Values of average particle/cluster size along with roughness data are summarized in Table I.** The particle size is found to increase monotonically with annealing temperature from 0.3 μm for as deposited layer to 2.0 μm for the layer annealed at 200 °C. **A similar coagulation of grains has been reported for copper phthalocyanine active layers[12,34].** The surface roughness in terms of the peak to peak height of $PdPc_6$ layer annealed at 200 °C is found to be much higher than that of as-deposited film, indicating the presence of voids possibly due to the desorption of organic molecules at high annealing temperature.

parameter	samples (annealing temperature, °C) as-prepared	50	100	150	200	**extracted from**
average particle size (μm)	0.3	0.5	0.8	1.0	2.0	AFM data
surface roughness (nm)	1.8	2.6	2.5	2.8	4.2	AFM data
μ_o (cm^2/Vs $\times 10^{-4}$)	0.016	0.27	0.72	0.18	1.1	(1), (8)
V_T (V)	8.2	-9.2	-6.5	8.8	9.4	(1), (8)
γ	1.6	1.6	1.6	1.6	1.6	(1), (8)
m	1.3	1.0	1.4	1.4	1.3	(1), (8)
α_m (A/V$^{m(1+\gamma)} \times 10^{-12}$)	0.38	——	——	4.0	1.9	(9)
V_T (V)	8.5	——	——	8.5	9.9	(9)
$V_T + V_S$ (V)	-6.8	-6.2	-3.5	-6.2	-5.6	(9)
on-off ratio ($\times 10^6$)	1.5	0.82	0.27	0.69	1.5	$I_D - V_G$ data

TABLE I. Organic thin film transistor device parameters.

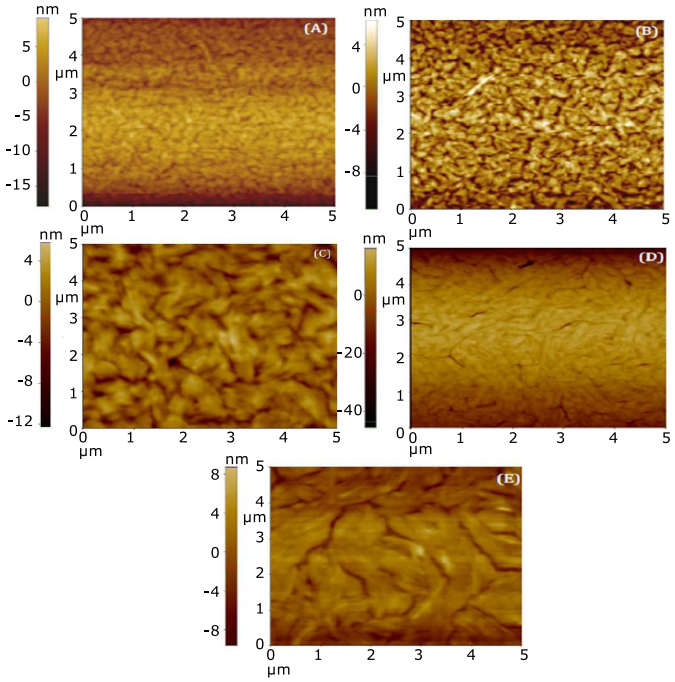

FIG. 3. Two-dimensional AFM micrographs of the surfaces of the thin layers of PdPc$_6$: (A) as-prepared, prior to heat treatment; heat treatment at (B) 50 °C, (C) 100 °C (D) 150 °C and (E) 200 °C.

B. Electrical behavior of PdPc$_6$ based OTFTs

1. Theory

The electrical characterization of the PdPc$_6$ based OTFTs is done with a generic charge drift model[28] which includes the voltage drop at the source contact ($V_S \equiv V_C$, the source terminal is assumed grounded) and an electric field dependent mobility $\mu = \mu_o (V_G - V_T)^{\gamma}$[35–37]:

$$I_D = \frac{k_o[(V_G - V_T - V_S)^{\gamma+2} - (V_G - V_T - V_D)^{\gamma+2}]}{\gamma + 2} \quad (1)$$

where V_G is the gate-terminal voltage, V_D is the drain-terminal voltage or voltage drop between the drain and the source terminals, V_T is the threshold voltage, γ is the mobility enhancement factor, $k_o = WC_i\mu_o/L$, W is the channel width, L is the channel length, C_i is the capacitance per unit surface of the oxide, $C_i = 14$ nF/cm^2 and μ_o is the mobility-related parameter. In order to provide a single value for the voltage dependent mobility, which its dimension is expressed as cm^2/(V$^{1+\gamma}$s), the mobility is evaluated at $V_{GT} = V_G - V_T = 1$ V[28]; thus $\mu(V_{GT} = 1\text{ V}) = \mu_o$ in cm^2/(Vs) or $k(V_{GT} = 1\text{ V}) = k_o$ in A/V^2. This model reflects the fact that the voltage drop at the drain contact is small in comparison to the voltage drop at the source contact[38]. Thus, the applied voltage between the drain and source terminals V_D can be split in the voltage drop along the intrinsic channel $V_{DS} = V_D - V_S$ plus the voltage drop along the contact region $V_S \equiv V_C$ (Figure 2d in Ref.[29]). In this work, we use indistinctly V_S or V_C.

Model (1) is especially useful when combined with a characterization technique to extract its parameters, such as the so called H_{VG} function[28,39]:

$$H_{VG}(V_G) = \frac{\int_{<V_T}^{V_G} I_D(V_G)dV_G}{I_D(V_G)} \quad (2)$$

The H_{VG} function can be evaluated in the linear and saturation modes. In the saturation mode, H_{VG} is linear with V_G[40]:

$$H_{VG}(V_G) = \frac{V_G - V_T - V_S}{\gamma + 3} \quad (3)$$

As a starting point, the H_{VG} function is a good option to initially estimate the transistor parameters. On the one side, the values of γ and V_T can be extracted easily from (3) if $V_S = 0$. However, it is more difficult when V_S is not zero and, in addition, V_S depends on the drain current and the gate voltage ($V_S = V_S(I_D, V_G) \neq 0$). On the other side, the $I_D - V_C$ curves can be extracted from experimental data and (1) if the parameters γ, k_o and

V_T are known:

$$V_S = V_G - V_T - \left[\frac{I_D(\gamma+2)}{k_o} + (V_G - V_T - V_D)^{\gamma+2}\right]^{1/(\gamma+2)} \quad (4)$$

However, it is not frequent to know *a priori* the values of γ, k_o and V_T or the $I_D - V_C$ curves at the contact region. To simultaneously determine the values of these three parameters and the contact $I_D - V_C$ curves from experimental output characteristics, a different characterization method was proposed instead and detailed in previous works[29,41,42].

This characterization method pays special attention to the role of the metal-organic contact. It is observed experimentally that output characteristics measured in OTFTs with contact effects show linear or nonlinear behaviors at low drain voltages[21,41]. The experimental output characteristics measured in this work in different annealed transistors (symbols in Figure 4) also show both behaviors at low values of the drain voltage V_D. In our case, a linear trend is observed only at the 50 °C annealing temperature (Figure 4b) and non-linear trends in the rest of the cases (Figures 4a, c-e).

In a metal-organic structure, a relation between the current density j and the applied voltage V_C can be found by solving the transport equations in the semiconductor[22,43–45]:

$$V_C = \left(\frac{2}{3}\right)\left[\frac{2j}{\varepsilon\mu\theta}\right]^{1/2}\left[(x_C + x_p)^{3/2} - (x_p)^{3/2}\right] \qquad x_p \equiv \frac{j\varepsilon\theta}{2\mu\left[\theta qp(0)\right]^2} \quad (5)$$

where $qp(0)$ is the charge density at the metal-organic interface, $q\theta p(0)$ is the free charge density, (with θ the ratio of free to total charge density), $j = I_D/S$, S is the cross section of the channel where current I_D flows, x_p is a characteristic length defined as the point from the contact interface towards the organic film, at which the charge density $qp(x_p)$ decays to $qp(0)/\sqrt{2}$, ε is the organic dielectric constant and x_C is the length of the contact region in the organic material. Equation (5) was demonstrated to have two asymptotic trends: a linear or Ohmic behavior if the characteristic length x_p is a few times larger than the contact length x_C,

$$I_D \approx \frac{S\theta qp(0)\mu}{x_C} V_C \equiv \frac{V_C}{R_C} \quad (6)$$

and a quadratic behavior (Mott-Gurney law) if the characteristic length x_p is much smaller than the contact length x_C[22,41]

$$I_D \approx \frac{9\varepsilon\mu\theta S}{8x_c^3} V_C^2 \equiv M \times V_C^2. \quad (7)$$

Intermediate cases between these two asymptotic trends can be expressed as

$$I_D = M_m \times V_C^m \quad (8)$$

with m in the range $1 \leq m \leq 2$. The limit values $m = 1$ and $m = 2$ correspond to the linear ($M_1 = 1/R_C$) and quadratic cases ($M_2 = M$), respectively. The parameter M_m is expected to depend on the gate voltage, as many experiments have shown the dependence of the $I_D - V_C$ curve at the contacts with the gate voltage[19,20]. A model for such dependence was proposed in[29]:

$$M_m = \alpha_m (V_G - V_T)^{1+\gamma} \quad (9)$$

where α_m is a constant. This model carries implicitly similar dependences between the contact resistance and the gate voltage can be found in previous models[46–48].

Model (9) was deduced for the cases in which the free charge density in the contact region, $\sigma_{contact}$, can be considered a fraction $1/K$ of the free charge density in the conducting channel, $\sigma_{contact} = \sigma_{channel}/K$, where the free-charge surface-density, $\sigma_{channel}$, is usually expressed as $\sigma_{channel} = C_i(V_G - V_T)$[49]. This relation is justified in situations in which the mobile charges in these two adjacent regions (conducting channel and contact region) start appearing at the same voltages and follow similar trends with the gate voltage. However, there may be situations in which this model (9) cannot be applied. This may indicate the presence of local non-uniformities, bulk charge traps, grain boundary traps of the organic active layer and traps in the interface with the gate insulator that can vary between the contact region and the conducting channel. Stress produced by thermal annealing may lead to a different molecular reorganization at the contact and the conducting active regions. In our study, we analyze how the relation between M_m and V_G varies with the annealing temperature. The evolution of the relation $M_m(V_G)$ with the annealing temperature provides a way to detect anomalies in the distribution of mobile charges along the organic material of the transistor, including the contact region.

The combination of (1), (8) and (9) results in a compact model that has been tested successfully in the past in OTFTs under different operating conditions (such as bias, temperature, hysteresis)[41,42,50,51]. Its applicability has also been checked in two dimensional field effect transistors in which the contact effects clearly affect the device performance[52,53]. This model is now applied to characterize the set of output and transfer characteristics of the PdPc$_6$ based OTFTs with active layers annealed at four different temperatures.

2. Parameter extraction

Figure 4 shows the **reproducible** output characteristics for the OTFTs measured at room temperature in terms of drain-source current, I_D, as a function of drain voltage, V_D, for gate voltages, V_G, varying between -10 and -50 V with a -10 V step. Figure 5 shows transfer characteristics for the same set of transistors in terms of drain-source current as a function of gate voltage for two values of the drain-voltage, $V_D = -5$ and -40 V. In

both set of figures, the experimental data are shown with symbols and the calculations following model (1) and (8) are shown with lines. The values of the parameters μ_o, γ and V_T and the $I_D - V_C$ curves were extracted following the characterization procedure described in Ref.[29]. The values of the parameters μ_o, γ and V_T are shown in Table I and the contact $I_D - V_C$ curves used in the calculation are represented with solid lines in Figure 6. The $I_D - V_C$ curves that make model (1) exactly match the experimental data of Figure 4 and Figure 5 are represented with symbols in Figure 6. These curves in symbols are obtained by introducing the experimental data, and the extracted values of μ_o, γ and V_T, in (4). The contact $I_D - V_C$ curves extracted from (4) (symbols) follow the trend given in (8) (solid lines). This comparison is necessary in order to check the physical viability of the results[29]. The parameters m and M_m define the solid lines in Figure 6. The parameter m takes the values 1.3, 1.0, 1.4, 1.4 and 1.3 for the as-prepared, 50 °C, 100 °C, 150 °C and 200 °C annealing temperatures, respectively. Non-linear contact effects are obtained for all the cases ($m > 1$) except for the 50 °C temperature ($m = 1$). The values of M_m, which depend on the gate voltage, are represented with symbols in Figure 7. The relation $M_m(V_G)$ can be reproduced with (9) for the as-prepared, 150 °C and 200 °C cases, but not for the 50 °C and 100 °C cases.

The evolution with the annealing temperature of the on-off current ratio, the mobility, μ_o, the threshold voltage, V_T, and an estimated mean value of the contact-voltage, $V_{S,aver}$, are represented in Figure 8. The mean value $V_{S,aver}$ is evaluated by averaging the contact voltage obtained at a constant value of the drain-terminal voltage ($V_D = -6$ V) and different values of the gate voltage. This definition of the mean value for the contact voltage $V_{S,aver}$ must be considered with care as several variables are involved in the nonlinear relation $V_C(I_D, V_G)$ (see (8) and Figure 6).

Overall, the mobility increases when the annealing temperature increases (Figure 8c). Initially, there is a one-order of magnitude increase at 50 °C. Then, it increases more slowly up to 150 °C, where a decrement is detected. At 200 °C, the mobility increases again. The on-off current ratio (Figure 8d) deteriorates with the thermal annealing until 150 °C where the on-off current ratio starts improving.

The evolution of the threshold voltage with the annealing temperature (Figure 8a) shows key transitions at the same temperatures as the mobility does. The as-prepared transistor has a value of the threshold voltage around +9 V (low negative value). The threshold value changes to high negative values (around -8 V) when the annealing temperature increases. This high negative value is maintained until 150 °C, in which the threshold voltage recovers the low negative value around +9 V (the notation "high" and "low" is referred to negative values; note the minus sign in the drain and gate voltages for these p-type transistors).

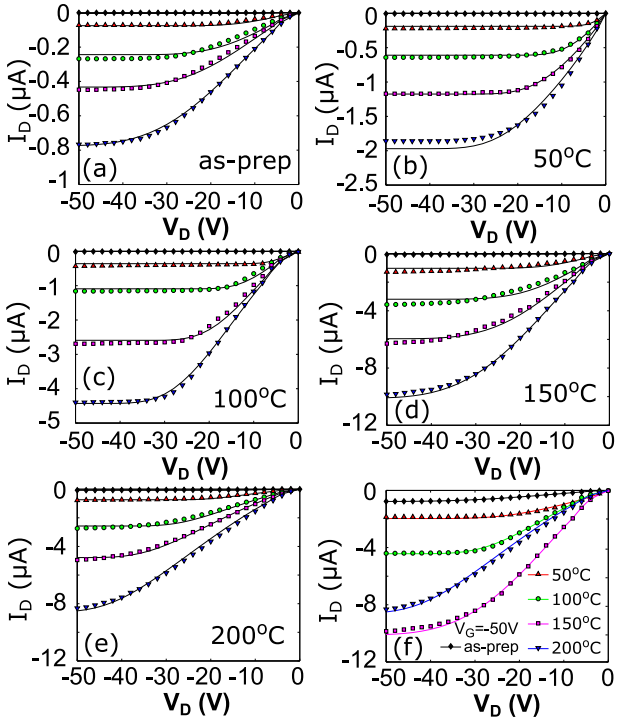

FIG. 4. (a)-(e) Comparison of experimental (symbols) and calculated (solid lines) output characteristics in PdPc$_6$ OTFTs at different gate voltages (from top to bottom, V_G is swept from -10 to -50 V with a -10 V step) and different annealing temperatures: (a) As-prepared, (b) 50 °C, (c) 100 °C, (d) 150 °C and (e) 200 °C. (f) Output characteristics at $V_G = -50$ V at different annealing temperatures.

Figure 8b shows the evolution of the mean value $V_{S,aver}$. The values of $V_{S,aver}$ and V_T show complementary trends: when the threshold voltage takes low or high negative values, $V_{S,aver}$ takes high or low negative values, respectively. An increment of one of these two variables is compensated with a decrement of the other one. This compensation between these two variables is visible after the analysis of Figure 9. This figure shows with symbols the H_{VG} function (2) calculated from the transfer characteristics measured in the OTFTs in the saturation region (Figure 5b). The solid line is the fitting with (3). The slope and intercept of the lines are very similar for all the annealed transistors. This means a similar evolution of the mobility with the gate voltage (controlled with parameter γ), and similar values for $V_T + V_S$. As mentioned before, V_S is not a constant value. However, it is significant how all the H_{VG} functions in Figure 9 intercept the x-axis at similar values of $V_T + V_S$ (second row from the bottom in Table I). This experimental result confirms the observation extracted from the analysis of Figures 8a-b, in which annealed samples show a combination of a high threshold voltage and a low average contact voltage or just the opposite, a low threshold voltage and a high average contact voltage (referred to negative values).

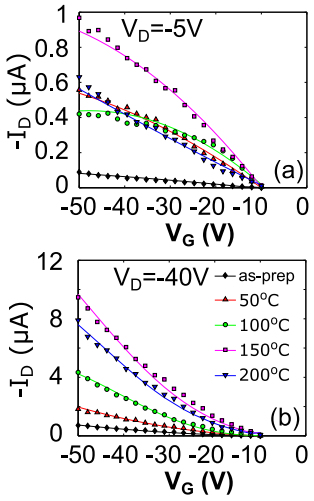

FIG. 5. Comparison of experimental (symbols) and calculated (solid lines) transfer characteristics at different drain voltages V_D in PdPc$_6$ OTFTs annealed at different temperatures: (a) $V_D = -5$ V, (b) $V_D = -40$ V.

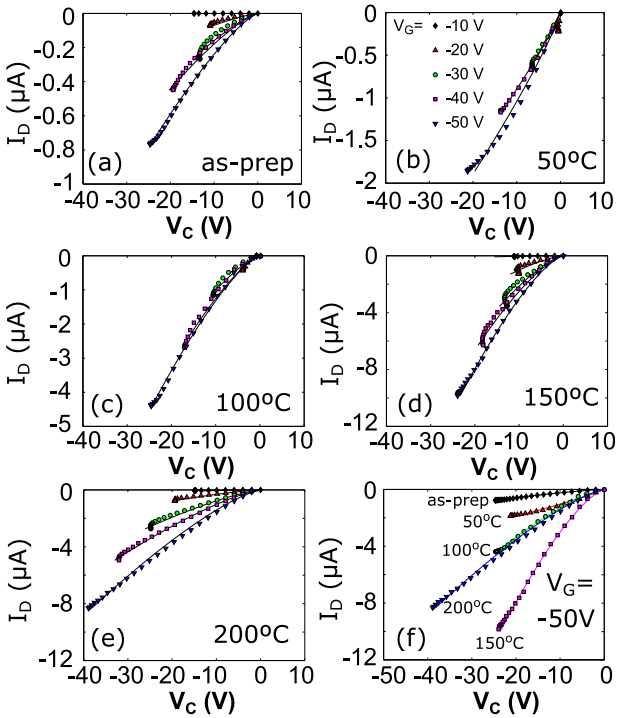

FIG. 6. (a)-(e) Current voltage curves at the contact at different gate voltages (from top to bottom, V_G is swept from -10 to -50 V with a -10 V step) and annealing temperatures: (a) As-prepared, (b) 50 °C, (c) 100 °C, (d) 150 °C and (e) 200 °C. (f) Current voltage curves at $V_G = -50$ V and different annealing temperatures. The symbols are extracted from (4) using the experimental output characteristics and the values of the parameters V_T, μ_o and γ given in Table I. The solid lines follow our model (8) for the contact region.

The origin of large variations of the threshold voltage of an OTFT (as seen in Figure 8a) can be associated to variations of the density of traps in the organic material[42,54,55]. The molecular reorganization produced by the annealing in the organic material can create or eliminate traps. After the analysis of Figure 7, changes in the trap density are expected to take place at 50 °C and 100 °C. Figure 7 shows with symbols the evolution of the parameter M_m with the gate voltage, which was extracted from our fitting procedure. The lines show the trend that M_m would follow according to (9) for the as-prepared, 150 °C and 200 °C samples, with α_m and V_T shown in the eighth and ninth rows of Table I. The lines intercept at gate voltages close to the threshold voltage used in the model (1) and (8) for their respective samples (fifth row of Table I). The deviation from the trend (9) for the 50 °C and 100 °C cases can be explained by a non-uniform molecular readjustment produced by the annealing along the organic material, being different in the active conducting channel and the contact region. This would also explain the large variation in the threshold voltage produced at 50 °C and 100 °C.

C. Discussion. Comparison of characterization techniques

The combined analysis of the electrical variables and parameters of the transistor shows that one group (mobility and contact voltage) improves its values at low annealing temperatures (50-100 °C) and other group (threshold voltage and on-off current voltage) deteriorates its values in this same temperature range. At 150 °C, an inflection point occurs as these trends are reversed. At 200 °C, a new change in the trend of some variables is observed. Changes in the trends observed in the evolution of different parameters with the annealing temperature occur mainly at 150 °C and 200 °C, just coinciding with the range where the onset of liquid crystallinity is observed.

An overall picture of the electrical performance of the annealed transistors can be seen in Figure 4f, in which a comparison of measured (symbols) and calculated (lines) output characteristic of the five transistors at $V_G = -40$ V is shown. The best performance is obtained for the 150 °C temperature. The drain current increases with the annealing temperature up to 150 °C. For higher temperatures, the current starts decreasing. This is confirmed with the study of the transfer characteristics measured (symbols) and calculated (lines) at $V_D = -5$ and -40 V (Figure 5). The worst scenario is observed at 200 °C. This is due to a deterioration of the contact region, despite the carrier mobility is the highest at this temperature. The deterioration of the contact region at 200 °C is clearly observed in Figure 6f.

The description of what is happening when the annealing temperature is increased is the following: at low annealing temperatures (50-100 °C) the mobility increases, the contact effects are reduced but some molecular reorganization modifies the trap density along the semiconductor, affecting differently the active channel and

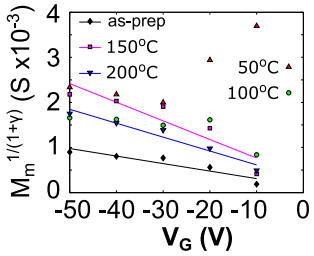

FIG. 7. Extracted values of M_m (symbols). The lines show the trend that M_m would follow according to (9) for the as prepared, 150 °C and 200 °C samples. The lines intercept at gate voltages close to the threshold voltage used in the model (1) for their respective samples (fifth row of Table I). The deviation from the trend (9) for the 50 °C and 100 °C cases can be explained by a non-uniform molecular readjustment produced by the annealing along the organic material, including the active conducting channel and the contact region.

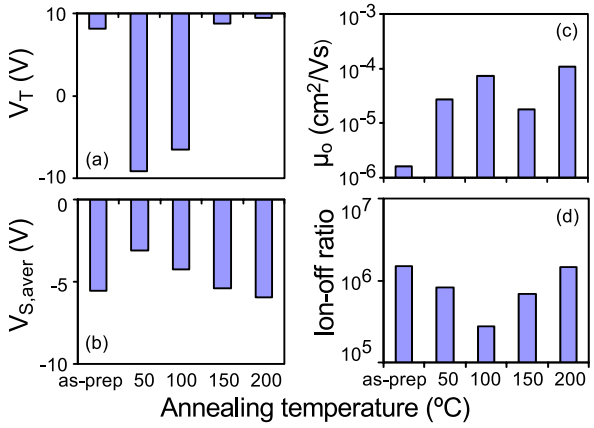

FIG. 8. Comparative study of the annealed devices. (a) Threshold voltage V_T; (b) averaged contact voltage determined at a constant value of the applied drain-terminal voltage $V_D = -6$ V and varying the gate voltage; (c) mobility evaluated at $V_{GT} = V_G - V_T = 1$V [$\mu(V_{GT} = 1$ V)$= \mu_o$ in cm^{2}V^{-1}s^{-1}]; and (d) on-off current ratio.

the contact region. This non-uniform redistribution of traps produces a change in the value of the threshold voltage toward higher negative values. At 150 °C, coinciding with the transition peak associated to the recrystallization of PdPc$_6$ (Figure 2), the semiconductor seems to reorganize uniformly the existing traps and the threshold voltage recovers a low negative value (positive in this case). A low negative threshold voltage and a high value of the mobility makes the $I_D - V_D$ curves increase dramatically. At 200 °C, the mobility is high, and the threshold voltage maintains its positive value. Despite these favorable factors, the transition at this temperature worsens critically the contact $I_D - V_C$ curves, making the $I_D - V_D$ curves decrease well under the optimum situation achieved at 150 °C. This can be explained by a decrease of the free to total charge density θ (and thus of the value of M_m in (8)) at 200 °C annealing temperature. A lower value of θ, can be associated to a creation of a higher number of traps or defects coinciding with the crystal to mesophase transition detected in Figure 2.

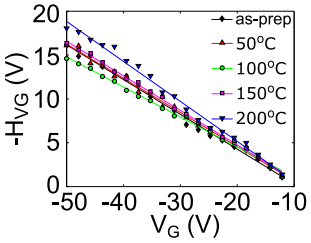

FIG. 9. H_{VG} function extracted from transfer characteristics measured at $V_D = -40$ V in the set of annealed samples. The solid line is the fitting with (3). The grouping of all the curves indicate similar values for the parameters $V_T + V_S$ and γ in (3).

The electrical characterization of annealed PdPc$_6$-based OTFTs agrees well with the DSC studies of the PdPc$_6$ semiconductor. Main changes in the evolution of electrical parameters with the annealing temperature (Figure 8) coincide with the transitions observed in the DSC study (Figure 2).

The study made in this work on PdPc$_6$ semiconductors can be extrapolated to other phthalocyanines such as the CuPc$_6$ materials studied in a previous work[12]. A comparative study between our PdPc$_6$ samples and the CuPc$_6$ devices[12] shows that the main differences between PdPc$_6$ and CuPc$_6$ are observed in the values of the transition temperatures detected in the DSC scans: the initial broad endothermic transition attributed to the crystal to columnar mesophase transition observed in the PdPc$_6$ DSC scan is 12 ^{o}C higher than in the CuPc$_6$ case[12] and the intense peak observed during the cooling cycle for the PdPc$_6$ is 12 ^{o}C lower than in the CuPc$_6$ case[12] implying a more stable mesophase is formed for PdPc$_6$. These differences are correlated with the differences in the electrical characteristics of PdPc$_6$ and CuPc$_6$ transistors. The evolution of the output characteristics $I_D - V_D$ with the annealing temperature is similar for both transistors. Overall, when the annealing temperature increases, the drain current starts to increase, reaches a maximum at a certain temperature, and then decreases (see Figure 4(f) for PdPc$_6$ and Figure 5[12] for CuPc$_6$). The difference between PdPc$_6$ and CuPc$_6$ transistors is just the value of this maximum, which is higher for the PdPc$_6$ case, in agreement with the also higher temperature at which the crystal to columnar mesophase transition takes place. Values of the order of tens of microamperes are obtained in PdPc$_6$ and CuPc$_6$[12] transistors, being slightly greater for the CuPc$_6$ transistors. Accordingly, the values of the carrier mobility should be slightly higher in the CuPc$_6$ than in the PdPc$_6$. The values of the carrier mobil-

ity determined experimentally should also reflect this fact. However, this would occur only if the same extraction procedures and electrical models were used in both cases. Otherwise, if the value of the carrier mobility is extracted without considering the contacts effects, this value can be overestimated several orders of magnitude as demonstrated in[50]. This would explain the differences reported for the values of the carrier mobility in $CuPc_6$ transistors[12] and the ones reported for the $PdPc_6$ transistors in this work.

IV. CONCLUSIONS

Annealed OTFTs based on a solution-processable material with a thermotropic mesophase, $PdPc_6$, have been investigated. The combined analysis of the electrical characteristics of annealed $PdPc_6$-based OTFTs and differential scanning calorimetry on $PdPc_6$ bulk materials has established a relation between the morphologic changes produced in the organic materials and the electrical parameters of the transistor. Annealing at low temperatures produces an increment of the charge carrier mobility and also a modification in the number of traps that increases the value of the threshold voltage. Their combined effect is the origin of electrical changes in the transistors. At intermediate annealing temperatures, close to but below the transition to a columnar liquid crystal, the transistor operates in optimal conditions with the highest values of the drain current. At higher annealing temperatures, the transistors deteriorate due to an increase of the contact effects, even though the values of the carrier mobility and threshold voltage are favorable to achieve high currents in the transistor. This deterioration takes place at a temperature where $PdPc_6$ forms exclusively its columnar mesophase. Overall, the combination of different characterization techniques allows for finding the optimum annealing temperature for the best electrical performance. In this study, the use of a compact model that takes into account the contact effects of the transistor has been essential for establishing the link between morphological and electrical changes in annealed transistors. **Solution processed $PdPc_6$ molecules can be exploited for low cost fabrication of active devices for large area display and sensor technologies.**

ACKNOWLEDGMENTS

This work was partially supported by MINECO of Spain under research Project MAT2016-76892-C3-3-R. Experimental work was carried out at Queen Mary, University of London under financial support from the UK Technology Strategy Board (Project No: TP/6/EPH/6/S/K2536J). The pre-patterned transistor substrates were prepared by QUDOS Technology, Rutherford Appleton Laboratory, Didcot, UK. The authors are grateful to Dr Craig E. Murphy and Dr Markys G. Cain of the National Physical Laboratory, Hampton Road, Teddington, Middlesex UK for fruitful discussions.

[1] C. Lu, Z. Ji, G. Xu, W. Wang, L. Wang, Z. Han, L. Li, and M. Liu, "Progress in flexible organic thin-film transistors and integrated circuits," Sci. Bull. **61**, 1081 – 1096 (2016).

[2] A. Yamamura, H. Matsui, M. Uno, N. Isahaya, Y. Tanaka, M. Kudo, M. Ito, C. Mitsui, T. Okamoto, and J. Takeya, "Painting integrated complementary logic circuits for single-crystal organic transistors: A demonstration of a digital wireless communication sensing tag," Adv. Electron. Mater. **3**, 1600456–n/a (2017), 1600456.

[3] X. Guo, Y. Xu, S. Ogier, T. N. Ng, M. Caironi, A. Perinot, L. Li, J. Zhao, W. Tang, R. A. Sporea, A. Nejim, J. Carrabina, P. Cain, and F. Yan, "Current status and opportunities of organic thin-film transistor technologies," IEEE Trans. Electron Devices **64**, 1906–1921 (2017).

[4] B. Kumar, B. K. Kaushik, and Y. S. Negi, "Organic thin film transistors: Structures, models, materials, fabrication, and applications: A review," Polym. Rev. **54**, 33–111 (2014).

[5] M. Mamada, H. Shima, Y. Yoneda, T. Shimano, N. Yamada, K. Kakita, T. Machida, Y. Tanaka, S. Aotsuka, D. Kumaki, and S. Tokito, "A unique solution-processable n-type semiconductor material design for high-performance organic field-effect transistors," Chem. Mater. **27**, 141–147 (2015).

[6] M. Gsänger, D. Bialas, L. Huang, M. Stolte, and F. Würthner, "Organic semiconductors based on dyes and color pigments," Adv. Mater. **28**, 3615–3645 (2016).

[7] G. de la Torre, G. Bottari, and T. Torres, "Phthalocyanines and subphthalocyanines: Perfect partners for fullerenes and carbon nanotubes in molecular photovoltaics," Adv. Energy Mater. **7**, 1601700–n/a (2017), 1601700.

[8] D. Mukherjee, R. Manjunatha, S. Sampath, and A. Ray, "Materials for chemical sensing," (Springer, 2017) Chap. Phthalocyanines as Sensitive Materials for Chemical Sensors. In: (eds) . Springer, Cham, pp. 165–226.

[9] Y. Peng, W. Lv, B. Yao, J. Xie, T. Yang, G. Fan, D. Chen, P. Gao, M. Zhou, and Y. Wang, "Improved performance of photosensitive field-effect transistors based on palladium phthalocyanine by utilizing al as source and drain electrodes," IEEE Trans. Electron Devices **60**, 1208–1212 (2013).

[10] A. S. Sukhikh, D. D. Klyamer, R. G. Parkhomenko, P. O. Krasnov, S. A. Gromilov, A. K. Hassan, and T. V. Basova, "Effect of fluorosubstitution on the structure of single crystals, thin films and spectral properties of palladium phthalocyanines," Dyes Pigments **149**, 348 – 355 (2018).

[11] A. D. Garland, I. Chambrier, A. N. Cammidge, and M. J. Cook, "Design and synthesis of liquid crystalline phthalocyanines: combinations of substituents that promote the discotic nematic mesophase," Tetrahedron **71**, 7310 – 7314 (2015), special Memorial Issue for Professor Alan Katritzky.

[12] N. B. Chaure, C. Pal, S. Barard, T. Kreouzis, A. K. Ray, A. N. Cammidge, I. Chambrier, M. J. Cook, C. E. Murphy, and M. G. Cain, "A liquid crystalline copper phthalocyanine derivative for high performance organic thin film transistors," J. Mater. Chem. **22**, 19179–19189 (2012).

[13] Y. Jiang, Y. Gao, H. Tian, J. Ding, D. Yan, Y. Geng, and F. Wang, "Synthesis and characterization of isoindigo[7,6-g]isoindigo-based donor-acceptor conjugated polymers," Macromolecules **49**, 2135–2144 (2016).

[14] Y.-J. Lin and H. Tsao, "Ambient-atmosphere annealing effect on the carrier conduction behavior based on the linear-regime transfer characteristics of pentacene thin film transistors," Microelectron. Eng. **149**, 57 – 61 (2016).

[15] M. J. Kim, M. Jung, W. Kang, G. An, H. Kim, H. J. Son,

B. Kim, and J. H. Cho, "Well-balanced carrier mobilities in ambipolar transistors based on solution-processable low band gap small molecules," J. Phys. Chem. C **119**, 16414–16423 (2015).
[16]B. Sun, W. Hong, Z. Yan, H. Aziz, and Y. Li, "Record high electron mobility of 6.3 $cm^2v^{-1}s^{-1}$ achieved for polymer semiconductors using a new building block," Adv. Mater. **26**, 2636–2642 (2014).
[17]J. Y. Na, M. Kim, and Y. D. Park, "Solution processing with a good solvent additive for highly reliable organic thin-film transistors," J. Phys. Chem. C **121**, 13930–13937 (2017).
[18]M. Pandey, S. Nagamatsu, W. Takashima, S. S. Pandey, and S. Hayase, "Interplay of orientation and blending: Synergistic enhancement of field effect mobility in thiophene-based conjugated polymers," J. Phys. Chem. C **121**, 11184–11193 (2017).
[19]D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S. Shur, "An experimental study of contact effects in organic thin film transistors," J. Appl. Phys. **100**, 024509–1–024509–13 (2006).
[20]S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi, "Contact-metal dependent current injection in pentacene thin-film transistors," Appl. Phys. Lett. **91**, 203508 (2007).
[21]M. J. Deen, M. H. Kazemeini, and S. Holdcroft, "Contact effects and extraction of intrinsic parameters in poly(3-alkylthiophene) thin film field-effect transistors," J. Appl. Phys. **103**, 124509–1–124509–7 (2008).
[22]P. Lara Bullejos, J. A. Jiménez Tejada, S. Rodríguez Bolívar, M. J. Deen, and O. Marinov, "Model for the injection of charge through the contacts of organic transistors," J. Appl. Phys. **105**, 084516 (2009).
[23]F. Torricelli, M. Ghittorelli, M. Rapisarda, A. Valletta, L. Mariucci, S. Jacob, R. Coppard, E. Cantatore, Z. Kovács-Vajna, and L. Colalongo, "Unified drain-current model of complementary p- and n-type otfts," Org. Electron. **22**, 5–11 (2015).
[24]A. Valletta, M. Rapisarda, S. Calvi, G. Fortunato, M. Frasca, G. Maira, A. Ciccazzo, and L. Mariucci, "A dc and small signal ac model for organic thin film transistors including contact effects and non quasi static regime," Org. Electron. **41**, 345–354 (2017).
[25]J. Li, W. Ou-Yang, and M. Weis, "Electric-field enhanced thermionic emission model for carrier injection mechanism of organic field-effect transistors: understanding of contact resistance," J. Phys. D: Appl. Phys. **50**, 035101 (2017).
[26]H. Karimi-Alavijeh and A. Katebi-Jahromi, "An analytical solution for contact resistance of staggered organic field-effect transistors," J. Appl. Phys. **121**, 105501 (2017).
[27]O. Fenwick, C. Van Dyck, K. Murugavel, D. Cornil, F. Reinders, S. Haar, M. Mayor, J. Cornil, and P. Samori, "Modulating the charge injection in organic field-effect transistors: fluorinated oligophenyl self-assembled monolayers for high work function electrodes," J. Mater. Chem C **3**, 3007–3015 (2015).
[28]O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, "Organic thin-film transistors: Part I-compact dc modeling," IEEE Trans. Electron Devices **56**, 2952–2961 (2009).
[29]J. A. Jiménez Tejada, J. A. López Villanueva, P. López Varo, K. M. Awawdeh, and M. J. Deen, "Compact modeling and contact effects in organic transistors," IEEE Trans. Electron Devices **61**, 266–277 (2014).
[30]N. B. McKeown, I. Chambrier, and M. J. Cook, "Synthesis and characterisation of some 1,4,8,11,15,18,22,25-octa-alkyl- and 1,4,8,11,15,18-hexa-alkyl-22,25-bis(carboxypropyl)phthalocyanines," J. Chem. Soc., Perkin Trans. 1 , 1169–1177 (1990).
[31]N. B. Chaure, A. N. Cammidge, I. Chambrier, M. J. Cook, M. G. Cain, C. E. Murphy, C. Pal, and A. K. Ray, "High-mobility solution-processed copper phthalocyanine-based organic field-effect transistors," Sci. Technol. Adv. Mater. **12**, 025001 (2011).
[32]A. N. Cammidge, I. Chambrier, M. J. Cook, E. H. Langner, M. Rahman, and J. C. Swarts, "Characterization, liquid crystallinity and spin-coated films of some metalated 1,4,8,11,15,18,22,25-octaalkyl tetrabenzo [b,g,l,q][5,10,15]triazaporphyrin derivatives," J. Porphyr. Phthalocya. **15**, 890–897 (2011).
[33]A. S. Cherodian, A. N. Davies, R. M. Richardson, M. J. Cook, N. B. McKeown, A. J. Thomson, J. Feijoo, G. Ungar, and J. Harrison, "Mesogenic behaviour of some 1,4,8,11,15,18,22,25-octa-alkylphthalocyanines," Mol. Cryst. Liq. Cryst. **196**, 103–114 (1991).
[34]X. Tian, Z. Xu, F. Zhang, S. Zhao, G. Yuan, J. Li, Q. Sun, and Y. Wang, "Influence of thermal treatment on the performance of copper phthalocyanine thin-film transistors," Curr. Appl. Phys. **10**, 129 – 132 (2010).
[35]C. H. Kim, A. Castro-Carranza, M. Estrada, A. Cerdeira, Y. Bonnassieux, G. Horowitz, and B. Iniguez, "A compact model for organic field-effect transistors with improved output asymptotic behaviors," IEEE Trans. Electron Devices **60**, 1136–1141 (2013).
[36]L. Li, M. Debucquoy, J. Genoe, and P. Heremans, "A compact model for polycrystalline pentacene thin-film transistor," J. Appl. Phys. **107**, 024519 (2010).
[37]B. Yaglioglu, T. Agostinelli, P. Cain, S. Mijalkovîc, and A. Nejim, "Parameter extraction and evaluation of uotft model for organic thin-film transistor circuit design," J. Disp. Technol. **9**, 890–894 (2013).
[38]L. Bürgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, "Close look at charge carrier injection in polymer field-effect transistors," J. Appl. Phys. **94**, 6129–6137 (2003).
[39]A. Cerdeira, M. Estrada, R. García, A. Ortiz Conde, and F. García Sánchez, "New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions," Solid-State Electron. **45**, 1077 – 1080 (2001).
[40]M. J. Deen, O. Marinov, U. Zschieschang, and H. Klauk, "Organic Thin-Film Transistors: Part II. Parameter Extraction," IEEE Trans. Electron Devices **56**, 2962 –2968 (2009).
[41]J. Jiménez Tejada, K. M. Awawdeh, J. A. López Villanueva, J. E. Carceller, M. J. Deen, N. B. Chaure, T. Basova, and A. K. Ray, "Contact effects in compact models of organic thin film transistors: Application to zinc phthalocyanine-based transistors," Org. Electron. **12**, 832 – 842 (2011).
[42]K. M. Awawdeh, J. A. Jiménez Tejada, P. López Varo, J. A. López Villanueva, F. M. Gómez Campos, and M. J. Deen, "Characterization of organic thin film transistors with hysteresis and contact effects," Org. Electron. **14**, 3286 – 3296 (2013).
[43]P. Lara Bullejos, J. A. Jiménez Tejada, M. J. Deen, O. Marinov, and W. R. Datars, "Unified model for the injection and transport of charge in organic diodes," J. Appl. Phys. **103**, 064504–1–064504–12 (2008).
[44]P. Lara Bullejos, J. A. Jiménez Tejada, F. M. Gómez-Campos, M. J. Deen, and O. Marinov, "Evaluation of the charge density in the contact region of organic thin film transistors," J. Appl. Phys. **106**, 094503–1–094503–4 (2009).
[45]P. López Varo, J. Jiménez Tejada, J. López Villanueva, J. Carceller, and M. Deen, "Modeling the transition from ohmic to space charge limited current in organic semiconductors," Org. Electron. **13**, 1700 – 1709 (2012).
[46]T. J. Richards and H. Sirringhaus, "Analysis of the contact resistance in staggered, top-gate organic field-effect transistors," J. Appl. Phys. **102**, 094510 (2007).
[47]M. Marinkovic, D. Belaineh, V. Wagner, and D. Knipp, "On the origin of contact resistances of organic thin film transistors," Adv. Mater. **24**, 4005–4009 (2012).
[48]Y. Xu, T. Minari, K. Tsukagoshi, J. A. Chroboczek, and G. Ghibaudo, "Direct evaluation of low-field mobility and access resistance in pentacene field-effect transistors," J. Appl. Phys. **107**, 114507 (2010).
[49]B. G. Streetman, *Solid State Electronic Devices* (Prentice-Hall, Englewood Cliffs, NJ, 1980).
[50]J. A. Jiménez Tejada, P. López Varo, A. N. Cammidge, I. Chambrier, M. J. Cook, N. B. Chaure, and A. K. Ray, "Compact modeling of organic thin-film transistors with solution processed octadecyl substituted tetrabenzotriazaporphyrin as an ac-

tive layer," IEEE Trans. Electron Devices **64**, 2629–2634 (2017).
[51]M. Fayez, K. M. Morsi, and M. N. Sabry, "Otfts compact models: analysis, comparison, and insights," IET Circ. Device. Syst. **11**, 409–420 (2017).
[52]K. D. Holland, A. U. Alam, N. Paydavosi, M. Wong, C. M. Rogers, S. Rizwan, D. Kienle, and M. Vaidyanathan, "Impact of contact resistance on the f_t and $f_{\max}$ of graphene versus MoS_2 transistors," IEEE Trans. Nanotechnol. **16**, 94–106 (2017).
[53]S. V. Suryavanshi and E. Pop, "S2ds: Physics-based compact model for circuit simulation of two-dimensional semiconductor devices including non-idealities," J. Appl. Phys. **120**, 224503 (2016).
[54]G. Horowitz and P. Delannoy, "An analytical model for organic-based thin-film transistors," J. Appl. Phys. **70**, 469–475 (1991).
[55]J. H. Schön and B. Batlogg, "Modeling of the temperature dependence of the field-effect mobility in thin film devices of conjugated oligomers," Appl. Phys. Lett. **74**, 260 (1999).