into the pure CUT, that is, there was no additional circuit. The second and third rows, 'D+pMOS' and 'pMOS', show simulation results when using a diode and a pMOS of the same size as the proposed sensor, and when using a pMOS one-quarter the size of M1 as the I-V translator, respectively. The last row, 'proposed', shows the results for the proposed sensor, which reduces the voltage drop at the VDD terminal of the CUT. It also performs relatively accurate measurement for a small current (i.e. relative error for 100kΩ fault resistance was 3.5%). Although the pMOS scheme for the I-V translator showed good performance concerning accurate measurement of a small current, it is difficult to apply the translator because it produces a small voltage drop and has a small noise margin.

Table 1: Summary of IDDQ sensors

Load for CUT	Fault resistance (R_f)		
	100kΩ	10kΩ	10Ω
CUT only	48.4/ -	361.3/ -	822.5/ -
D+*p*MOS	43.3/0.52	315.3/0.59	736.9/0.64
*p*MOS	47.8/0.06	330.2/0.40	677.5/0.87
Proposed	46.6/0.19	318.6/0.54	742.8/0.61

I_f [μA]/voltage drop at N1 [V]

Fig. 3 shows simulated waveforms for the proposed sensor. The fault in the CUT was excited at two intervals: from 50 to 100ns and from 200 to 250ns. The output of the sensor produced a high voltage at both these intervals. The line of Inv(T_{out}) in the Figures shows the output of an inverter fed by T_{out}. The propagation delay times of Inv(T_{out}) were 23.8ns for R_f = 100kΩ and 3.3ns for R_f = 10Ω. Thus the fault detection time of the sensor becomes slower as the fault current decreases.

Conclusions: A sensor with low voltage drop and accurate current measurement is proposed for IDDQ testing. Simulation results showed that this sensor satisfied the primary objective, but was not fast enough in the case of smaller fault current. This will be a subject of future research.

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Lithographic technology for microwave integrated circuits

P.R. Shepherd, P.S.A. Evans, B.J. Ramsey and D.J. Harrison

Indexing terms: Microwave integrated circuits, Lithography

Conductive lithographic films (CLFs) have been developed primarily as substitutes for resin/laminate boards, which share properties with the metallisation patterns used in planar microwave integrated circuits (MICs). The authors examine the microwave properties of the films and show that, although the losses are greater, they have potential as an alternative to the traditional manufacturing process of MICs.

Introduction: Conductive lithographic films (CLFs) are fabricated on paper substrates using a specially formulated silver-loaded ink and a standard lithographic printing process [1]. The resulting ink films consists of a thin layer (~3μm) of silver particles suspended in an organic resin binder. The pattern can be overprinted, with excellent registration, to achieve thicker layers if required. CLFs were developed primarily as an alternative to traditional resin/laminate boards for low frequency applications and have already been successfully tested in a range of telephone plant, microprocessor and security tagging applications.

The structure of the printed films is however very similar to the metallisations used in planar microwave integrated circuits (MICs). The use of CLFs in MICs or other planar structures has two main perceived advantages. First, owing to the simple printing process, it is likely to provide a cheaper manufacturing process for bulk applications. Secondly, owing to their flexible nature, CLF substrates can be readily bonded to curved substrates, whereas curved circuits are difficult to achieve in the standard MIC process. This could have applications in certain antenna structures (e.g. helical antennas or dipoles on co-axial feeds). The perceived disadvantages are that there is still a requirement for a base substrate onto which the paper is bonded. This is because the very thin paper substrate would require extremely narrow metallisation patterns to achieve suitable characteristic impedances. The second perceived disadvantage is in the loss of the films being higher than traditional MIC metallisations (e.g. copper).

Conductive lithographic films: In the CLF fabrication process, a conductive ink is deposited by a standard lithographic printing press to directly form circuit patterns on the substrate material. The ink developed for the CLF printing process consists of suspension of metallic silver particles in an organic resin. Although this resin is non-conductive, it acts as a vehicle for the conductive particles and partly determines the mechanical properties of the ink. The current ink formulation contains a high proportion (~80% w/w) of silver flake with a mean particle size of ≤ 1μm. The substrate material consists of a paper or polymer base, whose surface properties permit the adhesion of the ink, and allows contact between adjacent ink particles. Gloss art paper, and coated polyethylene have been used in printing trials.

Work to date has clearly demonstrated that standard lithographic printing technology can be adapted to electronic circuit fabrication. Printing trials have yielded ink films deposited onto paper substrates which have acceptable electrical characteristics. Typical CLF sheet resistivities approach those encountered in thick-film circuit practice, and CLF substrates have been assembled into a range of functional electronic systems.

Interest in the microwave properties of CLFs has arisen as a consequence of the similarity of deposited films to the metallisation patterns employed in MICs. In particular, the films exhibit a high degree of electrical conductivity, a surface roughness equivalent to the mean ink particle size (1 μm), and, in consequence of the lithographic printing process, excellent dimensional control and registration of the deposited ink films.

Microwave test circuits: Two basic circuit forms were generated for assessment of the CLFs, nominally 50Ω through lines of different lengths and a ring resonator structure. The same photolithographic artwork was used to construct the through lines on

standard copper-clad Duroid samples as well as the CLF patterns, for direct comparison of the characteristics.

For measurement purposes the paper CLF substrate was bonded onto a Duroid substrate which had had the top copper layer removed, but retained the copper ground plane. Clearly the additional paper thickness and higher dielectric constant of this layer will mean that the CLF line will no longer be 50Ω, but part of this work was to assess the change in effective dielectric constant from the pure Duroid line.

The samples were measured using an HP8510B vector network analyser. This was calibrated in 3.5mm coax, so the effect of the microstrip launchers is included in the measured results. By having identical structures, but of different lengths, and assuming the launcher characteristics are reasonably repeatable, it is assumed that these effects can be accounted for in the assessment [2]. Effectively we can use the copper-clad Duroid as a calibration standard to assess the loss characteristics of the CLF lines.

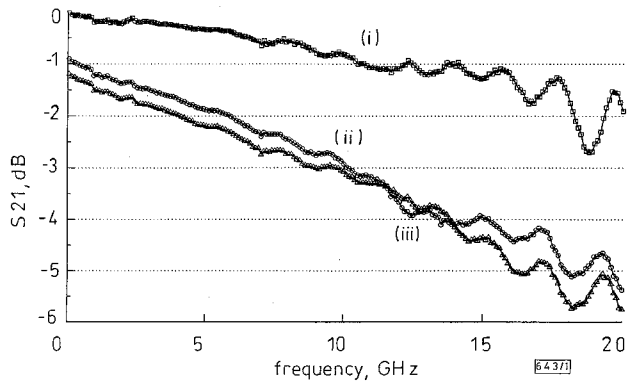

Fig. 1 *Measured S_{21} for 2in through lines*

(i) copper
(ii) cured CLF
(iii) uncured CLF

Results and discussion: Fig. 1 shows the measured S_{21} for the through line on a 2 in long substrate. The top trace shows the normal copper clad Duroid and shows an increasing loss to ~2dB at 20GHz. This is almost entirely due to the launchers as the expected loss in such structures increases to around 0.1dB at 20GHz. The second two traces are for the identical structure in CLF. The 'uncured' measurement is the result taken shortly after the substrate was printed, while the 'cured' trace is taken about 10 days later. This illustrates a trend that is already known in that the conductive properties on the CLF alter with time, taking around a week to settle at room temperature. DC resistance measurements taken on samples at about the same time as the microwave measurements indicated a change in sheet resistance from 0.9 to 0.6Ω/□. This increase in DC conductivity is reflected in a decrease in microwave loss of ~0.3dB across the band.

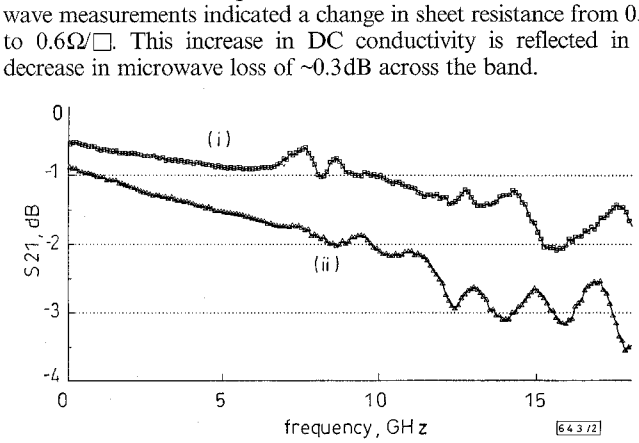

Fig. 2 *S_{21} of CLF lines referenced to copper lines*

(i) 1in line
(ii) 2in line

The ripple in these plots is due to the relatively poor return loss of the microstrip launchers. The reflections which are set up interfere with the forward power wave. The constructive and destructive interference depends on the relative phases of the signals, this in turn depends on the electrical length of the line which is a function of frequency. Hence the ripple effect with frequency. The shape of the ripple in the two measurements is similar, indicating a reasonable repeatability of the mounting fixture. A similar measurement was carried out using a 1in substrate. The CLF lines again show greater loss, the curing process reducing the loss by ~0.1–0.2dB. This is entirely consistent with the results from the 2in substrate where the line was twice the length. Referencing the CLF results to the copper results helps eliminate the launcher ripple and gives a good estimate of the excess loss of the CLF line. Fig. 2 shows these results for the two lengths of line, which indicates that the loss per inch of the CLF microstrip line increases almost linearly from ~0.5dB per inch at DC to ~1.8dB per inch at 18GHz. It may be possible to improve these figures, as previous print runs have had sheet resistances as low as 0.3Ω/□.

Through measurements were also made on the ring resonator structure and the resonant frequencies determined. From these, the effective dielectric constant (EDC) was calculated to be 2.15 for the CLF/Duroid structure. This compares with a figure of 1.89 for a line of the same width on the Duroid substrate. This increase is due to the higher dielectric constant of the paper layer and is consistent with a measured value of 7.5 for the paper at DC. The higher EDC results in a lower value of characteristic impedance for the CLF structure (to ~47Ω) and an electrical length different from the copper line. This is why the ripple is not completely eliminated in Fig. 2, where the referencing procedure relies on the same electrical length and characteristic impedance for both lines.

Conclusions: A new lithographic process (CLF) has been described which is suitable for application to MICs. CLF microstrip structures have been constructed and measured to assess their usefulness at microwave frequencies. The loss of these lines has been estimated at 2dB per inch at 20GHz, which represents a value at the poorest end of the spread of film conductivities which have been measured. While this loss is reasonably high, it would not preclude their use in MICs where the circuits are small or loss is not too important. The perceived advantages of low bulk cost and/or use in curved circuit structures would make the use of CLFs at microwave frequencies a useful alternative for many circuits.

The measurements carried out on the ring resonators have shown that the effective dielectric constant is increased due to the extra paper dielectric layer. This alters the characteristic impedance and electrical length of the lines, but this can be taken into account in the circuit design.

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