Power Switching Device Losses – Simulation and Non-Simulation Methods of Calculations

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***Abstract*— In the design and manufacture of power supplies and converters, commercial factors demand high efficiency figures in the operation and performance of these products. Potential loss areas in the circuits are identified to achieve minimum losses [1] [2]. One of the main component contributing to losses in converters is the switching device.**

The methods to calculate switching loss [3] are complex and involves several related parameters [4] [5]. Conduction loss, radiation interference [6] and temperature rise, impacts on design efficiency. Depending on the design limitations, a balance between the related parameters is necessary, which can be achieved by optimisation processes. Several methods are identified in this paper.

Keywords — Hard Switching, Input-Output Parameters, Losses, Switching Devices, Simulation and Non-Simulation Methods.

I. INTRODUCTION

The switching loss methods, will give the engineer the flexibility of choosing a suitable component for the design application. Size of the switching device is important, since parasitic capacitance is proportional to the dimensions and structure of the device [7]. Comparison between the various methods will enable critical selection between expensive switching devices (IGBTs, MOSFETS), with high performance and low-cost devices with inferior performance. Articles reviewed have referred to the calculation of switching device losses [8] and other procedures involving an optimisation process. Some manufacturers' publications describe their own stand-alone device selection procedures to assist designers in choosing one of their own component or switching device for power applications [9] [10] [11]. Other papers refer to the use of popular, leading-edge application software that covers a range of design, simulation procedures which can include genetic algorithms, artificial intelligence or offer a simpler simulation process using models. Hence it was felt that there was a need to compile as many such methods as shown in Fig. 1.

It is important to determine the total switching loss, in the event of hard switching [12] being used (see Fig.2). The losses due to the high peak voltage and dv/dt oscillations [13] [14] generated across the switch can be damped or removed by Turn-Off RC snubber circuits with an optimised value of time constant [15] [16].

Fig. 2, shows a linear representation of the loss in the switching device during the switch-off transition, represented by the shaded triangular area due to the intersection of the dv/dt and the di/dt gradients. This loss area as in the Linearised Calculation method listed shown in Fig. 1 is explained in the next section.

II. METHODS TO DETERMINE SWITCHING DEVICE LOSSES

A. Non-Simulation method - Linearised calculation on an ideal switch

Fig. 3 shows a solid-state switch in series with an inductive load with a free wheel diode connected in parallel, and an RCD snubber circuit connected across it. The circuit will be used to explain the current and voltage waveforms and the switch losses during the On/Off transitions and the On and Off cycle states of the switch.

Fig. 4, has three sections: -
Section (A), shows the control signal, with the ON and Off periods that closes and opens the switch. Section (B), shows the waveforms for the load current I_L and the switch voltage V_{SW}. Section (C), shows the Power waveform for the losses in the switch during the switching On and Off transitions and the On and Off periods due to the control signal.
Figure 4 (A), shows the switch control signal, with period, T = (t off + t on) and frequency f = 1/T Hz.

Control Signal On – Fig. 4 (B), shows that the switch is initially ON, with a load current I_L and a low 'V_{swON}' voltage drop across it.

At 't_1' the control signal switches to the OFF state. The switch voltage remains at 'V_{swON}' and starts to increase after a delay of '$t_{d(off)}$' from 't_1', and a further delay of 't_{Vrise}' the switch voltage increases to 'V_{swOFF}' (equal to the supply voltage) at a voltage gradient of dv/dt = $(V_{swOFF})/(t_{Vrise})$.

Control Signal Off - At 't_2' the control signal switches to the OFF state, but the switch voltage remains at the '$V_{sw\ OFF}$' level. Since the load is inductive, due to the collapse of the magnetic field there is a delay for the growth of the -Ldi/dt voltage, whilst the diode D1 in Fig. 3 remains forward biased due to 'V_{swOFF}' during the 't_1 to t_2' Off period and maintains a connection between the top end of the switch and the supply voltage (equal to V_{swOFF}). When the -Ldi/dt voltage is equal to the supply voltage, D1 is reversed biased and the switch voltage drops at a negative gradient of dv/dt = $(V_{swOFF})/(t_{Vfall})$ to a low value of 'V_{swON}' volts. This cycle is repeated during the frequency of the control signal.

Current Wave Form Cycle **-** Fig. 4 (B), shows that the switch is initially ON, with a load current I_L flowing through it.

Control Signal Off **-** At 't1' the control signal switches to the OFF state, but the load current I_L is maintained due to the load inductance and starts to decrease (when the switch voltage is at the open circuit level of 'V_{swOFF}') at a negative gradient of di/dt = $I_L/(t_{i\ fall})$ and approaches zero level.

Control Signal On **-** At 't_2', I_L remains at the low level and begins to rise after a delay of '$t_{d(on)}$' at a gradient of di/dt = $I_L/(t_{i\ rise})$ and reaches full load current of I_L and remains at this level for the duration of the On period of the control signal.

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Switch Losses, Transition and Closed States **-** Fig. 4 (C), is the power loss wave form due to the product of I_L and V_{SW} in Fig.4(B). The shaded areas represent this power loss, due to its linear shape it can be estimated by simply using the formula for the area of a triangle. See equations (4) and (5).

Equations derived from Fig.4 (A, B & C).

Equations Key					
OL	Overlap	PL	Power Loss	SW	Switch

(A) Control signal period, $T = (t_{on} + t_{off}) = 1/f$ Hz (1)

(B) Overlap (off) peri^{x}od, $t_{OLoff} = t_{Vrise} + t_{ifall}$ (2)

Overlap (on) period, $t_{OLon} = t_{irise} + t_{Vfall}$ (3)

(C) Switch energy during Turn-Off Transition,

$W_{PLoff} = ½ \times (t_{OLoff}) \times (I_L V_{SW})$ Joules (4)

Switch energy during Turn-On Transition,

$W_{PLon} = ½ \times (t_{OLon}) \times (I_L V_{SW})$ Joules (5)

Power loss in switch/cycle = {(4) + (5)} $\times$ f

$= ½\ I_L\ V_{sw}\ (t_{OLoff} + t_{OLon})\ f$ Watts (6)

$= ½\ I_L\ V_{sw}\ (t_{OLoff} + t_{OLon})\ f$ Watts (7)

And it is observed that,

Power loss $\propto$ the duty cycle $\frac{(t_{Ol\,on} + t_{Ol\,off})}{(t_{on} + t_{off})}$ (8)

Power loss $\propto$ f, (t_{OLon}) and (t_{OLoff}) (9)

Turn-Off loss,

$W_{sw} = V_{swoff} \times I_L$ Joules (10)

(Negligible, due to low leakage current)

Turn-On loss,

$Wsw = V_{sw\ off} \times I_L$ Joules (11)

and the average Power during the On state,

$W_{SW} = I_L \times (V_{sw\ on}) \times (t_{on}/T)$ Joules (12)

Important deductions

Three important deductions are made from this simplified linear voltage and current wave form transitions: -

1 From equation (6), approximate RC components values in the snubber circuit in Fig.3, can be estimated by equating the loss energy from equation (4) or (5) (whichever is greater) to the capacitor energy $1/2C(V_{swoff})^2$ of the snubber circuit [17] [18]. These RC values may be

used as the initial weighted values for an optimisation process.

2 From equation (8), choosing switches with short switching times (t_{OLon}), will dissipate less energy and therefore operate at higher frequencies.

3 From equation (11), adjusting the control switching signal On-period to a small value will minimise the switch loss energy during the On state [1].

B. Design of Switching Device Power model

A simple model is proposed to simulate switching devices (S) instead of using custom designed manufacturers' simulation programmes. These require very small-time steps (< 0.1µs) which would take a long to simulate if the simulation run-time is a few seconds and would also be very expensive. However, the (S) power loss in manufacturer's data sheet will be used to equate the total (S) and diode (D) losses. The power losses for switching devices in a two-level 3-ph voltage source converter (VSC) was considered [19]. Fig. 5 shows one-leg of the VSC and the corresponding model for a switching device. The model shows two resistors R_a to identify the separate losses in (S) and in (D). The (S) on-off switching transients generate high voltage and current spikes for short periods but contains high power. The conduction losses in the on state and the dv/dt, di/dt product loss in both the on and off states need to be considered.

The manufacturers' power loss data (P_{man}) is equated to the losses related to I_{RMS}/ph through (S).

$$\text{i.e. } P_{man} = aI^2_{ph} + bI_{ph} + c, \quad (13)$$

where a, b and c are unknowns. These coefficients can be found during simulations, by varying the I_{ph} for the load range from the data sheet and measuring each simulation power loss as a function of I_{ph}. With at least three power equations (13), "a", "b" and "c" can be found.

In Fig.5, R_a models the power losses due to the $(I_{RMS})^2$ in the (S) and (D) and relates to "a" in (13). R_c models the power losses due to $(V_{DC})^2$ and relates to "c" in (13). Vb models the losses due to the I_{RMS} in the (S) and (D) relates to "b" in (13).

Computation of the Model parameters R_a, R_c and V_b. Equating the phase current and the S_1 and S_2 currents.

$$\text{In Fig. 5, } i_{ph} + i_1 = i_2 \text{ and iph} = i_2 - i_1 \quad (14)$$

$$\text{and } i_1 = (i_{S1} - i_{D1}) \text{ and } i_2 = (i_{S2} - i_{D2}) \quad (15)$$

substituting (15) into (14),

$$i_{ph} = i_{S2} - i_{D2} - i_{S1} + i_{D1} \quad (16)$$

The power is related to the $(I_{RMS})^2$ of i_{ph},

$$\text{i.e. } I_{ph}^2 = (I_{S2}^2 + I_{D2}^2) + (I_{S1}^2 + I_{D1}^{2)} \quad (17)$$

Since the currents in $S_1 = S_2$ and currents in $D_1 = D_2$

$$\text{(17) reduces to, } I_{ph}^2 = 2I_{S1}^2 + 2\,I_1^2 \quad (18)$$

$$\text{And from (15), } \quad I_{ph}^2 = 2I_1^2$$

Total losses in Fig.5 model,

$$P_S = R_aI_1^2 + V_bI_1 + (V_{DC}^2)/R_c \quad (19)$$

$$\text{From (18), } Iph^2 = 2I_1^2 \quad \text{and } Iph = \sqrt{2}I_1 \quad (20)$$

$$\text{Therefore, } P_S = R_a(I_{ph}^2)/2 + V_b(I_{ph}/\sqrt{2}) + (V_{DC}^2)/R_c \quad (21)$$

Comparing (13) and (21),

$$a\,I^2_{ph} = R_a(I_{ph}^2)/2, \text{ and } R_a = 2a \quad (22)$$

$$b\,I_{ph} = V_b(I_{ph}/\sqrt{2}), \text{ and } V_b = \sqrt{2}b \quad (23)$$

$$c = (V_{DC}^2)/R_c \text{ and } R_c = (V_{DC}^2)/c \quad (24)$$

Having determined the values for "a", "b" and "c" in (13), the values for ($R_a = 2a$), ($R_c = (V_{DC}^2)/c$) and ($V_b = \sqrt{2}b$), can be applied in the proposed model in Fig.5. This model has been designed for the VSC circuit for validation of power losses obtained from manufacturers' software. The designers of the model confirm that with some fine tuning of the parameters, simulation power loss results compare closely to actual VSC circuit losses. [19]. With further adjustments, this simple model may be used as the switching device in a converter. The simulation to determine the power losses can be crossed checked using equation (21) with modifications as necessary.

C. Power Switching Device losses by PSpice Simulation

This is an example in PSpice, to show that a component (in this case the capacitor in an RC snubber circuit) can be varied over a range of values to determine the value that reduces the switch loss to a minimum during its turn-off transition period. The power loss for the switching device in the Schematic shown in Fig.7, is simulated by the process shown in the flow diagram in Fig.6. PSpice converts all non-linear components to linear equivalent models. It creates Nodal matrix of any Conductance (G) and Currents (I) and solves the corresponding linear Nodal equations for G x V = I. In Fig. 7, a random selection of values for R11 = 50Ω and C11 varied from 5µf to 50µf in increments of 5µf. The ten simulation runs resulted in a "family" of waveforms of voltage, current and power shown in Fig.8. Table1 shows the ten simulation runs with corresponding symbols used to identify each trace. These symbols are also presented below the PSpice time axis for V, I and W. The peak value of the yellow trace was the

lowest value of 201W and corresponded to the first simulation run giving the value for C11 = 5µf. The power traces show the effect of the variation of capacitor on the switch loss. The "□" symbol under Run 1, identifies the I, V and P traces for minimum power. The "grey" area has no entry.
In this example, the turn-off period, T = 50µs
The measured switch transition period, t_{off} = 90ns
The RC time constant tau, τ = 50Ω x 5µf = 250µs
Comparing these periods, τ = 5 x T and 2777 x t_{off}, which accounts for the 201W minimum power loss (in the family of traces) for the switch during t_{off}. i. e. the RC time constant was too large to effectively reduce the switch loss to a negligible value. In UPEC Paper 4, it was shown that selecting the RC time constant τ = t_{off}, or = ¼ x t_{off} would eliminate or reduce the switching loss to a negligible value. [20] [21] [22].

TABLE 1.V, I & P Traces' Symbols and Switch loss

No. of Runs	1	2	3	4	5	6	7	8	9	10
C11-µf range	5	10	15	20	25	30	35	40	45	50
Trace ymbols for V, I & P	□	◊	∇	Δ	○	+	x	λ	Y	*
I (3.8A)	□	This grey area of the table is redundant								
V (100V)	□									
Pmin (201W)	□									
C11-5µf	□									

R11 fixed at 50Ω

III. Conclusions

This paper presented seven non-simulation and six simulation methods which determine the switching device losses. One of the main cause of switching losses is in the use of hard switching. These losses have been critically described in the method of linear approximation assuming an ideal switch. To minimise these losses, the equations identified the relationship between these losses and the selection of switches with short switching times, and a short mark/space ratio of the switching frequency.

The design of a switching model was presented, based on the losses due to the high voltage spikes and oscillation, the conduction losses and the di/dt and dv/dt losses. These were represented in a basic three element differential equation and developed to determine the three related coefficients. The circuit model was derived by applying Thevenin's theorem and the values of the resistors and voltage generator were calculated from the analysis of the model differential equations. The final model can then be used in a schematic where the losses can be simulated.

Finally, a comprehensive PSpice PARAM simulation was carried out by sweeping through a range of capacitor values which resulted in a family of voltage, current and power traces. These traces show the effect of the capacitor value on the reduction of switching loss and also identified the particular capacitor value related to the minimum loss.

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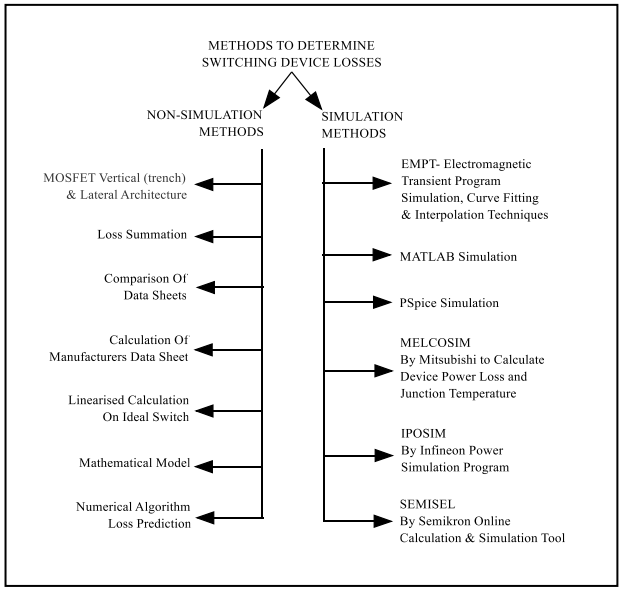

Fig. 1: Methods to Determine Switching Losses

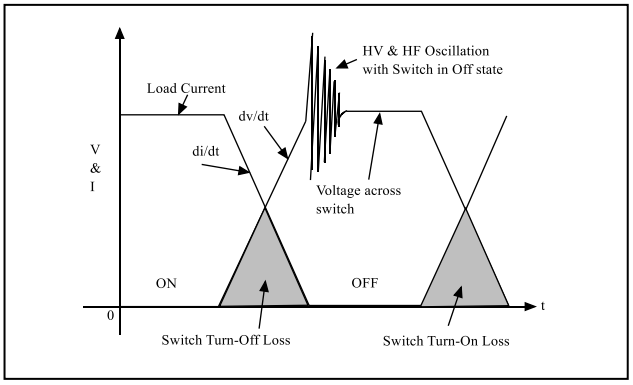

Fig. 2: Hard Voltage and Current Switching

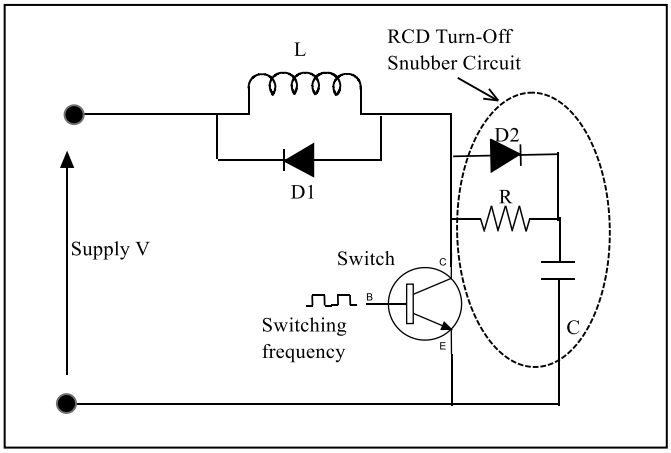

Fig. 3. Switch with inductive load
and turn-off snubber circuit

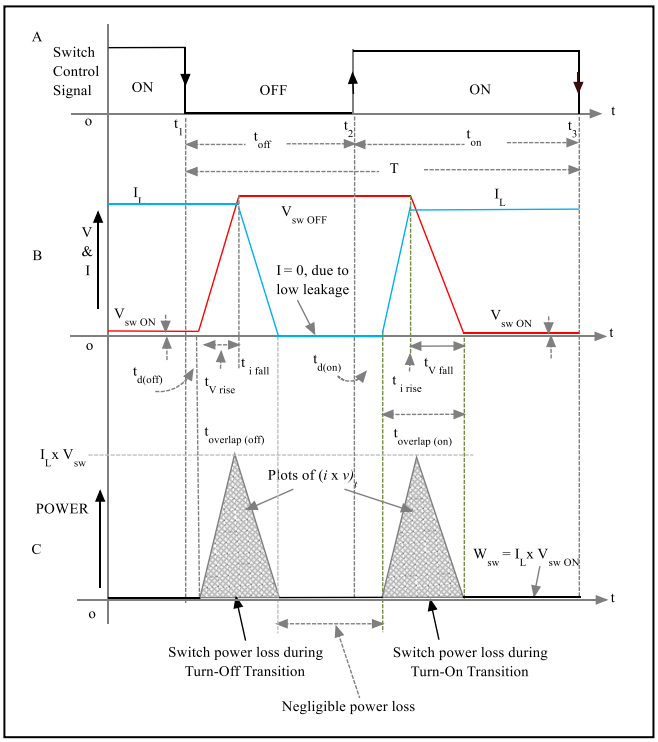

Fig. 4. Losses in ideal switch based on linear approximation
of V & I Switching waveform

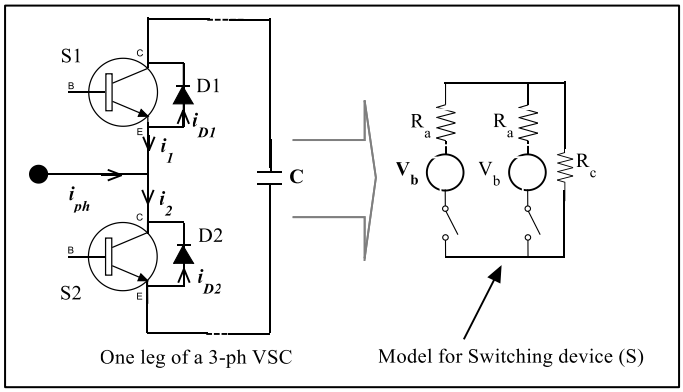

Fig.5. Model for a VSC switching Device

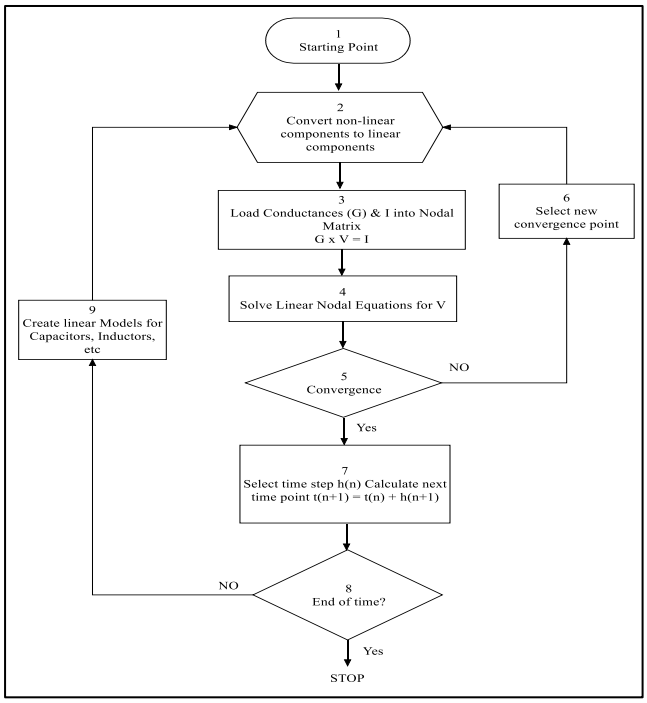

Fig. 6. Flow diagram of PSpice Working Algorithms

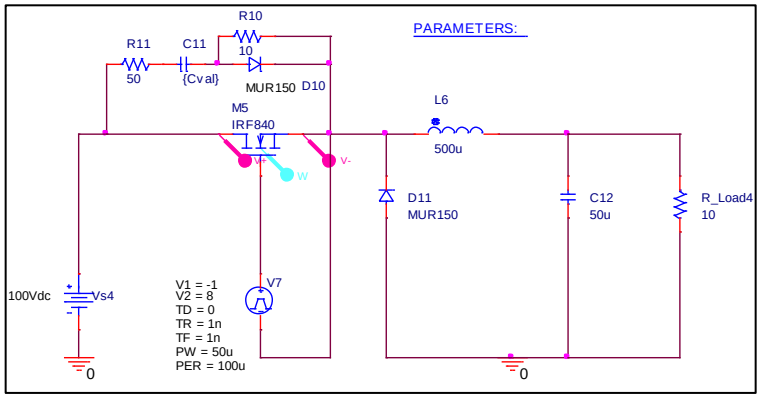

Fig. 7. PSpice Schematic for simulation of Switching device Power Loss

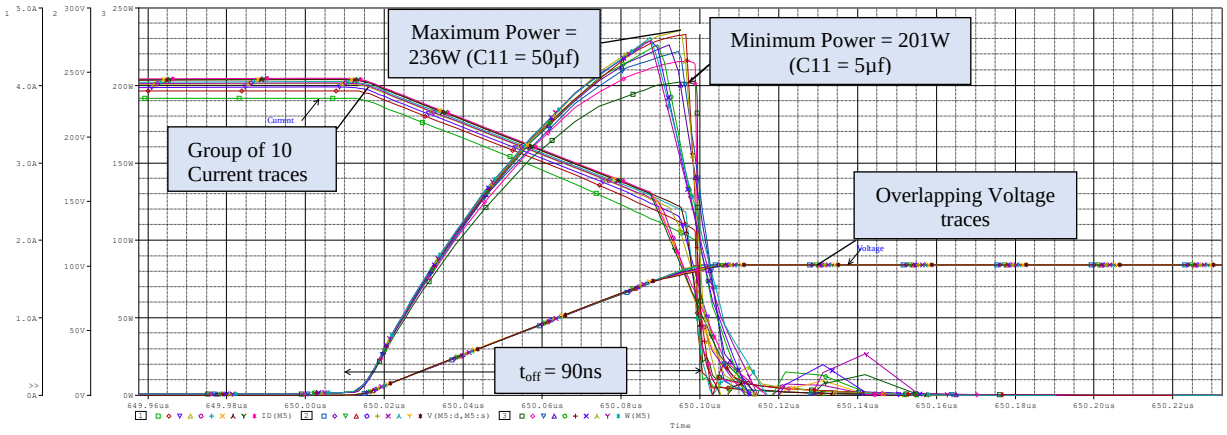

Fig.8. Family of Ten Traces of Voltage, Current and Power for Switching Device during the switching period t_{off}