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Conference Paper · July 2019

DOI: 10.1109/UPEC.2019.8893523

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Efficiency Investigation of A Protection and Correction Solid State Device for Low-Voltage Distribution Networks

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***Abstract* — A Solid State device which can limit and interrupt a fault, apply power factor correction and voltage regulation under normal conditions is presented with an investigation of its efficiency. The losses of the switching semiconductors are investigated by employing the PSIM Thermal Module. This work closely investigates the phase shift between the current and voltage waveforms for a 50Hz system and switching frequency of 5kHz before modelling and calculating the IGBT losses. For DC/DC converters the associated currents and voltages are in phase. However, as this work shows for switched capacitor circuits there is a 90^o phase shift between current and voltage. Finally, calculated losses are compared to simulated losses as well as to other methodologies suggested in literature.**

Keywords — ***Efficiency, Losses, Thermal Module, Fault Limiting, Switched Capacitor, Power Factor.***

I. INTRODUCTION

The switched capacitor circuit [1] – [9] which is inserted in series with the line, Fig.1 enables a number of functions to be performed that enhances power quality [10]. During normal operation the power factor is improved. In the event of a fault, the fault current is limited to safe levels and interruption is possible. The new feature which is presented in this paper is the correction of Voltage sags. Correction up to 14% is demonstrated with a certain set of L and C values. The efficiency of such a device inserted in the main flow of power in a Low Voltage Distribution Network is of paramount importance. The losses are identified in the switching semiconductor devices and the transformer.

The industry of power electronics and switched mode power supplies has been revolutionized by the introduction of semiconductor switches. Since, the introduction of transistors (bipolar and field effect) engineers and scientists are pushing the innovation envelope, producing products with higher durability and efficiency [11]-[13]. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Insulated Gate Bipolar Transistors (IGBT) have dominated the designs of switched mode power supplies [14], [15]. IGBT offer higher operating voltages than MOSFET. On the other hand MOSFET are cheaper and also offer higher switching speeds as compared to IGBT. As indicated by the data tabulated on Tables I and II, MOSFET offer much lower switching delays as compere to IGBT. The data of Tables I and II have been obtained or derived directly from the device datasheet [16]-[20].

Another very important selection criterion includes the losses of semiconductor devices which are divided into switching and conduction. As explained and analyzed in [21] and [22] the conduction losses of MOSFET are proportional to the on-resistance ($R_{DS(on)}$) and drain current (I_D), whereas in the case of IGBT are proportional to the collector-emitter saturation voltage ($V_{CE(SAT)}$) and collector current (I_C). The switching losses for both cases are proportional to the switching frequency.

For DC/DC converters the associated currents and voltages are in phase. However, as this work shows for switched capacitor circuits there is a 90^o phase shift between current and voltage. Therefore, this work closely investigates the phase shift between the current and voltage waveforms for a 50Hz system and switching frequency of 5kHz before modeling and calculating the IGBT losses.

II. THE OPERATION OF THE PROPOSED DEVICE

In this section the four functions of the circuit Fig.1 are presented. As shown in Fig. 1, the Switched Capacitor (SC) circuit is inserted in series with the load. By proper action of the two switches this circuit can limit the current in the event of a fault, improve the power factor in normal operation and correct to some extent voltage sags.

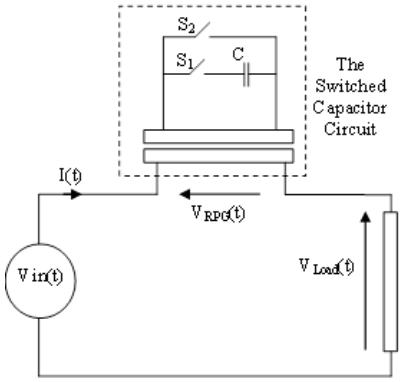

Fig.1: The Switched Capacitor Circuit.

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A. *Fault Limiting and Interrupption*

This function of the circuit is well explained in [1]-[9]. In the event of a fault the impedance of the SC circuit is increased accordingly by setting the duty cycle (D) of the switches. This impedance is reflected through the transformer to the line thus the current is limited to a safe value.

B. *Power Factor Correction*

The impedance of the SC circuit is set capacitive during the normal operation of the Low Voltage Network by setting the appropriate duty cycle of the switches. It was shown [1] that the power factor can be improved from 0.786 to 0.85. This is done with reference to Fig.2. For every value of the power factor PF, there is a corresponding value for the load voltage and the voltage across the semiconductor switches and the passive components of the switched capacitor, V_{SC}. From Fig. 2, D is found for the desired power factor. It is found from this graph that for power factor corrected to 0.85 lagging, the load voltage is always 5% higher than the supply.

C. *Voltage Sag Correction*

This is a new feature and it is taking advantage of the fact that the load voltage is increased with the insertion of the SC circuit, Fig. 2. As it was shown above, a compromise is achieved between power factor and acceptable increase of load voltage at D = 0.535 improving the power factor to 0.85 and allowing an increase of the load voltage of only 5%. This "disadvantage" of the SC circuit is turned into an advantage when there is a sag in the mains voltage at the point of connection. As indicated in Fig.2 it is possible to set the load voltage at about 12.5% higher with reference to the nominal voltage at the point of connection. The value of D is close to 1as read from Fig.2. Sag voltage correction is demonstrated in Fig.3 where a sag of 15.3% is corrected back to 236.9V, which is only 2.05% from its value before the disturbance.

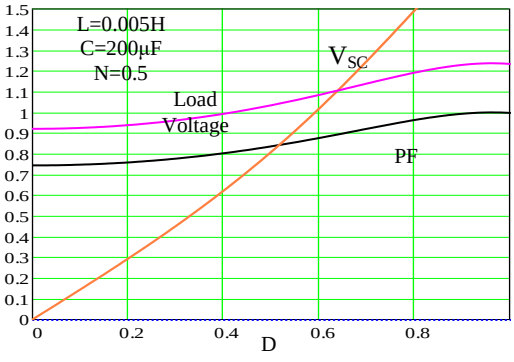

Fig.2: Power Factor and Circuit Voltages against the Duty Cycle of the Switches D.

III. Calculation of Losses

A. *Current Voltages of the Semiconductor Switches*

In order to derive the losses in the transistors the voltage across them and currents through them must be established. The duty cycle D of the switch S_1 the SC circuit in Fig.1 is such that the current is leading the supply voltage therefore the capacitor voltage is lagging the current by 90^o. The modes of the SC circuit are shown in Fig.4 (a) and (b). It is shown that the voltage across switch S_1 is the capacitor voltage reversed and the voltage across switch S_2 is the capacitor voltage. The ideal bidirectional switches of Fig.1 are implemented by two IGBTS connected as shown in Fig.4 (c).

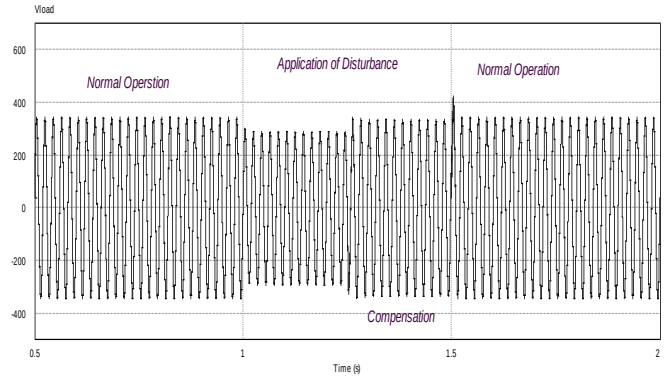

Fig.3: Voltage at the Connection Point.

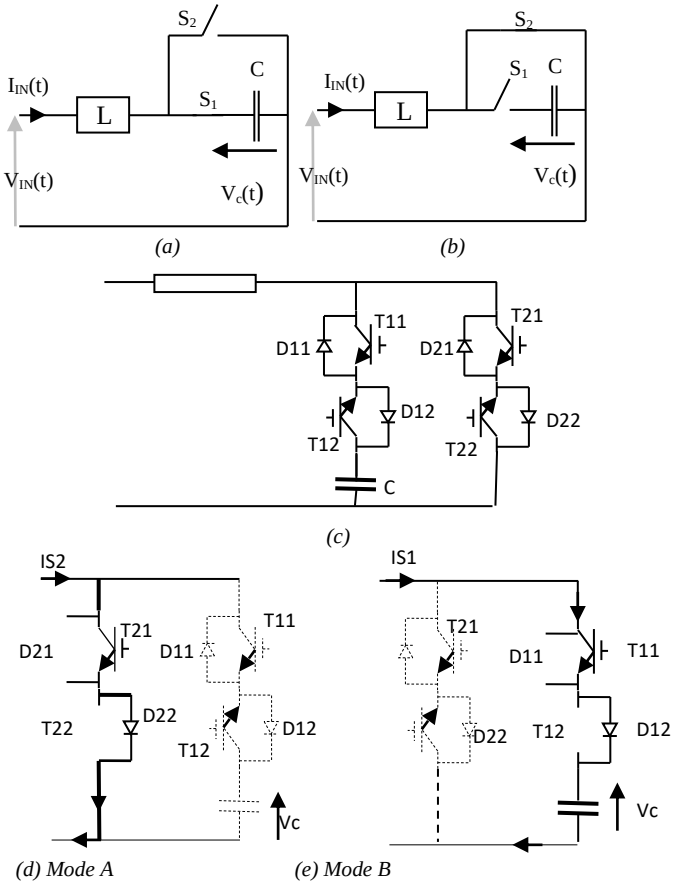

Fig.4: (a) and (b) Modes of the SC circuit (c) Implementation of the ideal switch $S_1$with bidirectional (d) Mode A and Mode B of the implemented circuit.

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The current in each branch of Fig.4 (c) can flow in both directions. In the branch with the capacitor, S1 is implemented with two IGBTs, T11 and T12. Each transistor has the usual anti-parallel diode. The current for S1, IS1 flows through T11 and D12 in one direction and through T12 and D11 in the opposite direction. In a similar way the current flows in the other branch.

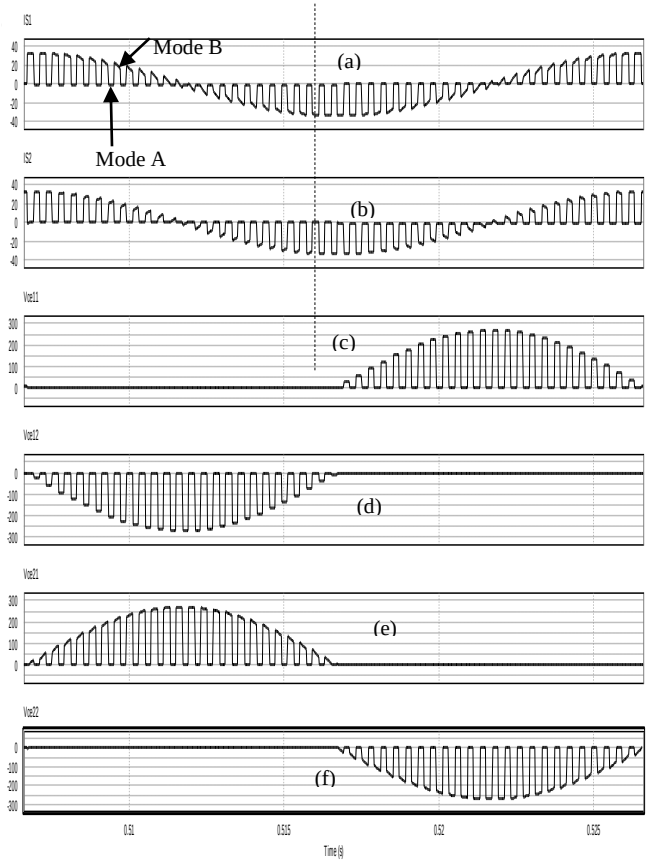

Fig. 5: Voltage Across and Current through the transistors
(a) Current through S1, (b) current through S2, (c) Voltage across transistor T11, (d) Voltage across transistor T12, (e) Voltage across transistor T21, (f) Voltage across transistor T22.

The chopped waveforms of voltages across the transistors and currents through them of circuit Fig.4a are shown in Fig.5. The modes of the circuit are increased to four (ABCD) with the implementation of S1 and S2 with IGBTs. Modes A and B are shown in Fig. 4 (d) and (e) only. In Mode A the current is positive; it flows downwards through T21, D22. The capacitor voltage appears across the non-conducting transistors in the other branch T11 and T12, +ve at Collector of T12 and –ve at cathode of D11 Fig. 4 (d). D11 is forward biased even though not conducting hence the voltage across it is practically zero, same with T11. The capacitor voltage therefore appears across T12, reversed, Fig.5.(d). Note that the current is a chopped cosine waveform Fig.5 (b). During this mode A the losses are the conduction losses in D21 and T22.

In Mode B Fig.4e the current is positive; it flows downwards through T11, D12. The capacitor voltage appears across the non-conducting transistors in the other branch T22 and T21, +ve at Collector of T21 and –ve at cathode of D22 Fig.4 (e). D22 is forward biased even though not conducting hence the voltage across it is practically zero, same T21. During this mode B the losses are the conduction losses in D12 and T11

Switching losses take place when one mode is replaced by the next one. Modes A and B are interchanged (A B A B …) during the Positive current half-cycle and Modes C and D are interchanged (C D C D…) during the Negative current half-cycle. Within one cycle of the switching frequency there are two mode changes e.g from mode A to mode B and back to mode A, Fig.5. For each change of mode a transistor and a diode are switching OFF and another transistor and a diode switching ON, two switching losses. From mode A to Mode B transistor T21and diode D22 are switching OFF and transistor T11 and a diode D12 switching ON. Since this process is repeated within one switching frequency cycle, the total switching losses within a cycle of the switching frequency is four times the losses of one transistor. Note that the losses in the reverse-connected diodes are neglected because according to the IGBT datasheets as shown on Tables I these free-wheel diodes offer superfast recovery; few ns instead of hundreds ns.

More specifically in the transition from A to B, T21 and D22 are switching OFF from a current given by $I_p cos(\omega nT)$ and the voltage across them is raised to $V_m sin(\omega nT)$ across them in t_{Fall} (ns). Because D22 is forward biased in mode B the voltage across it is practically zero for switching losses and this voltage appears across T21, Fig. 5 (e) (reversed but no problem!). At the same time T11 and D12 are switching ON from zero to a current $I_p cos(\omega nT)$ and the voltage is dropping from $V_m sin(\omega nT)$ to zero in t_{Rise} (ns), Fig.5 (c)

Therefore for each change of mode we have a transistor and a diode switching OFF and another transistor and a diode switching ON, two switching losses.

B. Losses During Normal Operation, no Disturbance

The use of the thermal module of PSIM to study the losses of semiconductor devices has been investigated by [23] whereas [1] derived the theoretical losses of IGBT. This work will investigate and compare the PSIM simulated results and the theoretical of IGBT-IXGT40N60C2D1 which is available in the PSIM Thermal Module Database.

TABLE I: IGBT CHARACTERISTICS at 25°C

Model	I_C (A)	$V_{CE(sat)}$ (V)	Delay (ns)		Rise / Fall (ns)	
			$t_{d(on)}$	$t_{d(off)}$	t_{Rise}	t_{Fall}
IXGT40N60C2D1	75	2.6	18	90	20	32
CM1000HA-24H	1000	3.6	600	1200	1500	350
F3L300R12PT4	460	2.15	210	380	90	70
FF450R12KE4	520	2.15	200	500	45	10
IRGPS60B120KDP	105	2.5	72	366	32	45

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TABLE II: MOSFET CHARACTERISTICS at 25ºC

Model	V_{DSBV} (V)	$R_{DS(ON)}$ (mΩ)	I_D (A)	Delay (ns)		Rise / Fall (ns)	
				$t_{d(on)}$	$t_{d(off)}$	t_{Rise}	t_{Fall}
STW45NM50	500	70	45	27	22	108	88
SCT30N120	1200	90	45	19	45	28	20
IRF3805	55	3.3	75	20	87	150	93
GS66516	650	25	60	4.6	14.9	12.4	22

As shown on Tables I and II, state of the art IGBT can handle much higher currents than MOSFET at the expense of much higher delays. Hence, MOSFET are the preferred choice for high switching applications.

Fig. 6 is the implementation of a bidirectional switch by two transistors T_1 and T_2 using the PSIM Thermal Module. This configuration replaces S1 and S2 in Fig.4 (a)and (b). This configuration includes the thermal resistances of the transistor and the diode, and the sum of the thermal resistances between the junction to case ($R_{th\text{-}jc}$), the case and heat sink ($R_{th\text{-}cs}$), and between the heat sink and the ambient ($R_{heatsink}$). The ammeters represent the conduction and switching losses in watts.

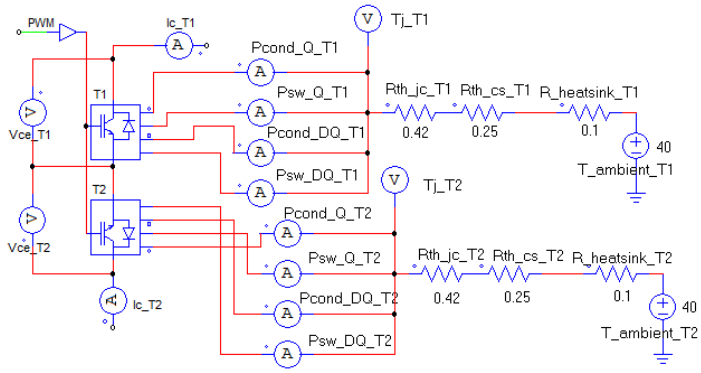

Fig.6: IGBT Configuration for conduction in both Cycles.

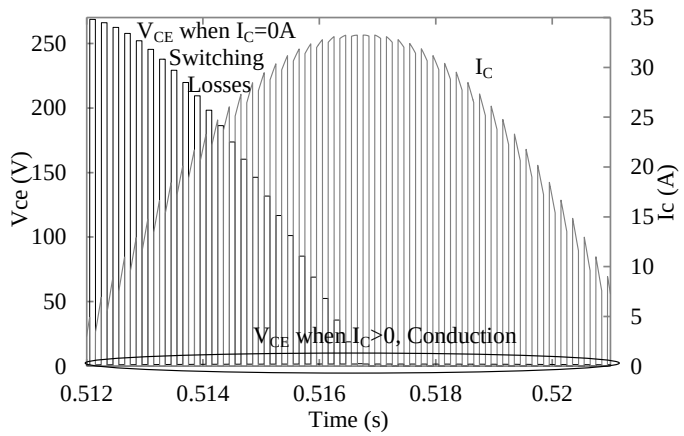

Fig. 7: IGBT Conduction Period.

As shown on Fig. 4, the collector current is best described as a half cycle (rectified) sinusoid signal. However, Fig. 7 clearly identifies the limits of integration. Hence, the average value given as:

$$I_{C\_AVG} = D\frac{1}{T}\int_{T/2}^{T} I_{C\_peak}\cos(\omega t)\,dt = D\frac{I_{C\_peak}}{\pi} \quad (1)$$

In addition the saturation collector-emitter voltage V_{CESAT}, is also described as a half cycle (rectified) sinusoid signals with the average value given as:

$$V_{CESAT\_AVG} = D\frac{1}{T}\int_{T/2}^{T} V_{CESAT\_peak}\sin(\omega t)\,dt \quad (2)$$

$$V_{CESAT\_AVG} = D\frac{V_{CESAT_{peak}}}{\pi} \quad (3)$$

Hence, as shown on Fig. 8, the average conduction losses, P_{cond_AVG}, given I_{C_peak}=33.2A, $V_{CESAT\ \_peak}$=1.66V and a switching frequency duty cycle, D of 50%, are given by

$$P_{cond\_AVG} = \frac{I_{C\_peak}V_{CESAT\_peak}}{\pi}D \quad (4)$$

Using (4) the conduction losses are calculated to 8.77W and are also tabulated on table III.

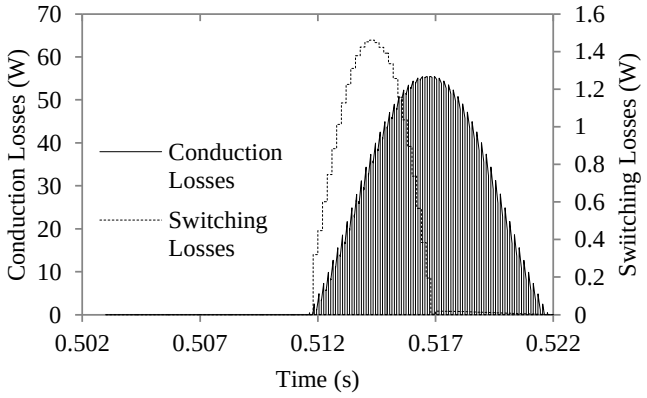

Fig. 8: IGBT Conduction and Switching Losses for f=50Hz, f_{SW}=5kHz and D=0.5.

The switching losses are composed of two components; turning-on and turning-off losses. These losses take into account the time it takes for the current and voltage to change state from ON to OFF and vice-versa. Referring to Fig. 7, they are described as a quarter cycle (rectified) signals one is cosine the other sinwave with the average value given as:

$$V_{CE\_AVG} = D\frac{1}{T}\int_{0}^{T/4} V_{CE\_peak}\sin(\omega t)\,dt = D\frac{V_{CE\_peak}}{2\pi} \quad (5)$$

Hence, including the switching delays, V_{CE_peak} is 269V then the losses can be rewritten as:

$$P_{sw} = P_{sw\_ON} + P_{sw\_OFF} \quad (6)$$

$$P_{sw} = \frac{f_{sw}DI_{C\_peak}V_{CE\_peak}}{2\pi}[t_{RISE} + t_{FALL}] \quad (7)$$

Using (7) the switching losses are calculated to 0.213W and are also tabulated on Table III. Worth noting, that the IGBT delays were adjusted for the rise in temperature. Based on the manufacturer datasheet when the junction temperature increases then the delay to turn on and rise times are not affected whereas the delay to turn-off and fall time is linear to

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the temperature change. Hence, for the IGBT used (IXGT40N60C2D1) for a temperature increase from 25°C to 46.4°C then the $t_{d(off)}$ increased from 90ns to 98.4ns and the t_f increased from 32 to 40ns.

TABLE III: COMPARISSON THEORETICAL (EQ.4 AND 7) AND SIMULATED SWITCHING LOSSES

Theory		PSIM Simulation		Difference	
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}
(W)	(W)	(W)	(W)	(W)	(W)
8.77	0.213	8.62	0.268	0.15	0.055

Equations 7 to 10 show the methodology suggested in [1] where losses are the summation of discrete values. Where V_{CE} and I_C is the peak operating values, T is the period of the switching frequency; M is the number of switching instances in a power cycle. The results are tabulated on Table IV.

$$E_{ON} = \sum_{n=1}^{M/4} \left[t_{RISE} \frac{1}{2} V_{CE} \sin(\omega.T.n) I_C \cos(\omega.T.n) \right] \quad (8)$$

$$E_{OFF} = \sum_{n=1}^{M/4} \left[t_{FALL} \frac{1}{2} V_{CE} \sin(\omega.T.n) I_C \cos(\omega.T.n) \right] \quad (9)$$

For the on-State the lost power is given by

$$P_{LossesSS} = \sum_{n=1}^{M/2} [t_{ON} V_{CEON} I_C \sin(\omega.T.n)] \quad (10)$$

The total losses using (7) to (9) can be rewritten as:

$$P_{LOSSES} = (P_{OFF} + P_{ON}).f_{sw} + P_{LossesSS} \quad (11)$$

TABLE IV: COMPARISSON SUMMATION OF DICRETE VALUES (EQ. 8 TO 11) AND SIMULATED SWITCHING LOSSES

Theory		PSIM Simulation		Difference	
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}
(W)	(W)	(W)	(W)	(W)	(W)
8.77	0.224	8.62	0.268	0.15	0.044

Comparison between the results tabulated on Tables III and IV shows that techniques, integration and summation of discrete values, are the same with only a small difference on switching losses of 0.009W. Another method as suggested in [24] is to calculate the switching losses is to normalize given the datasheet values. However, this method only works for the switching losses. Hence, expression (9) can be rewritten as:

$$P_{sw} = \frac{f_{sw} D I_C V_{CE}}{2\pi} \left[\frac{E_{ON}+E_{OFF}}{I_C V_{CE}} \right]_{Datasheet} \quad (12)$$

Taken directly from the datasheet for IGBT IXGT40N60C2D1 [6], I_C = 30A, V_{CE} = 400V, T_j=25°C, E_{ON} = 20mJ and E_{OFF}=30mJ then P_{sw} = 0.296W.

TABLE V: COMPARISSON DATASHEET NORMALISATION (EQ.12) AND SIMULATED SWITCHING LOSSES

Datasheet Normalization	PSIM Simulation	Difference
P_{sw}	P_{sw}	P_{sw}
(W)	(W)	(W)
0.296	0.268	0.028

Comparison between the results tabulated on Tables III to V shows that the PSIM simulation is the average between the Theory and Normalization methods. Worth noting that a closer investigation of the PSIM user manual revealed that for IGBT a normalization factor is used, including only the effects of V_{CE}.

TABLE VI: TOTAL POWER LOSSES FOR THE 4 IGBT

Datasheet Normalisation	PSIM Simulation	Theory
$P_{cond}+P_{sw}$	$P_{cond}+P_{sw}$	$P_{cond}+P_{sw}$
(W)	(W)	(W)
4x(0.296+8.77)	4x(8.62+0.268)	4x(8.77+0.213)
4x9.066	4x8.888	4x8.983
36.264	35.552	35.932

Table VI represents the total power. Multiplication by 4 is justified because within a cycle of the switching frequency we have two switching OFF and two switching ON actions. Specifically for the half cycle of positive current where modes A and B are interchanged, Within one cycle of the switching frequency A is replaced by B and then B by a. For each change of mode we have a transistor and a diode switching OFF and another transistor and a diode switching ON. ie from mode A to Mode B transistor T21and a diode D22 are switching OFF and transistorT11 and a diode D12 switching ON. This is repeated in the reverse order when mode B is replaced by A.

C. LOSSES ANALYSIS FOR THE COMPENSATION PERIOD

During voltage sags the system compensates so that the output load voltage remains almost constant (331.8V_{pk} = 236.9V_{RMS}, which is only 2.05% from its value before the disturbance). as shown on Fig.3 and 9. During the compensation the duty cycle of the switches D is set to 1 so only the branch with the capacitor conducts, only 2 IGBTs conduct; pair T1 and T12, Fig 4 (a). Therefore, the pair of T21 and T22 has zero conduction and switching losses. However, the pair experiences a sinusoidal collector-emitter voltage of 500V.

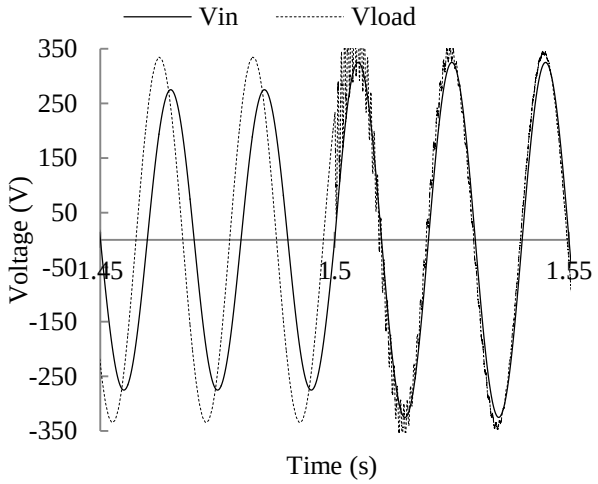

Fig.9: System Compensates for Voltage Sag.

During compensation the conducting pair of IGBT is kept ON with a duty cycle of 100%, D = 1. The collector current, I_C

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is 32.4A and the collectro-emitter voltage, V_{CE} is 1.65V. The simulated junction temperature is 52°C. Figure 10 show the simulated IGBT conduction losses. Hence, since the conductions losses of Fig. 10 looks like a half wave rectified sinusoid then the methodology described using equations (1) to (7) was used. The theoretical results are tabulated on Table VII. The values are for a single IGBT.

TABLE VII: COMPARISSON THEORETICAL AND SIMULATED SWITCHING LOSSES

Theory		PSIM Simulation		Difference	
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}
(W)	(W)	(W)	(W)	(W)	(W)
17.03	6.6u	15.6	5.7u	1.43	0.9u

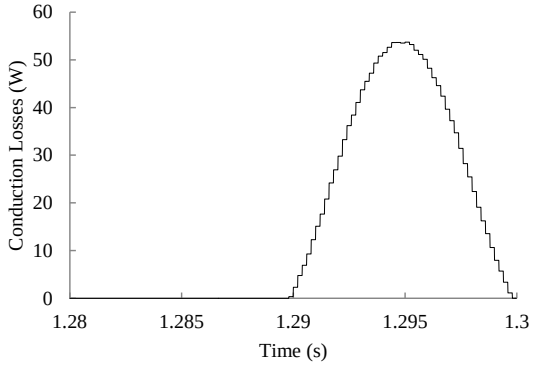

Fig. 10: Conduction Losses.

IV. DISCUSSION AND CONCLUSIONS

A Fault Current Limiter is presented where the SC Circuit is employed to correct the P.F. and at the same time it is a solid-state fault current limiting and interrupting device (FCLID) for low voltage distribution networks. Control is achieved by setting the value of the duty cycle of the switches. The choice of values of L and C is critical. Optimisation is applied to correct the power factor to an acceptable value of 0.85 and keep the load voltage within acceptable limits. For a lagging power factor of 0.85 the Load voltage is always 5% above the supply.

Sag voltage correction is a new feature and it is taking advantage of the fact that the load voltage is increased with the insertion of the SC circuit. As it was shown, a compromise is achieved between power factor and acceptable increase of load voltage; improving the power factor to 0.85 and allowing an increase of the load voltage of only 5%. As demonstrated it is possible to set the load voltage at about 12.5% higher with reference to the nominal voltage at the point of connection. Sag voltage correction is demonstrated where a sag of 15.3% is corrected back to $236.9V_{RMS}$ ($331.8V_{pk}$) which is only 2.05% from its value before the disturbance. This can either be tolerated or it is a useful feature in areas where the Grid voltage is low.

The losses of the switching semiconductors are investigated by employing the PSIM Thermal Module. This work shows that for switched capacitor circuits there is a 90° phase shift between current and voltage. Comparison between the calculated and simulated losses shows a difference of 150mW for conduction losses and 30mW for switching losses.

Finally, since this process is repeated within one switching frequency cycle, the total switching losses within a cycle of the switching frequency is four times the losses of one transistor, totalling 36W.

V. REFERENCES

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