

# Design and implementation of a modified Fourier analysis harmonic current computation technique for power active filters using DSPs

M.El-Habrouk and M.K.Darwish

**Abstract:** The design and implementation of a harmonic current computation technique based on a modified Fourier analysis, suitable for active power filters incorporating DSPs is presented. The proposed technique is suitable for monitoring and control of load current harmonics for real-time applications. The derivation of the basic equations based on the proposed technique and the system implementation using the Analogue Devices SHARC processor are presented. The steady state and dynamic performance of the system are evaluated for a range of loading conditions.

## 1 Introduction

The problem of power system harmonics has been addressed by many publications and has acquired a great deal of importance worldwide [1–5]. Various circuit topologies for active filters are available. These include the standard inverter circuit configurations [2–5], the switched capacitor systems [6–8], the lattice structures [9, 10] and the voltage regulator type arrangements [11, 12]. These circuits constitute the main building block in implementing appropriate active power filters. Fig. 1 shows a typical active filter incorporating the various control loops.

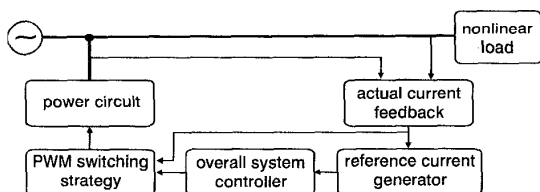


Fig. 1 Generalised block diagram for active filters

The response time of any active power filter is governed by three main factors:

- (i) the synthesis of the reference signal.
- (ii) the overall system controller.
- (iii) the response time of the power circuit.

The response of each of these blocks is crucial when assessing the possible delays between the change in the load current and the response of the filter. Factors (ii) and (iii) are beyond the scope of this paper and have been discussed elsewhere [2–5, 12]. Here the performance of the reference current generator is discussed and analysed. Compared with previous work, the proposed approach, incorporating

digital signal processors (DSPs) and a modified Fourier analysis, offers a much faster response, as demonstrated by the practical results.

## 2 Techniques for identifying current harmonics in load currents

There are many existing methods of identifying current harmonics in load current for single-phase and three-phase systems. Only the techniques suitable for single-phase systems are briefly reviewed below.

### 2.1 Analogue methods

This technique [3, 13, 14] uses a low-pass filter to identify the fundamental component of current, which is then subtracted from the total current to give a measure of the current harmonics. The design of the active filter has to incorporate at least a 6th-order filter to ensure a reasonable roll-off frequency. The main disadvantage with this method is that the fundamental component thus derived has magnitude and phase errors. The phase lag error normally reaches more than  $100^\circ$ , which is unacceptable for power filter applications. A phase-lead circuit can be used, but this introduces a phase shift of  $360^\circ$ , leading to a delay of one complete mains cycle, and is therefore not suitable for an application requiring a fast response.

### 2.2 Digital FFT calculations

This method [3, 15–17] is the most widely used. The FFT computation is performed by taking samples of one complete cycle (or an integral number of cycles) in order to generate the Fourier coefficients and to identify the low-frequency components in the load current. Therefore, it is suitable for slowly varying load conditions. Although this approach is more flexible than the analogue approach, there is still an inherent time delay equivalent to at least one complete mains cycle.

The computational time required for this case is enormous since the FFT computation takes a considerable amount of time. Resolutions of 12 and 14 bits (with a dynamic range over 10 bits, at least 0.1% dynamic error and 60dB SQNR) are normally required for the high-accuracy computations of active filter harmonics. Using cheap ( $\sim$ \\$10 per unit) and slow processors ( $\sim$ 20MHz), the amount

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The authors are with the Department of Electronic and Computer Engineering, Brunel University, UK

of time required to perform this operation may increase astronomically to reach several mains cycles. Therefore, this approach is not suitable for single-phase applications with fast varying loads (within one mains cycle), such as motor controllers and arc furnaces. It is, however, suitable for systems with slowly changing harmonic patterns (within 100ms), such as power system harmonics in medium- and high-voltage distribution networks [1, 2].

### 2.3 Fictitious power compensation algorithm

This technique relies on the principle of fictitious power compensation developed previously [18–20]. Despite opposition to the theory [21–23], this principle was proven to operate properly. The system controller attempts to generate a reference current signal, which minimises the undesired components of power (fictitious power). This technique is suitable for single-phase systems. However, it involves a large amount of computation.

### 2.4 Other algorithms

There are many harmonic estimation techniques, and all the utilities and libraries of the mathematical techniques can be used to perform this task. DSP algorithms, which form modifications of the FFT and DFT algorithms [17], may be used to correct the nonlinearities due to other techniques. Software implementations of signal filters as FIR or IIR filters can replace the analogue techniques outlined above. Other methods have been introduced, such as neural networks [24], adaptive [25, 26] and adaptive/predictive [27] estimation techniques, which are quite accurate and, of course, have a much better response.

These techniques require large amounts of computation; with the help of the state-of-the-art DSPs, they can fulfil their requirements within the specified sampling and control intervals. The computational burden on the DSP in some of these cases (neural networks and some adaptive techniques) is large, and most of the DSP time (30–250 $\mu$ s) is spent on the harmonic computation process. Our proposed technique introduces a different approach to the problem solution, in order to reduce the amount of time needed for the harmonic computations.

## 3 Proposed modified sliding-window Fourier analysis

The proposed method employs a modified sliding-window Fourier computational approach using a SHARC-21061 DSP, which overcomes the drawbacks associated with currently used methods.

### 3.1 Basic equations

For an arbitrary band-limited repetitive waveform  $x(t)$ , with a period  $T_{period}$  and consisting only of odd harmonics ranging from the fundamental  $\omega$  to  $(\omega \cdot N_{max})$ , the Fourier series equations are given by

$$x(t) = \sum_{\substack{i=1 \\ i \text{ odd}}}^{N_{max}} A_i \cos(i\omega t) + B_i \sin(i\omega t) \quad (1)$$

where

$$A_i = \frac{2}{T_{period}} \int_0^{T_{period}} x(t) \cos(i\omega t) dt \quad (2)$$

and

$$B_i = \frac{2}{T_{period}} \int_0^{T_{period}} x(t) \sin(i\omega t) dt \quad (3)$$

The above equations need to be modified in order to be used in DSP applications. Discretising the above equations at a fixed sampling interval  $\tau$ , and with a total number of points  $N_{points}$  per cycle, we obtain

$$x(k\tau) = \sum_{\substack{i=1 \\ i \text{ odd}}}^{N_{max}} A_i \cos(i\omega k\tau) + B_i \sin(i\omega k\tau) \quad (4)$$

where

$$k = 0, 1, 2, \dots, (N_{points} - 1) \quad \text{and} \quad \tau = \frac{T_{period}}{N_{points}}$$

and similarly

$$A_i = \frac{2}{N_{points}} \sum_{j=0}^{N_{points}-1} x(j\tau) \cos(i\omega j\tau) \quad (5)$$

and

$$B_i = \frac{2}{N_{points}} \sum_{j=0}^{N_{points}-1} x(j\tau) \sin(i\omega j\tau) \quad (6)$$

The above equations are still unsuitable for the fast computation of the instantaneous current harmonics because they require the signal to start (at  $j = 0$ ) from an initial fixed time.

This is, however, not the case for the sliding-window Fourier analysis since the starting point is always moving to the next one, once the new sampled point is available. This yields the following two equations (note that the index  $j$  ranges from  $N_{current}$  to  $N_{current} + N_{points} - 1$ ):

$$A_i = \frac{2}{N_{points}} \sum_{j=N_{current}}^{N_{points}+N_{current}-1} x(j\tau) \cos(i\omega j\tau) \quad (7)$$

$$B_i = \frac{2}{N_{points}} \sum_{j=N_{current}}^{N_{points}+N_{current}-1} x(j\tau) \sin(i\omega j\tau) \quad (8)$$

The modification in this case is still insignificant due to the large amount of calculation required to synthesise each harmonic amplitude and phase. The important point to note in this case is that the fundamental component is the only one needed in the active filtering application. This is implemented by calculating only the fundamental component and subtracting its value from the total load current. In this way, it is possible to obtain the total current harmonic, which in this case does not take a large amount of calculation.

The fundamental component  $x_1(k\tau)$  is given by

$$x_1(k\tau) = A_1 \cos(\omega k\tau) + B_1 \sin(\omega k\tau) \quad (9)$$

where  $k$  and  $\tau$  are as defined above. The factors  $A_1$  and  $B_1$  for the sliding-window system are

$$A_1 = \frac{2}{N_{points}} \sum_{j=N_{current}}^{N_{points}+N_{current}-1} x(j\tau) \cos(\omega j\tau) \quad (10)$$

and

$$B_1 = \frac{2}{N_{points}} \sum_{j=N_{current}}^{N_{points}+N_{current}-1} x(j\tau) \sin(\omega j\tau) \quad (11)$$

To obtain the instantaneous values of the desired signal in real time, the values of  $A_1$  and  $B_1$  have to be known at that same instant of time. This necessitates the evaluation of the summations in eqns. 10 and 11 at every sampling instant, which is still time consuming.

The better alternative would be to use the software capabilities of DSPs in handling arrays in order to implement the solution of eqns. 10 and 11 into two single-dimensional arrays. The consecutive values stored in each element of these two arrays correspond to the consecutive evaluations of the equations under the summation sign of the target equations (eqns. 10 and 11), respectively. The summation of all the elements of the two arrays,  $A_1$  and  $B_1$ , are then calculated only once during the initialisation of the system.

Fig. 2 summarises the approach proposed here. At each sampling interval, the old evaluated equations ( $N_{points}$  ago), which are stored in the indexed element of the arrays, are subtracted from the total saved sums of  $A_1$  and  $B_1$ , respectively. The sampled and calculated values of the new sampling interval are then introduced into the positions of the old ones. They are also added to the modified values of  $A_1$  and  $B_1$ , respectively, to produce the desired references for the variable under consideration (nonlinear load current) using eqn. 9. The system uses the principle of circular arrays [28] to represent the sliding-window problem. The amount of computations required for each coefficient is limited to one addition, one subtraction and one multiplication operation. The overall computation time is reduced significantly, and hence the calculation can be carried out within one DSP time slot.

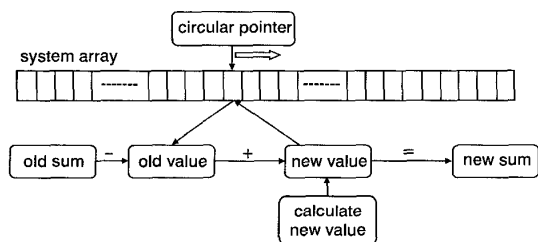


Fig. 2 Proposed computational system model

### 3.2 Hardware and software implementation

The hardware incorporates a 40MHz, ADSP-21061 SHARC DSP implemented in the SHARC EZ-KIT LITE [28, 29]. The basic kit incorporates a 14-bit analogue interface circuit (AIC) (AD1847). The analogue/digital converter is used for the acquisition of the load current signal, which is sensed using a Hall-effect current transducer. The on-board digital/analog interface is used to obtain the control signal from the DSP for monitoring purposes. The DSP board also includes several interrupt inputs and flag input/outputs. The flags are used to communicate the control signals between the DSP and the synchronisation circuits; this is an external custom-built board necessary to detect the starting edges of the supply-voltage waveform for the positive and negative half-cycles. These signals are isolated from the mains using 6N137 high-speed opto-couplers and are connected to the flag inputs of the DSP board.

The software uses a floating-point resolution of 64 bits. The program is written in C and dedicated for the SHARC family of DSPs. The flow chart of the program is shown in Fig. 3. The main role of the DSP is to calculate the harmonic content of the load current waveform. This harmonic content is then used to calculate the reference signal, which drives the active filter circuit. The program generates the following waveforms for controlling the filter:

(a) the fundamental component of the load current.

(b) the total harmonic content of the load current.

These resulting waveforms are then normalised into 12-bit integer format and then dispatched to the next software stage of the active filter controller (within the same DSP), which then performs the remainder of the control task.

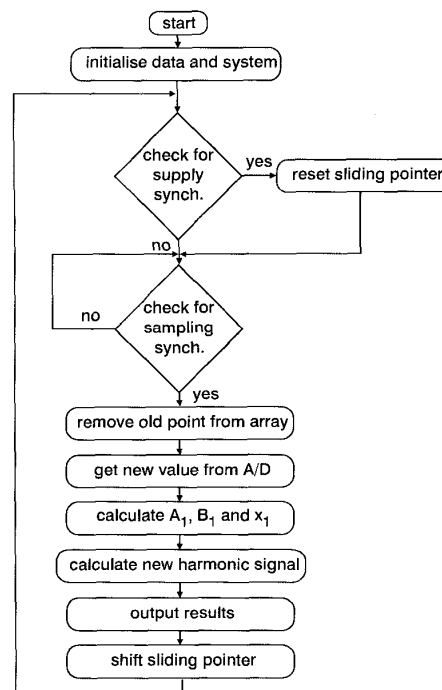


Fig. 3 Flowchart for harmonic computation program

The floating-point calculations were used in this program to minimise the computational overheads. This is important for the multiplication and division operations to avoid the necessity for normalising the magnitudes of the sine and cosine components generated by the DSP. Note that the sampling frequency of the analogue/digital converter onboard the DSP card is fixed at 25kHz, which corresponds to a sampling time of 40 $\mu$ s. The control and sampling sub-cycle is then limited by this value. The time taken to compute the proposed algorithm is 6 $\mu$ s, leaving the remaining 34  $\mu$ s for the overall active filter controller.

Note that by calculating only the sine component  $B_1$ , instead of both  $A_1$  and  $B_1$ , the system ends up acting as a compensator for current harmonics as well as fundamental reactive power; this is a major advantage of the system in terms of system flexibility.

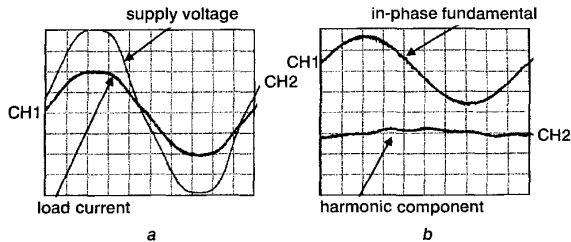
## 4 Practical results of harmonic current synthesis

The above computations lead to the system implementation for which the following results show its effectiveness. These results are shown in Figs. 4–9 for the various waveforms that were applied to the system to test its sensitivity and error analysis. Six different waveforms were applied to the system. The results for each case are listed below and are compared to the values measured with the harmonic analyser (Voltech PM100), and tabulated in the Appendix (Section 8).

### 4.1 Purely resistive load (sinusoidal current waveforms)

The simple case of a sinusoidal current waveform applied to the sensing and harmonic current calculation circuit is

shown in Fig. 4. Fig. 4a shows the supply voltage waveform with its phase relation with the load current; in this case, this is almost sinusoidal. The high-frequency noise on the signal is due to the quantisation error of the oscilloscope as well as the sampling noise, which accompanies the analogue/digital conversion process. Other sources of noise are due to the fact that the sensing of the sampled current is performed via the Hall-effect transducer which introduces additional noise. The load and supply parameters and characteristics are provided in the Appendix (Section 8).

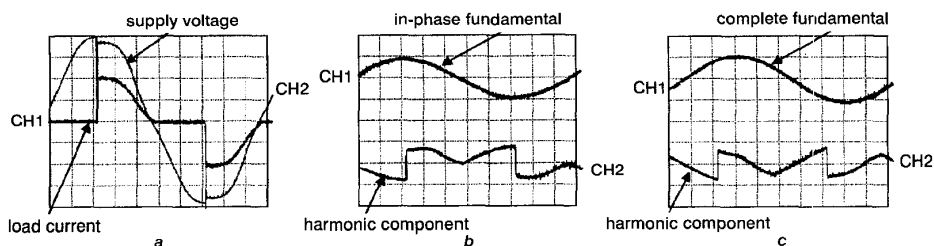


**Fig. 4** Practical results of reference current estimator for purely resistive load  
Voltage scale = 85V/div including voltage transducer gain; current scale = 6.25A/div including current transducer gain; 2ms/div

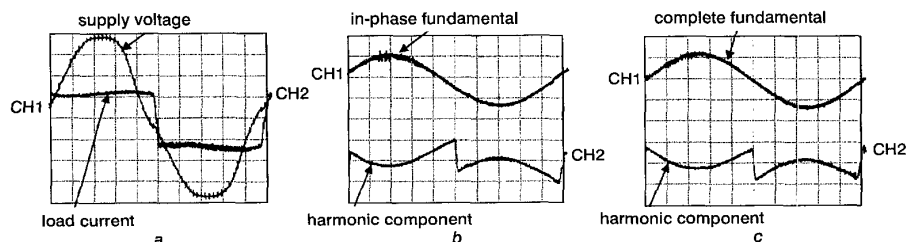
Fig. 4a shows a very small phase lag from the current waveform, which is confirmed by the value of  $5.9^\circ$  provided in the Appendix (Section 8). The second waveform, presented in Fig. 4b, provides the fundamental load current component, which is in phase with the supply voltage waveform. The harmonics present in the signal are, of course, negligible, but still exist, as is clear from the corresponding table in the Appendix (Section 8).

#### 4.2 Thyristor bridge with resistive load

Fig. 5 shows the overall performance of the system under the loading condition of a thyristor bridge feeding a pure resistance. Fig. 5a shows the supply voltage waveform with the load current, which is, of course, a replica of the output voltage waveform. The change of amplitude present in the voltage waveform signal is due to the voltage drop across the supply impedance. This drop is predominant in this case due to the presence of the series current measuring resistance as well as the output impedance of the auto-



**Fig. 5** Practical results of reference current estimator for thyristor bridge with resistive load  
Voltage scale = 85V/div including voltage transducer gain; current scale = 6.25A/div including current transducer gain; 2ms/div



**Fig. 6** Practical results of reference current estimator for thyristor bridge with inductive load  
 $\alpha \approx 0$ ; voltage scale = 85V/div including voltage transducer gain; current scale = 10A/div including current transducer gain; 2ms/div

transformer used to supply the circuit. The supply impedance is measured to be in the range of  $0.8\Omega$ .

Figs. 5b and c show the fundamental component of the load current as well as its total harmonic content. The difference here is that the first one shows the fundamental component which is in phase with the supply voltage (i.e. compensating for both harmonics and reactive power). The second waveform is the result of the calculation of both  $A_1$  and  $B_1$  in the C program. The magnitudes and phase shifts present in this case show good correspondence with the expected results provided in the Appendix (Section 8).

#### 4.3 Thyristor bridge with resistive/inductive load at minimum triggering angle

The most common case of load harmonic spectrum is, of course, the inductive load, which represents most of the industrial loads and conventional DC motor drives. The inductance value used in this case is around 180mH, which is a reasonably high value as expected in industrial cases. The corresponding current waveform, shown here in Fig. 6a in conjunction with the supply voltage, shows the smoothing effect of the highly inductive load present on the DC side of the thyristor bridge. Note that the triggering angle in this case is not exactly zero but is a minimum value of around  $13^\circ$ , as provided by the triggering module used in this case. The result would thus be a phase shift between the fundamental component representing only the harmonics (shown in Fig. 6c) and that incorporating both the harmonics as well as the reactive power compensation (shown in Fig. 6b).

The phase shift of about  $18^\circ$ , which is present between the two waveforms, constitutes a reasonable value when compared with the value of  $18.3^\circ$  provided in the corresponding table of the Appendix (Section 8) for the fundamental component of current. Note also that the non-perfectly flat-topped waveform results in the presence of distortions in each of the two quarter-cycles forming the positive and negative half-cycles. The harmonic components in the case of Fig. 6b (for which the fundamental current waveform is given to be in phase with the supply voltage) suffer from an unevenness of the positive and negative half-cycles rising and falling edges. This fact is correct for such type of waveforms, which confirms the accuracy of the implemented system.

#### 4.4 Thyristor bridge with resistive/inductive load at higher triggering angle

Similar to the above loading condition for load parameters and configuration, this case provides a different triggering angle for the load current sensed by the harmonic calculation. For the case of continuous DC side current, the waveform would simply alter by being phase-shifted, with its magnitude reduced as shown in Fig. 7a. The spikes shown at the transition points are due to the resonance effect between the snubber circuit capacitor connected across the thyristor and the supply inductance. This transient oscillation is due to the energy accompanying the step transition of current path between the two thyristor pairs.

The fundamental harmonic current signal, as shown in Fig. 7c is shown to lag the supply voltage waveform by a value of  $59.4^\circ$ , as compared to the value of  $58.5^\circ$  which is shown in the Appendix (Section 8). The thick traces in this case are due to the digitisation noise. Fig. 7b shows the waveform of the fundamental component which is the result of both the compensation of the harmonics and the reactive power of the load current.

#### 4.5 Thyristor bridge with resistive/capacitive load at minimum triggering angle

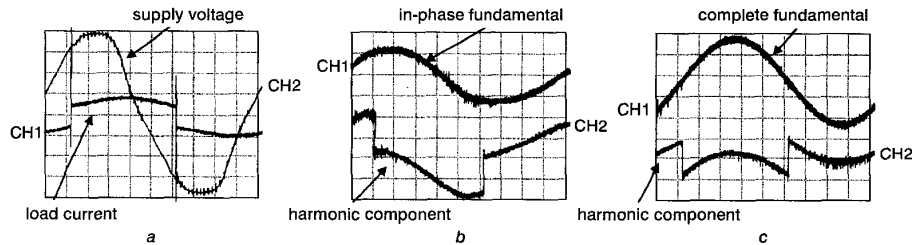
However uncommon in practice, this load configuration with a thyristor bridge is tested here for the sole purpose of providing the ability to change the wave shape and position of the pulse current, as shown below. This condition of a small triggering angle is similar, to a certain extent, to the case of a diode bridge feeding a rectifier DC-link capacitor, which is very common in AC/DC/AC inverter circuits. This same configuration with a diode bridge is mainly used for

the AC interface of switched mode power supplies. This widespread application (despite the fact that the harmonic pollution accompanying it is of negligible effect due to the extremely small values of currents involved with such systems) constitutes a great danger to the power quality and continuity [7].

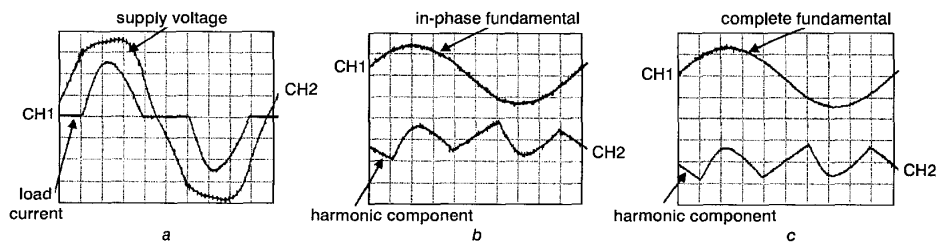
The high-amplitude current pulse generated here is shown in Fig. 8a for the load current and supply voltage waveform. As is clearly seen in this case, the supply waveform is non-sinusoidal. This would not change any of the system performances, except in the case of introducing further harmonics in the load current; in this case, this would be detected by the harmonic calculation system under investigation. Figs. 8b and c show the harmonic currents and the fundamental components corresponding to the two different cases of harmonic and reactive current compensation as well as harmonic current compensation, respectively.

#### 4.6 Thyristor bridge with resistive/capacitive load at higher triggering angle

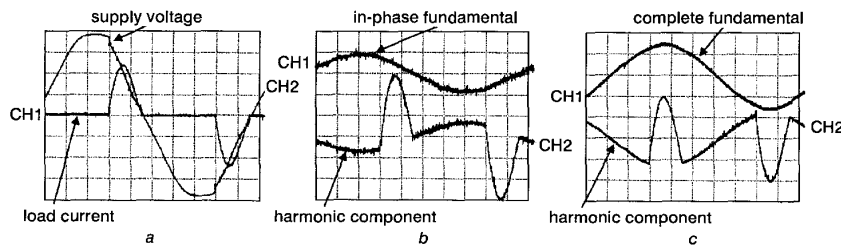
This load configuration is not of any industrial application at all. However, it is presented here for system performance demonstration. The main important characteristic of this waveform is its pulsed current during only a small portion of each half-cycle. The high-amplitude pulse can be shifted from the mid-region of the supply cycle to the right-hand side of the half-cycle. The width of the pulse reduces when shifted to the right at higher triggering angles. This is the main reason why such current waveforms (shown in Fig. 9a) are difficult to compensate. The reference estimator has to consider this huge amount of current before the



**Fig. 7** Practical results of reference current estimator for thyristor bridge with inductive load  
 $\alpha > 0$ ; voltage scale = 85V/div including voltage transducer gain; current scale = 10A/div including current transducer gain; 2ms/div



**Fig. 8** Practical results of reference current estimator for thyristor bridge with capacitive load  
 $\alpha > 0$ ; voltage scale = 85V/div including voltage transducer gain; current scale = 12A/div including current transducer gain; 2ms/div



**Fig. 9** Practical results of reference current estimator for thyristor bridge with capacitive load  
 $\alpha > 0$ ; voltage scale = 85V/div including voltage transducer gain; current scale = 12A/div including current transducer gain; 2ms/div

filter can respond to it. Note that the speed of detection of any variation in this signal is delayed by a few milliseconds since the presence of the zero current periods does not help the calculation process to predict the variation quickly enough.

Similar to the above systems, the fundamental component in phase with the supply voltage and that corresponding to the harmonic elimination are as presented in Figs. 9b and c, respectively. Note that the phase shift of  $54.6^\circ$  for the case of the total fundamental current component corresponds to a phase shift of about  $54^\circ$  in the estimated fundamental signal, which is acceptable under this severe loading condition. The supply voltage in Fig. 9a changes magnitude abruptly at the starting point of the capacitor charging process. This huge drop is because the current rate of rise is very high which interacts with the supply impedance.

## 5 Static and dynamic response

The proposed reference signal estimator is then used in conjunction with the other system signals to generate the control effort that will drive the PW modulator of the filter switching circuit. It is, however, important to check the system's static accuracy for the magnitudes and the phase errors.

The calibration of the measuring system can be performed taking into account the values measured for the true magnitude of the load fundamental and those calculated by the program. To compare these values, the readings must be calibrated and referred to directly directly in amps. This is performed using the case of a purely resistive load in conjunction with a sinusoidal waveform. The measured value of the fundamental component generated by the DSP (generated in volts) ( $0.8V$  from Fig. 4b) is used in conjunction with the magnitude measured with the harmonic analyser for the true value of the fundamental load current (from the table in the Appendix (Section 8):  $9.35 \times \cos(-5.9^\circ) = 9.3A$ ). If the latter is divided by the former, this results in the constant transformation value of

$$\begin{aligned} \text{const} &= 9.3/0.8 \\ &= 11.625 \text{ amps/peak volts} \end{aligned}$$

This value is then used to generate Table 1 from the data of Figs. 4–9. From this Table, it can be deduced that the percentage error does not exceed 0.925%, which is a good acceptable value for a system static accuracy.

The measurements of the phase angle errors are performed in Table 2. The depicted error values show that the maximum error occurs with a percentage error of 8.47%, which is very high. However, if the absolute error value of  $0.5^\circ$  is considered to be equivalent to a time difference of  $27.77\mu\text{s}$ , these small absolute error values can be ignored. The system in this case must then tolerate an error of double the magnitude of the sampling interval, which is in the order of  $1.44^\circ$ . It is obvious from the presented cases

that the system has a maximum value of the error in the order of  $0.9^\circ$ , which is well within the tolerance band.

**Table 1: Percentage errors in current magnitude measurements**

Case	Measured current (A)	True value (A)	% error
1	8.4	8.4	0
2	6.39	6.375	-0.235
3	7.556	7.6	0.579
4	5.81	5.85	0.645
5	14.5	14.4	-0.9
6	8.425	8.35	-0.925

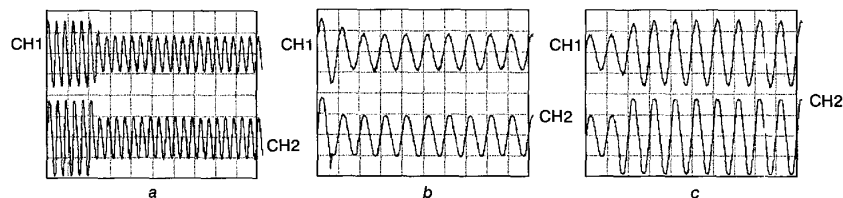
**Table 2: Percentage errors in current phase angle measurements**

Case	Measured phase	True phase	Absolute error	% error
1	$5.4^\circ$	$5.9^\circ$	$-0.4^\circ$	-8.47%
2	$34.2^\circ$	$34^\circ$	$0.2^\circ$	0.59%
3	$18^\circ$	$18.3^\circ$	$-0.3^\circ$	-1.64%
4	$59.4^\circ$	$58.5^\circ$	$0.9^\circ$	1.54%
5	$4.5^\circ$	$4.6^\circ$	$-0.1^\circ$	-2.17%
6	$54^\circ$	$54.6^\circ$	$-0.6^\circ$	-1.1%

The above error analysis performed for the calculations shows a good performance, which identifies a good accuracy characteristic for the proposed system. It now remains to analyse the performance of the system from the dynamic performance viewpoint. The system in this case while performing a one-cycle integration is expected to have a tracking error with a maximum of one whole cycle for zero estimation error. However, the practical case is much milder.

Consider the proposed system with a fast changing load, as given in Figs. 10 and 11. The various cases outlined show that the performance of the system is rather satisfactory and that the error reduces quickly with time. For cases like those in Fig. 10, which have a step change in the load magnitude either increasing (Fig. 10a near zero crossing and Fig. 10b near the peak) or decreasing (Fig. 10c), this affects the computation process. Note from the curves that the maximum error occurs for a graph like Fig. 10b (where the load current changes near the peak value of the sinusoidal waveform). This is the severest case, and a reasonable error value of the order of 10% can be obtained within less than one half-cycle.

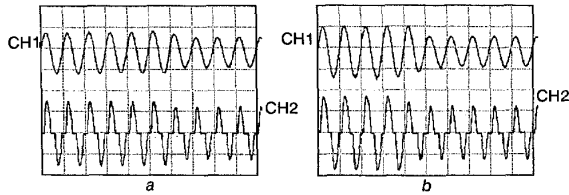
Fig. 11 shows a slowly varying resistive load connected across a rectifying bridge with a reservoir capacitor on the DC side. Part of the resistance is being switched out of the circuit (reducing the load current). The current decay is not



**Fig. 10** Practical results of reference current estimator with dynamic loading conditions

CH1 = calculated fundamentals; CH2 = actual load current waveform  
a Decreasing sinusoidal load current near zero crossing; 5A/div; 50ms/div  
b Decreasing sinusoidal load current near peak; 5A/div; 20ms/div  
c Increasing sinusoidal load current near middle cycle; 5A/div; 20ms/div

instantaneous. It is, however, sluggish, which gives the estimator reasonable time for the calculations to settle down. This mild condition is more expected in the cases of power system applications with slow changes.



**Fig. 11** Practical results of reference current estimator with dynamic loading conditions  
 CH1 = 5A/div; CH2 = 10A/div; 20ms/div  
 a Rectifier bridge with capacitive load current at high triggering angle  
 b Rectifier bridge with capacitive load current at low triggering angle

## 6 Conclusions

The implementation of the proposed technique on the SHARC processor shows a great deal of flexibility and a major reduction in computation time over ordinary techniques using standard FFT and DFT algorithms. It is well suited to the active filter application. If properly implemented even on slow and cheap platforms (such as the DSP kit used), it can serve as a fast method for generation of harmonic signals necessary for active power filter operation. The proposed harmonic estimator starts reacting to load changes after a maximum of 80 $\mu$ s, which includes the acquisition time (analogue/digital conversion delay) as well as the computation time. The dynamic response of the system is limited only by the averaging process, which is represented here by the integration necessary for the calculation of the Fourier coefficients. Practical results show that a maximum error of 10% can be reached within only one half-cycle. The numerous test results show that the system is robust and accurate for a range of test waveforms.

Furthermore, comparing this case with the ordinary slow FFT and DFT algorithms, the proposed system is superior owing to its ability to incorporate a larger number of samples per cycle according to the hardware capabilities of the processor (memory and computational speed) as well as the data acquisition system (analogue/digital acquisition and conversion), without degrading any of the system characteristics. A larger number of points can then be used to reduce the effect of noise using numerical manipulation techniques, such as averaging of several consecutive points or oversampling.

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## 8 Appendix

The supply parameters (including current measuring devices and auto-transformers) are given as follows:

$$R_{source} = 0.58 \Omega \quad L_{source} = 1.735 \text{ mH}$$

The measured load currents of the six loading conditions outlined in the paper are presented in Table 3, with the THD of each case measured using the harmonic analyser (Voltech PM100).

The current harmonics measured (A) from the harmonic analyser are given in Table 4.

The phase angles of the each of the harmonics measured from the harmonic analyser for the six cases are given in Table 5.

**Table 3**

Case	$I_{rms}$ (A)	$I_{pk}$ (A)	THD (%)
1	9.4	12.5	6.6
2	7.17	12.5	50.8
3	8.3	10.9	44.73
4	6.01	8.725	26
5	17	30	48.42
6	12.5	28.15	92.59

**Table 4**

Case	Fund	3rd	5th	7th	9th	11th	13th	15th	17th	19th
1	9.35	5.6%	3.3%	0.82%	0.4%	0.29%	0.07%	0.07%	0.08%	0.01%
2	6.375	41.9%	17%	12.6%	8.9%	8.75%	6.26%	5.95%	4.9%	4.63%
3	7.6	35.5%	19.5%	11%	7.8%	6.77%	5.6%	4.43%	3.64%	3.1%
4	5.85	21.7%	6.45%	6.23%	4.95%	4.18%	3.77%	3.2%	2.8%	2.34%
5	14.4	47.1%	5.8%	8.4%	1.36%	2.65%	1.4%	0.79%	1.15%	0.11%
6	8.35	74.3%	47.8%	24.4%	6%	6.46%	6.5%	2.95%	1.95%	2.96%

**Table 5**

Case	Fund	3rd	5th	7th	9th	11th	13th	15th	17th	19th
1	-5.9°	-66.7°	-124°	-83.3°	-222°	-217°	-99°	-19.5°	-18.4°	0°
2	-34°	-262°	-75.6°	-238°	-45.7°	-222°	-28°	-202°	-9.3°	-184°
3	-18.3°	-25.3°	-29°	-36.7°	-51.9°	-65°	-73°	-85°	-977°	-113°
4	-58.5°	-106°	-273°	-346°	-111°	-197°	-308°	-42°	-149°	-247°
5	-4.6°	-180°	-311°	44°	-76.8°	-234°	-256°	-70°	-86.5°	-212°
6	-54.6°	340°	-259°	-176°	-68.4°	-248°	-155°	-53.4°	-232°	-125°