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# Live Demonstration: Real-Time High-Amplitude Signal Acquisition with 2-Channel Modulo ADC

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***Abstract*—Modulo analog-to-digital converters (ADCs) offer a potential solution to the clipping challenges in conventional ADCs by folding signals that exceed the threshold. This makes them suitable for high-amplitude signal acquisition in wide dynamic range applications. In this demonstration, we present a 2-channel modulo ADC system implemented on a field-programmable gate array (FPGA) with an integrated real-time recovery algorithm. By managing both signal folding and recovery entirely in hardware, the system ensures low-latency processing. The FPGA efficiently handles high-bandwidth signals, making it a promising option for applications that require robust performance in high-amplitude signal environments.**

## I. Introduction

Modulo ADCs address signal saturation through signal folding. For an input $x \in \mathbb{R}$, the folding operation is defined as [1]:

$$\langle x \rangle_{\Delta} = \Delta \left( \left[\!\!\left[ \frac{x}{\Delta} + \frac{1}{2} \right]\!\!\right] - \frac{1}{2} \right), \quad [\![x]\!] \stackrel{\text{def}}{=} x - \lfloor x \rfloor, \qquad (1)$$

where $\lfloor \cdot \rfloor$ is the floor function and $\Delta$ represents the ADC's range. While modulo ADCs mitigate clipping, single-channel systems require high sampling rates, resulting in increased data volume and computational complexity. 2-channel modulo ADCs [2], [3] address this by distributing the signal across $L$ channels with progressively larger thresholds $\Delta_1 < \Delta_2$, reducing the sampling rate while maintaining dynamic range.

This demo presents a 2-channel modulo ADC sampling system based on the authors' prior work [2], [3]. The FPGA-based system implements real-time recovery in hardware, addressing challenges such as signal bandwidth and recovery complexity. The system consists of an analog front-end and an FPGA, as shown in Figure 1. The analog front-end monitors the input signal and, when it exceeds the threshold $\left[-\frac{\Delta_l}{2}, \frac{\Delta_l}{2}\right]$, $l = 1, 2$, the FPGA adjusts it via a digital-to-analog converter (DAC) to bring it within range. Each channel samples the folded signal at the Nyquist rate and sends it to the FPGA, where the recovery algorithm reconstructs the original signal in real-time.

## II. Demonstration Setup

The demo utilizes a basic signal, such as a sinusoidal wave from a generator, along with various input types to demonstrate the system's capabilities, as shown in Figure 2. A display will visually compare the clipped signal from a traditional ADC with the folded and recovered signals from the 2-channel modulo ADC. Additionally, data types, such as audio signals,will be demonstrated through software simulation, highlighting the system's potential applicability across a range of domains.

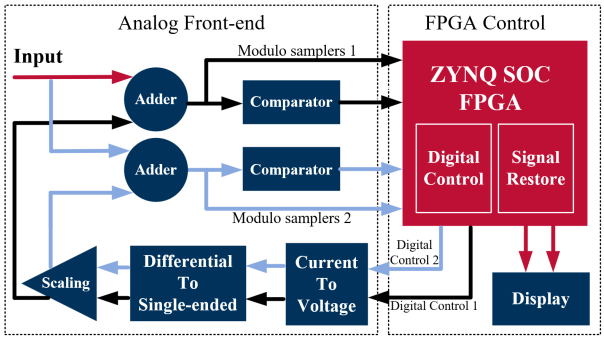
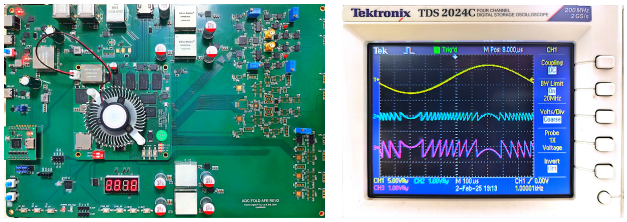



Fig. 1: Real-time 2-channel modulo ADCs sampling system.




(a) (b)

Fig. 2: Hardware prototype and modulo signal: (a) 2-channel modulo ADC prototype. (b) Input and modulo signals.

## III. Visitor Experience

Visitors will observe how the system handles various types of high dynamic range signals, demonstrating its practical application across multiple scenarios.

## References

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