



MAPS-based tracking and vertexing for the Electron–Ion Collider

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ABSTRACT

Experiments at the future Electron–Ion Collider (EIC) pose stringent requirements on the tracking system for the measurement of the scattered electron and charged particles produced in the collision, as well as the position of the collision point and any decay vertices of hadrons containing heavy quarks. Monolithic Active Pixel Sensors (MAPS) offer the possibility of high granularity in combination with low power consumption and low mass, making them ideally suited for the inner tracker of the EIC detector(s). In this contribution, we will discuss the configuration optimized for the ATHENA detector, selected physics performance metrics, and associated R&D towards a well-integrated, large-acceptance, precision tracking and vertexing solution for the EIC based on a new generation of MAPS sensors in 65 nm CMOS imaging technology.

1. Detector requirements

The needs to track the scattered electron and charged particles produced in the collision at the future Electron–Ion Collider (EIC) with good momentum resolution over a wide kinematic range, and to resolve primary from secondary vertices with high precision, can be satisfied by a well integrated, large acceptance detector featuring high granularity and low material budget.

The requirements for the detector, as defined in the Yellow Report [1], are the following:

- spatial resolution: $\leq 3 \mu\text{m}$ in the vicinity of the interaction region; $\leq 5 \mu\text{m}$ in the forward and backward directions, or at larger radii in the central region;
- reduced material budget: $< 0.1\% X_0$ close to the interaction region; $< 0.3\% X_0$ in the forward and backward directions; $< 0.8\% X_0$ at larger radii in the central region;
- power consumption in the 20–40 mW/cm² range;
- integration time lower than 2 μs .

In order to meet these requirements, the ATHENA Collaboration [2] proposed a vertexing and tracking system formed by a compact silicon barrel in the central region, consisting of three innermost vertex layers and two outer tracker layers, and two series of six and five silicon disks in the hadron and electron directions, respectively, complemented by Micro-pattern Gaseous Detectors (MPGDs) farther out. A schematic drawing of the proposed layout is shown in Fig. 1, and the preliminary dimensions and locations of layers and disks are listed in Table 1.

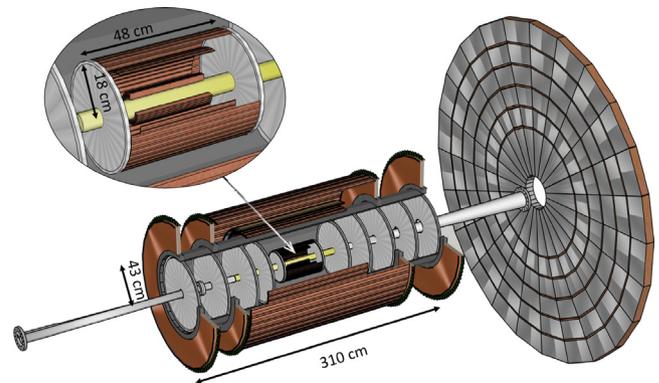


Fig. 1. The ATHENA vertexing and tracking system layout. Silicon barrel layers and disks around the beam pipe are shown completed by MPGD farther out. The inset shows the vertexing layers and the first forward and backward disks.

2. Technology choice and expected performance

The Monolithic Active Pixel Sensor (MAPS) technology offers the possibility of high granularity in combination with low power consumption and low mass, making them ideally suited for the inner tracker of the EIC detector. In particular, the specifications of the 30 cm wafer-scale MAPS sensor currently under development in 65 nm CMOS technology for the ALICE ITS3 detector [3] meet the EIC requirements. Simulations and geometry considerations show that the ITS3 conceptual design, consisting of large-area stitched sensors, thinned to less

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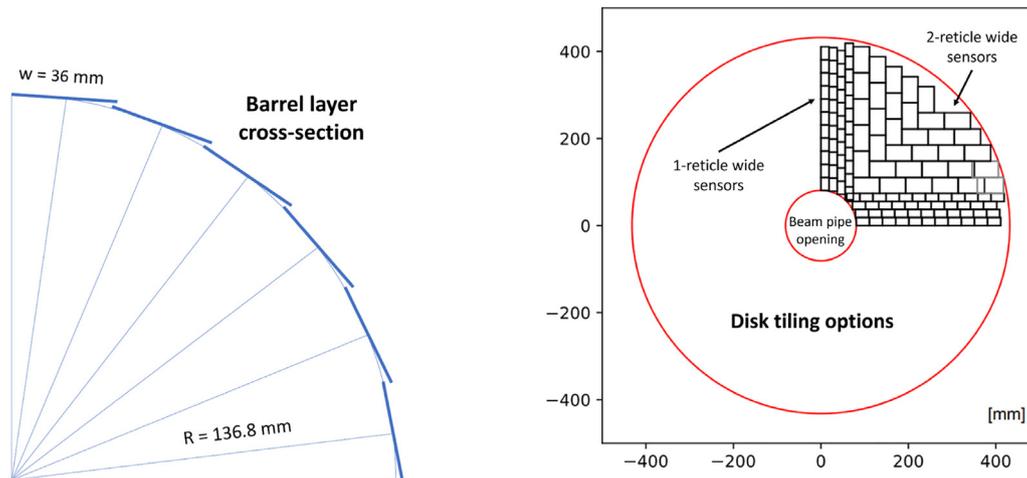


Fig. 2. Left: preliminary layout option for a ~ 137 mm radius barrel layer (cross section). Each stave is based on a sequence of ~ 36 mm-wide modules. Right: preliminary tiling option for the disks, based on two different sensor sizes (single reticle, 18 mm-wide and double reticle, 36 mm-wide sensors, respectively).

Table 1

Proposed dimensions and locations of the ATHENA silicon tracking and vertexing system layers and disks.

Layers	Radius (cm)	Length (cm)
L0, L1, L2	$\sim 3.5\text{--}6.0$	~ 29.0
L3, L4	$\sim 13.0\text{--}18.0$	$\sim 35.0\text{--}48.0$
Disks	Inner/Outer radius (cm)	Distance in z (cm)
6 forward	$\sim 3.5/43.0$	$\sim 25.0\text{--}165.0$
5 backward	$\sim 3.5/43.0$	$\sim 25.0\text{--}145.0$

than $50\ \mu\text{m}$, bent around the beam pipe and held in place using low mass carbon fiber support structures, can be directly adopted for the EIC Detector inner barrel. The target specifications and characteristics for the 65 nm CMOS sensor in preparation for the ITS3 are currently the following:

- pixel pitch: $15\ \sim\ 20\ \mu\text{m}$,
- power consumption: $\sim 20\ \text{mW}/\text{cm}^2$,
- integration time $\sim 200\ \text{ns}$,
- layout: wafer-scale (up to $\sim 28 \times 10\ \text{cm}^2$), thin ($20\div 40\ \mu\text{m}$), sensor, bent around the beam pipe,
- services: air cooling, carbon foam rings and cylindrical structural shell, no electrical interconnections in the active area,
- material budget: $\sim 0.05\% X_0$.

A dedicated development, consisting in the optimization of the ITS3 sensor size for high yield, low cost and large area coverage and in the minimization of the overall material budget, is required to use this technology for the tracking layers and disks, which are expected to be based on more conventional flat sensors, also stitched but not to wafer scale. The baseline design concept features a material budget of:

- $\sim 0.55\% X_0$ on the outer barrel staves,
- $\sim 0.24\% X_0$ on the forward and backward disks.

3. R&D items towards the EIC detector

An EIC Silicon Consortium (SC) formed in 2020 to develop a vertex and tracking detector for EIC. The SC is now engaged in the sensor

development and characterization within the ALICE ITS3 framework, with the main goals of estimating the stitched sensor yield, redefining the EIC-specific stitching plan for maximized yield and wafer-area usage, and potentially optimizing the sensor operations for EIC. A testing campaign focused on the estimate of the stitching yield and power distribution over long distances is foreseen to extend the testing conducted within the ALICE ITS3 Project. Alternative interconnection options will be studied to overcome potential weaknesses in the design.

The SC coordinates the development of a module concept to equip the large-area outer layers and disks, considering different tiling options to maximize the coverage with low material budget. The module will integrate the stitched sensor, the power and data networks, the support structure and the cooling system, in one unit which can be sequentially interconnected to form larger structures embedding services and data lines. The implementation of a redistribution layer and interconnection technology that allows a standardized assembly procedure in an industrial environment is under study. Modular LEGO structures are considered to apply the same module layout to staves and disks. Some of the preparatory work for the layout development is shown in Figs. 2 and 3.

In parallel, the EIC SC is leading the R&D towards the services reduction. The current activities focus on the optimization of the powering scheme, by investigating the use of radiation tolerant DC-DC converters and the serial powering with in-die or hybrid power regulations, and of the readout architecture, by considering on-detector data regulation through FPGA, reception over twinaxial cables or Flex Printed Circuits (FPC), and transmission over optical fibers. Once the conceptual design will be completed, the first prototypes implementing the different options will be produced in 2023.

4. Conclusions

A MAPS-based vertexing and tracking system has been proposed by the ATHENA Collaboration to satisfy the requirements posed by the EIC physics goals. The 65 nm CMOS imaging process offers the best solution for this detector: the large-area stitched sensor currently under development for the ALICE ITS3 project using this technology can be

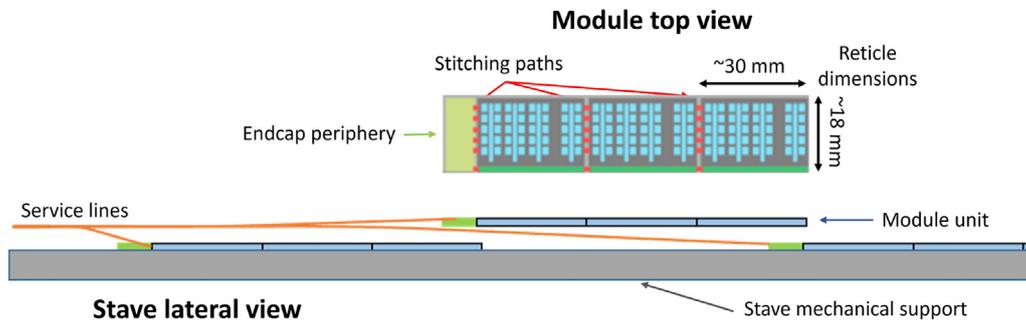


Fig. 3. Schematic drawing of the stave cross-section, imagined as a sequence of modules integrating the sensor (1×3 stitched reticles) and the interconnections on a common support structures. The top-view of a sensor unit is shown as a reference.

adapted to the EIC needs. The R&D activities towards the development of the detector concept and the infrastructure are now progressing well within the EIC Silicon Consortium in close collaboration with the EIC Detector-1 Tracking Working Group.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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