# Transport mechanisms in porous silicon

A. K. Ray, M. F. Mabrook, and A. V. Nabok
*Physical Electronics and Fibre Optics Research Laboratories, School of Engineering, City Campus, Pond Street, Sheffield S1 1WB, United Kingdom*

S. Brown
*School of Science, Sheffield Hallam University, Pond Street, Sheffield, S1 1WB, United Kingdom*

(Received 4 December 1997; accepted for publication 12 June 1998)

The current transport mechanism through porous silicon (PS) films fabricated from 8 to 12 Ω cm $p$-type silicon ($p$-Si) substrates has been investigated using current–voltage $I(V)$ measurements on metal/PS/$p$-Si/metal devices in the temperature range of 77–300 K. The characteristics for all devices show a rectifying behavior with ideality factor very close to unity. A value of 0.7 eV is obtained for the barrier height at the interface between PS and bulk $p$-Si at room temperature and the barrier height is found to increase with rising temperature. A band model is proposed in order to explain the observed characteristics. © *1998 American Institute of Physics.* [S0021-8979(98)02918-1]

## I. INTRODUCTION

Porous silicon (PS) has been identified as a potential optoelectronic material compatible with silicon technology after the discovery of strong room-temperature photoluminescence (PL) from high porosity PS in 1990.[1] Electroluminescence (EL) is also observed from Schottky diodes formed from PS under forward bias.[2,3] The origin of light emission has been extensively studied.[4–6] The similarity between PL and EL spectra indicates that a common recombination mechanism is involved in both cases but the quantum efficiency of the EL is smaller than that of the PL by at least one order of magnitude. In order to improve the efficiency, it is important to study the influence of recombination centers, surface states, and electrical contacts on the EL and PL. For this purpose, much attention is being paid to the studies of electric and photoelectric properties of PS-based structures. Zheng *et al.*[7] described the spectral response of a metal PS photodiode is essentially the same as for devices manufactured from crystalline silicon. According to Simons *et al.*,[8] PS fabricated from $n$-type substrates is $n$ type in nature and the Fermi level appears to be pinned by states on the surfaces of silicon wires within the PS film. Surface states play an important role. The exponential dependence of the dark conductance of a self-supporting PS on temperature is due to the tunneling between thermally vibrating sites placed on the surface.[9] In the majority of the work, the rectification in $I(V)$ characteristics is believed to be due to the existence of a Schottky barrier between the metal and PS interface.[10] However, an interpretation of rectifying characteristics due to the junction between the PS and its Si substrate is also reported in the literature.[11] The present investigation reports results of dc measurements on PS/$p$-Si structures sandwiched between two aluminum (Al) electrodes. The devices are biased at voltages less than 2.0 V. The range of voltages is important since the series resistance becomes a dominant factor for controlling current at relatively high voltages. Experimental results are analyzed in terms of a band model of a junction between PS and $p$-Si structures. The validity of this model is discussed in light of earlier experimental evidence due to Pulsford *et al.*[11]

## II. EXPERIMENTAL DETAILS

PS layers were prepared by the anodization of (100) $p$-type silicon substrates in a 1:1 solution of HF acid (49% in water) and ethanol at a current density of 25 mA/cm$^2$ for 10 min in the dark. Experiments have been performed with substrates having different resistivities in the range between 8 and 12 Ω cm. Before anodization, Ohmic contacts were deposited on the backside of the wafers by Al evaporation followed by annealing at 625 K for 30 min. Following anodization, the samples were rinsed in deionized water for 15 min, dried and transferred to a vacuum chamber to deposit thin Al contacts onto the PS surface to make electrical contacts. The metal evaporation was performed at a glancing angle between the molecular beam and the wafer in order to prevent direct contact between the silicon and the metal. The active area $S$ of the devices is found to be 0.3 cm$^2$. Gold was used for some of the samples for comparison with Al electrodes. Using a Keithley digital electrometer, the forward current is recorded when a positive voltage is applied to the metal contact on PS with respect to the Al contact on the $p$-Si substrate. Measurements are then repeated under reverse bias conditions.

## III. RESULTS AND DISCUSSION

Dc measurements were made in the dark on a number of samples of Al/PS/$p$-Si/Al structures for the temperature range between 150 and 300 K (room temperature). Figure 1 shows a set of typical current–voltage $I(V)$ characteristics at six different temperatures. The characteristics are found to be reversible and reproducible; and show a rectifying behavior. Measurements were also performed on structures fabricated under different conditions using various anodization currents and postanodization treatments. The $I(V)$ characteristics ex-

 

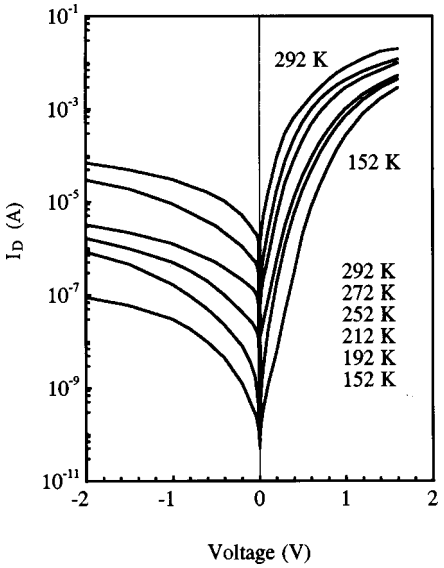


FIG. 1. Current–voltage $I_D(V)$ characteristics of Al/PS/$p$-Si/Al structures at different temperatures ranging from 150 to 293 K.

hibit similar rectifying features. The use of gold as a top electrode has produced no major effects on the results. This observation is in keeping with the previously published data for forward bias turn-on current through similar structures obtained with calcium, magnesium, and antimony as a top electrode material.[11] It has been found that the current turns on at the same value irrespective of the metal used as the top electrode. The present results, together with earlier observations, therefore, indicate that the interface between the metal and PS layer may not be responsible for rectification. Generally, this type of nonlinear dependence of the forward current $I_D$ on the applied bias voltage $V$ at temperature $T$ is written in the form:[12]

$$I_D = I_s \exp\left(\frac{q(V-I_D R_s)}{nkT}\right)\left[1-\exp\left(\frac{-q(V-I_D R_s)}{kT}\right)\right], \tag{1}$$

where $I_s$ is the zero-bias reverse current, $q$ is the electron charge, $n$ is the ideality factor, and $R_s$ is an appropriate series resistance. The reverse current does not appear to be saturating, but shows a voltage dependence. This may be indicative of carrier transport through a heterostructure. The form of Eq. (1) is chosen in order to account for the effects of thermionic-field emission and recombination of electron–hole pairs in the depletion region on transport mechanisms. Nonideal situations may also arise from a voltage dependence of the barrier height. Equation (1) is reduced to the law governing diffusion current due to thermonic emission for $n=1$ and $R_s=0$. The factor $[1-\exp(-qV/kT)]$ is found to be the most effective within the reverse bias range and the forward voltage regime up to $3kT/q$ when the series resistance $R_s$ becomes extremely small. The equation is a generic one and can be applied to describe the conduction through a barrier at both $p$-$n$ junctions and metal–semiconductor Schottky contacts. The relationship is physically significant

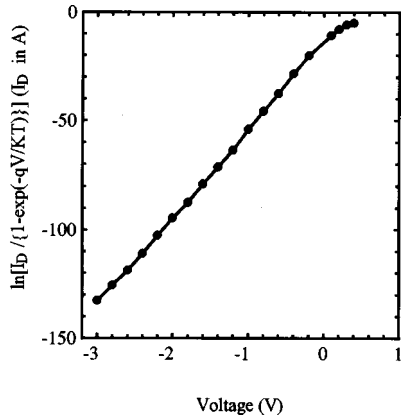


FIG. 2. Plots of $\ln[I_D/\{1-\exp(-qV/kT)\}]$ against $V$ for the same structure as in Fig. 1.

since the factors which are responsible for the nonideal behavior under the forward bias are active under the reverse bias.[13]

The series resistance $R_s$ and the ideality factor $n$ are used as adjustable parameters in order to obtain a theoretical fit to experimental curves. Figure 2 shows a plot of $\ln[I_D/\{1-\exp(-qV/kT)\}]$ against $V$ at room temperature. The resulting graph is linear within a voltage range of $-3.0\ \text{V} \leqslant V \leqslant 0.4\ \text{V}$ and the value of $n$ is found from the slope of the linear portion of the graph. By substituting the values for $n$ and $I_s$ into Eq. (1), an approximate value of $R_s$ is obtained. A least-squares-fitting procedure is then set up with these starting values for the adjustable parameters in order to achieve a satisfactory convergence between experimental and theoretical data at different temperatures over a wide range of bias voltage. Similar calculations have been performed for the remaining temperatures, and values of $R_s$ and $n$ are obtained with a standard error of less than 5%.

Figure 3 shows the dependence of series resistance $R_s$ and ideality factor $n$ on temperature $T$ between 150 and 300 K. $R_s$ is believed to be decreasing with temperature $T$ in an exponential fashion of the type: $R_s = R_0 \exp(\Delta E_R/kT)$ with $R_0 = 0.28\ \Omega$ and $\Delta E_R = 0.19$ eV. It is found that $n=1.13$ at $T=150$ K while $n=1.01$ at $T=290$ K. This indicates that the departure from the ideality is not significantly large. As

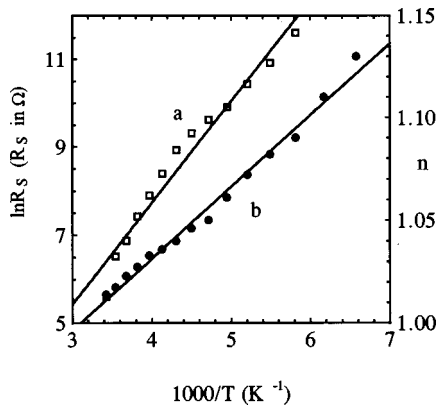


FIG. 3. A set of two graphs showing the variation of ideality factor $n$ and series resistance $R_s$ with respect to temperature $T$: (a) for $R_s$ and (b) for $n$.

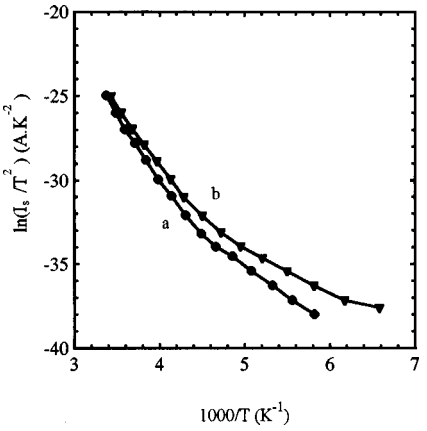


FIG. 4. Plots of $\ln(I_s/T^2)$ against (a) the reciprocal of $nT$ and (b) the reciprocal of $T$.

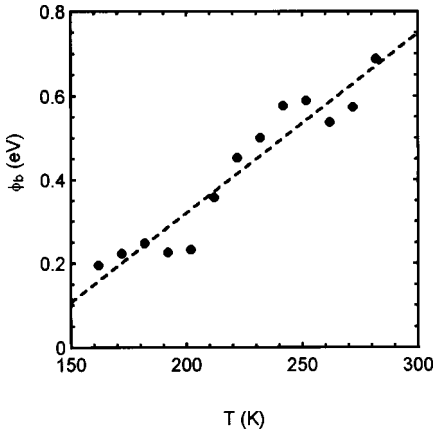


FIG. 5. The temperature dependence of equilibrium barrier height $\phi_b$.

shown in Fig. 3, the linear plot of $n$ versus temperature $T^{-1}$ gives a law for the temperature dependence of the ideality factor in the form:

$$(n-n_0)T=T_0, \tag{2}$$

where $T_0$ and $n_0$ are two constants. It is found that $n_0=0.897$ and $T_0=34$ K.

Assuming that the zero-bias reverse current $I_s$ is primarily due to the thermionic emission, the general behavior of $I_s$ can be written in a modified form:

$$I_s=AST^2\ \exp\left[-\frac{q\phi_b}{k(n_0T+T_0)}\right], \tag{3}$$

where $A$ is the Richardson's constant and $\phi_b$ is the equilibrium barrier height.

Figure 4 shows a plot of $\ln(I_s/T^2)$ against the reciprocal of the product of the ideality factor and temperature $(nT)$. The resulting graph is found to be nonlinear, implying that the barrier height $\phi_b$ is dependent upon temperature. Two dominant conduction processes, however, are believed to exist, giving values of 0.70 and 0.22 eV for activation energy corresponding to high- and low-temperature regimes, respectively. The transition between the two regimes is not abrupt but takes place gradually. The graph of $\ln(I_s/T^2)$ versus $T^{-1}$ is included in Fig. 4 for comparison. There is a tendency for convergence between the two plots at high temperatures, and therefore, it appears that thermionic emission diffusion processes are predominate at high temperatures. This observation is in agreement with the fact that ideality factor $n$ approaches to unity at high temperatures (see Fig. 2). The relatively small value of activation energy at low temperatures is believed to be associated with recombination currents. For further analysis, the value of $\phi_b$ is calculated by applying the midpoint rule as a function of temperature. The room-temperature value of $\phi_b$ is found to be 0.7 eV. As shown in Figure 5, there is a monotonical increase in barrier height $\phi_b$ with rise in temperature. The temperature coefficient $\alpha$ of the barrier height is estimated to be 4.3 meV $K^{-1}$ from the least-square linear approximation to experimental data.

It has been previously reported that porous silicon on a $p$-Si substrate behaves like $n$-type silicon.[11] The surface of silicon is usually positively charged due to the presence of surface states either on the silicon surface or in the native oxide. It is, therefore, expected that the surface is depleted of majority carriers, which are holes. This is a plausible assumption in light of recent experimental evidence.[14] The depth of depletion, the region which depends on carrier concentration and the surface charge of silicon, extends over a distance of a few tenths of microns into silicon. Taking into account that silicon rods in PS film have a thickness in the nanometer range, which is at least two orders of magnitude less than the depletion width, it can be easily inferred that the bulk of PS is depleted of holes. Depleted PS forms an Ohmic contact with the Al top electrode. It should be noted that the Au film as a top electrode, having a much higher work function ($\phi_M=5.2$ eV), does not make a significant difference in the $I(V)$ characteristics. The nature of porous silicon implies a very large effective surface area, and consequently, a large concentration of dangling bonds. The dominance of a very high surface charge density in PS is expected to fix the Fermi level in a certain position near the conduction-band edge. However, similar effects can be observed if the surface states are not adequately passivated, leaving an incomplete surface termination.

A band model is now proposed in Fig. 6 in order to account for the conduction in Al/PS/$p$-Si/Al devices. The validity of this model can be justified in light of reported results from the measurements of the short-circuit photocurrent when a laser beam is scanned across the cleaved edge of the PS layer.[11] The photoexcitation at the interface between

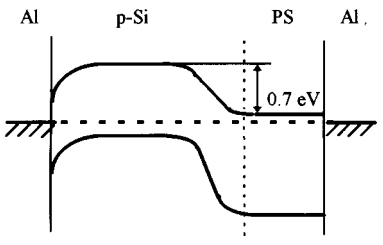


FIG. 6. A band model for Al/PS/$p$-Si/Al structures.

the metal and PS layer and across the PS layer produces no response, but a sharp increase in photoinduced current is found to have occurred when the region just inside the Si substrate is illuminated. The present band structure has also some similarities with the heterojunction model proposed for the photoelectronic properties of the PS layer in which the PS layer is assumed to have a much wider band gap than bulk Si.[15] Al layers form a Schottky contact with the $p$-type Si substrate, giving a blocking contact for holes but Ohmic for electrons. The electron current through the system is controlled by the barrier between $p$-Si and depleted PS, which can cause an observed rectification. The barrier height $\phi_b$ of 0.70 eV obtained experimentally, therefore, corresponds to the barrier between the $p$-Si substrate and PS layer. The temperature coefficient $\alpha$ of the barrier height $\phi_b$ can be written as

$$\alpha=\left[\frac{\partial E_{F(\mathrm{PS})}}{\partial T}-\frac{\partial E_{F(p\text{-Si})}}{\partial T}\right], \tag{4}$$

where $E_{F(\mathrm{PS})}$ and $E_{F(p\text{-Si})}$ represent the Fermi levels of the PS layer and the $p$-silicon substrate. The value of the second term $(\partial E_{F(p\text{-Si})}/\partial T)$ is estimated to be 0.7 meV $\mathrm{K}^{-1}$. The value of $(\partial E_{F(\mathrm{PS})}/\partial T)$ is approximately equal to 5.0 meV $\mathrm{K}^{-1}$. The phenomenological description of the temperature dependence of the barrier height using the equation of carrier transport due to thermionic emission is adequate since the reverse current in a heterojunction shows an exponential dependence on temperature.[16] Because of the band-gap inhomogeniety, Fermi-level $E_{F(\mathrm{PS})}$ of porous silicon is, however, a spatially dependent quantity and it is, therefore, expected that there will be a distribution of values of $(\partial E_{F(\mathrm{PS})}/\partial T)$ over the interface. The value of 5.0 meV $\mathrm{K}^{-1}$ is believed to represent an average of the coefficients for this distribution. The position of the Fermi level with respect to the conduction band in the PS layer is influenced by the thermal generation of minority carriers. The series resistance $R_s$ represents the net resistance of depleted PS and the nonactive region in the silicon substrate and its value is also largely controlled by the thermal generation of minority carriers (electrons) in the PS layer. This is why an increase of barrier height $\phi_b$ and a decrease of series resistance $R_s$ with temperature are observed.

## IV. CONCLUSIONS

Electrical conduction properties of Al/PS/$p$-Si/Al have been investigated at relatively low bias voltages. The present experimetal results indicate that PS films behave like $n$-type Si due to their depletion of majority carriers (holes). The Fermi level appears to be positioned near the conduction band and it is also possible that the inhomogeneous band gap of the PS film has an effect of destorting barrier height $\phi_b$ to a relatively small value at lower temperatures. The observed rectification of electron current is found to be caused by the barrier between $p$-Si and PS. The value of the ideality factor close to unity is interpreted as evidence that the Si/PS junction characteristics are controlled by carrier diffusion in the PS. The low value of ideality factor $n$ is consistent with the diffusion model of charge carriers in an ideal $p-n$ junction. The proposed band model, therefore, gives a qualitative explanation for the main features of dc conduction in Al/PS/$p$-Si/Al structures.

## ACKNOWLEDGMENTS

The authors are grateful for the fruitful discussions with Dr. J. R. Travis and Professor J. Atkinson for stimulating discussions. Thanks are due to G. France for his technical help.

[1] L. T. Canham, Appl. Phys. Lett. **57**, 1046 (1990).
[2] N. Koshida and H. Koyama, Appl. Phys. Lett. **60**, 347 (1992).
[3] A. Halimaoui, C. Oules, and G. Bomchil, Appl. Phys. Lett. **59**, 304 (1991).
[4] S. Sawada, N. Hamada, and N. Ookubo, Phys. Rev. B **49**, 5236 (1994).
[5] B. Bessais, H. Ezzaouia, H. Elhouichet, M. Queslati, and R. Bennaceur, Semicond. Sci. Technol. **11**, 1815 (1996).
[6] F. Xue, X. Bao, and F. Yan, J. Appl. Phys. **81**, 3175 (1997).
[7] J. P Zheng, K. L. Jiao, W. P. Shen, W. A. Anderson, and H. S. Kwok, Appl. Phys. Lett. **61**, 459 (1992).
[8] A. J. Simons, T. I. Cox, M. J. Uren, and P. D. J. Calcott, Thin Solid Films **255**, 12 (1995).
[9] J. J. Mares, J. Kristofik, J. Pangrac, and A. Hospodkova, Appl. Phys. Lett. **63**, 180 (1993).
[10] D. B. Dimitrov, Phys. Rev. B **51**, 1562 (1995).
[11] N. J. Pulsford, G. L. J. A. Rikken, Y. A. R. R. Kessener, E. J. Lous, and A. H. J. Venhuizen, J. Appl. Phys. **75**, 636 (1994).
[12] S. Chand and J. Kumar, J. Appl. Phys. **80**, 288 (1996).
[13] M. Missous and E. H. Rhoderick, Electron. Lett. **22**, 477 (1986).
[14] T. Ozaki, M. Araki, S. Yoshimura, H. Koyama, and N. Koshida, J. Appl. Phys. **76**, 1986 (1994).
[15] D. Stievenard and D. Deresmes, Appl. Phys. Lett. **67**, 1570 (1995).
[16] S. M. Sze, *Physics of Semiconductor Devices* (Wiley-Interscience, New York, 1981).